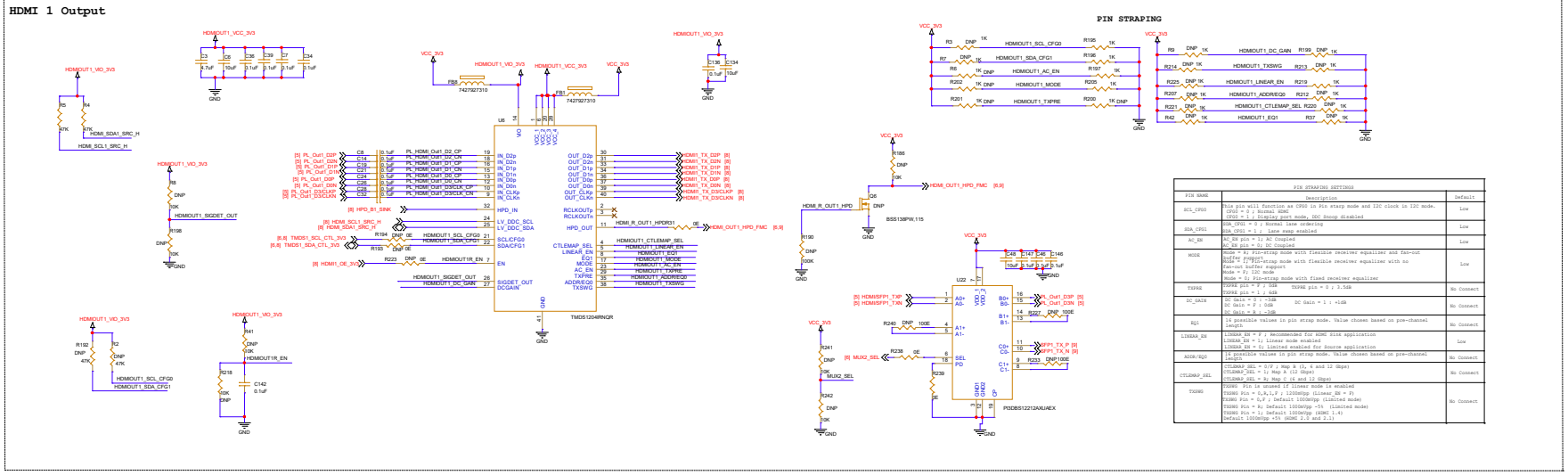
HDMI 1 Output



PIN STRAPING SETTINGS		
PIN NAME	Description	Default
SCL_CFG0	This pin will function as CFG0 in Pin strap mode and I2C clock in I2C mode. CFG0 = 0 ; Normal HDMI CFG0 = 1 ; Display port mode, DDC Snoop disabled	Low
SDA_CFG1	SDA_CFG1 = 0 ; Normal lane ordering SDA_CFG1 = 1 ; Lane swap enabled	Low
AC_EN	AC_EN pin = 1; AC Coupled AC_EN pin = 0; DC Coupled	Low
MODE	Mode = 8; Pin-strap mode with flexible receiver equalizer and fan-out buffer support Mode = A; Pin-strap mode with flexible receiver equalizer with no fan-out buffer support Mode = F; I2C mode Mode = 0; Pin-strap mode with fixed receiver equalizer	Low
TXPRE	TXPRE pin = F ; 0dB TXPRE pin = 0 ; 3.5dB TXPRE pin = 1 ; 6dB	No Connect
DC_GAIN	DC Gain = 0 : -3dB DC Gain = F : 0dB DC Gain = 1 : +1dB DC Gain = 8 : -3dB	No Connect
EQ1	16 possible values in pin strap mode. Value chosen based on pre-channel length	No Connect
LINEAR_EN	LINEAR_EN = F ; Recommended for HDMI Sink application LINEAR_EN = 1; Linear mode enabled LINEAR_EN = 0; Limited enabled for Source application	Low
ADDR/EQ0	16 possible values in pin strap mode. Value chosen based on pre-channel length	No Connect
CTLEMAP_SEL	CTLEMAP_SEL = 0/F ; Map B (3, 6 and 12 Gbps) CTLEMAP_SEL = 1; Map A (12 Gbps) CTLEMAP_SEL = 8; Map C (6 and 12 Gbps)	No Connect
TXSWG	TXSWG Pin is unused if linear mode is enabled TXSWG Pin = 0,A,1,F ; 120mVpp (Linear_EN = F) TXSWG Pin = 0,F ; Default 100mVpp (Limited mode) TXSWG Pin = 8; Default 100mVpp -5% (Limited mode) TXSWG Pin = 1; Default 100mVpp (HDMI 1.4) Default 160mVpp +5% (HDMI 2.0 and 2.1)	No Connect

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