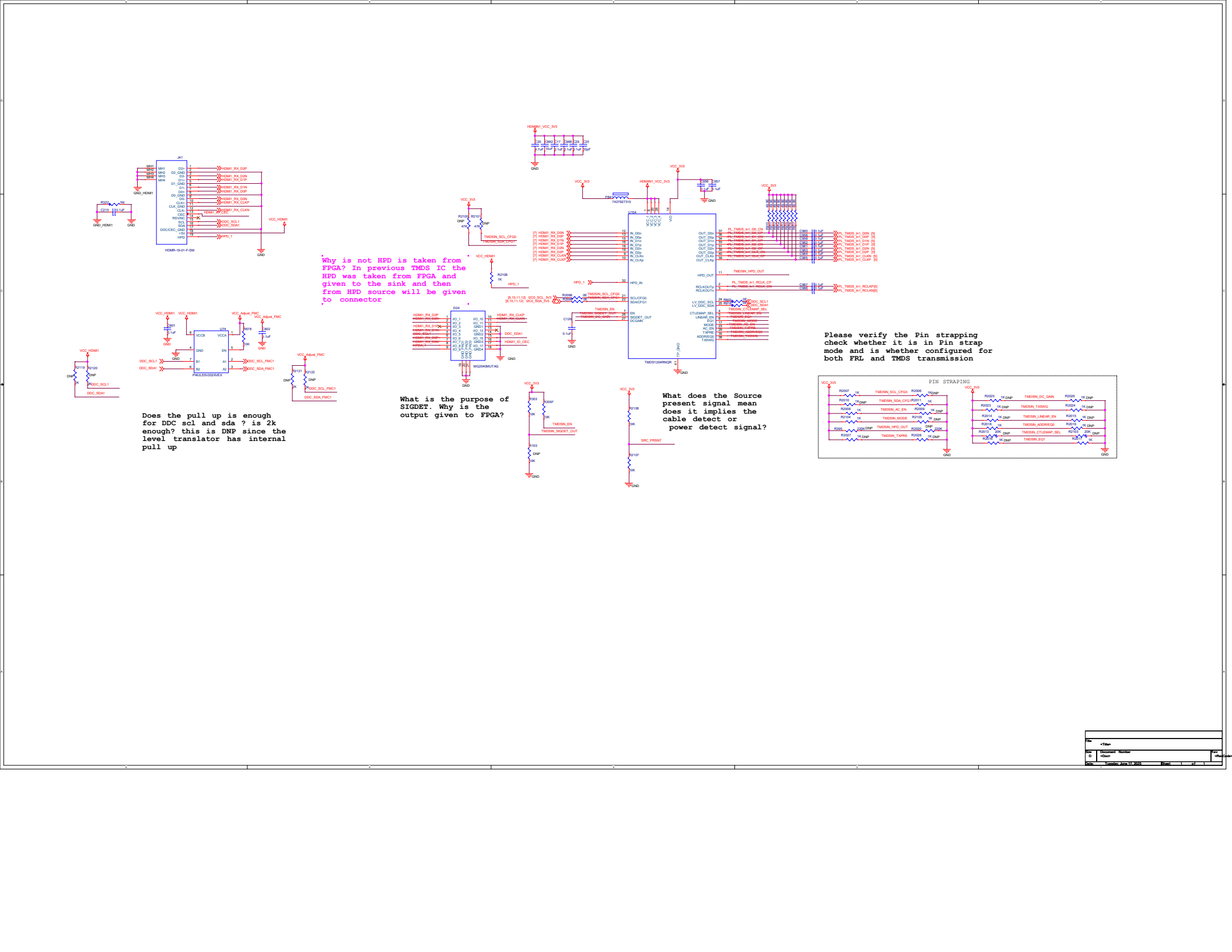
Why is not HPD is taken from FPGA? In previous TMDS IC the HPD was taken from FPGA and given to the sink and then from HPD source will be given to connector
Does the pull up is enough for DDC scl and sda ? is 2k enough? this is DNP since the level translator has internal pull up
What is the purpose of SIGDET. Why is the output given to FPGA?
What does the Source present signal mean does it implies the cable detect or power detect signal?
Please verify the Pin strapping check whether it is in Pin strap mode and is whether configured for both FRL and TMDS transmission
PIN STRAPING
HDMI-19-01-F-SM
PWULS5V202KIEX
MG2040MUT AG
TMDS1204RNQR
Title
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Size
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Document Number
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Rev
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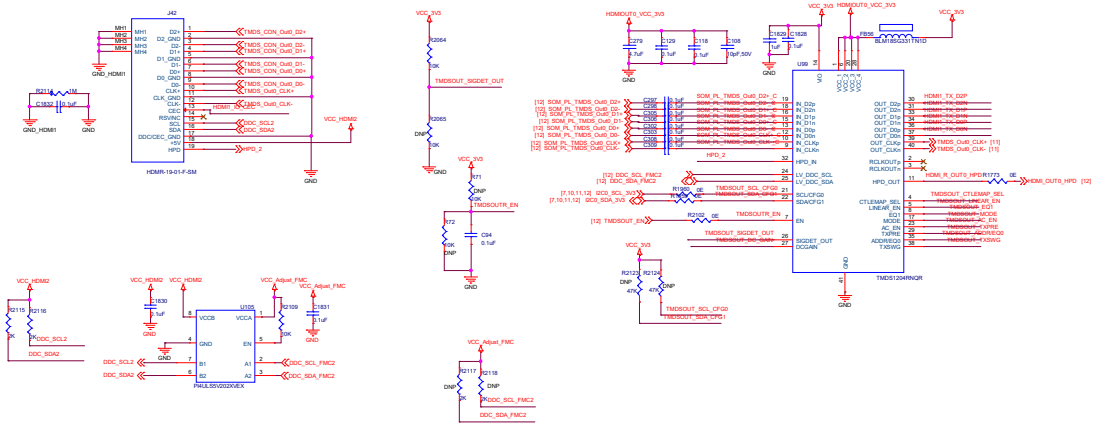
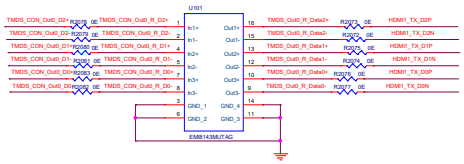
Date:
Tuesday, June 17, 2025
Sheet
1
of
1

Please verify this for the Source side application



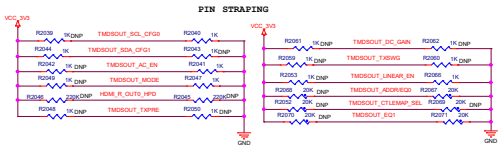
Note: The all the connection is for FMC HPC connector and the VADj FMC voltage is adjustable to 1.2V and 1.8V so the voltage is not mentioned

CMC WITH ESD PROTECTION



I2C Address: 1011101

PIN STRAPING



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Date: Tuesday, June 17, 2025	Sheet 1 of 1		