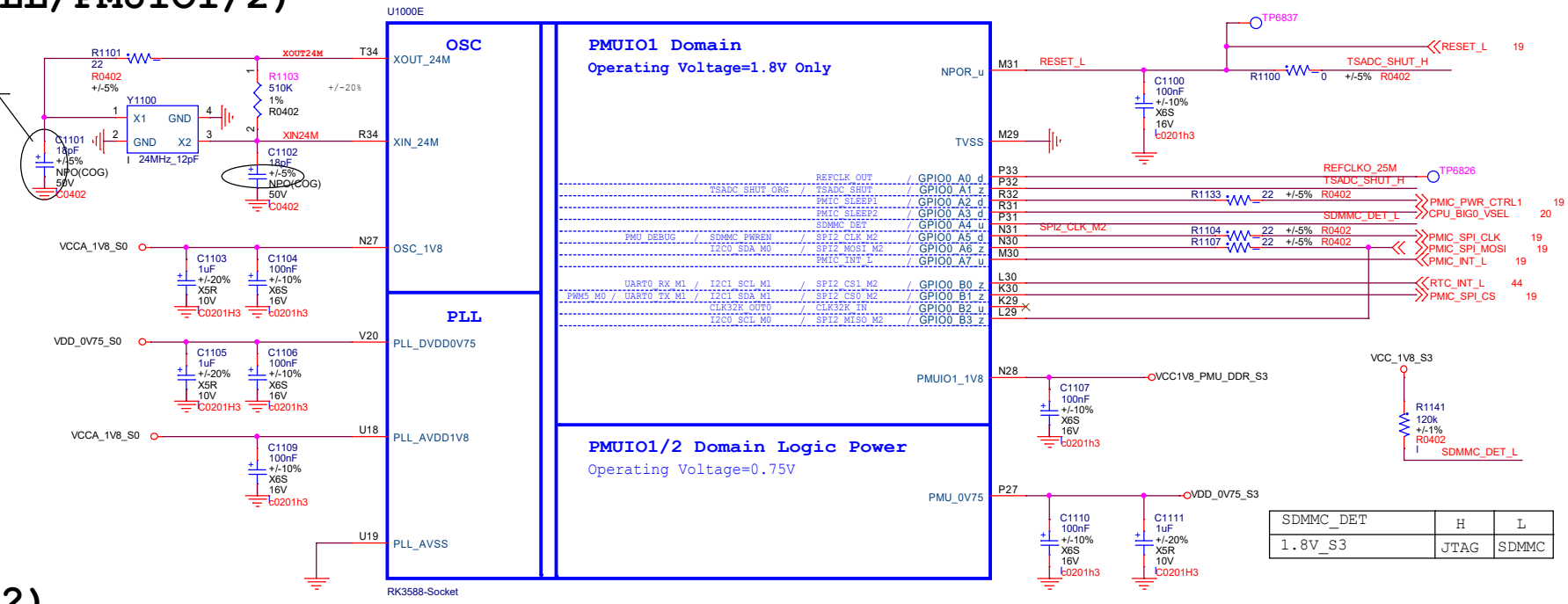
RK3588_E(OSC/PLL/PMUIO1/2)

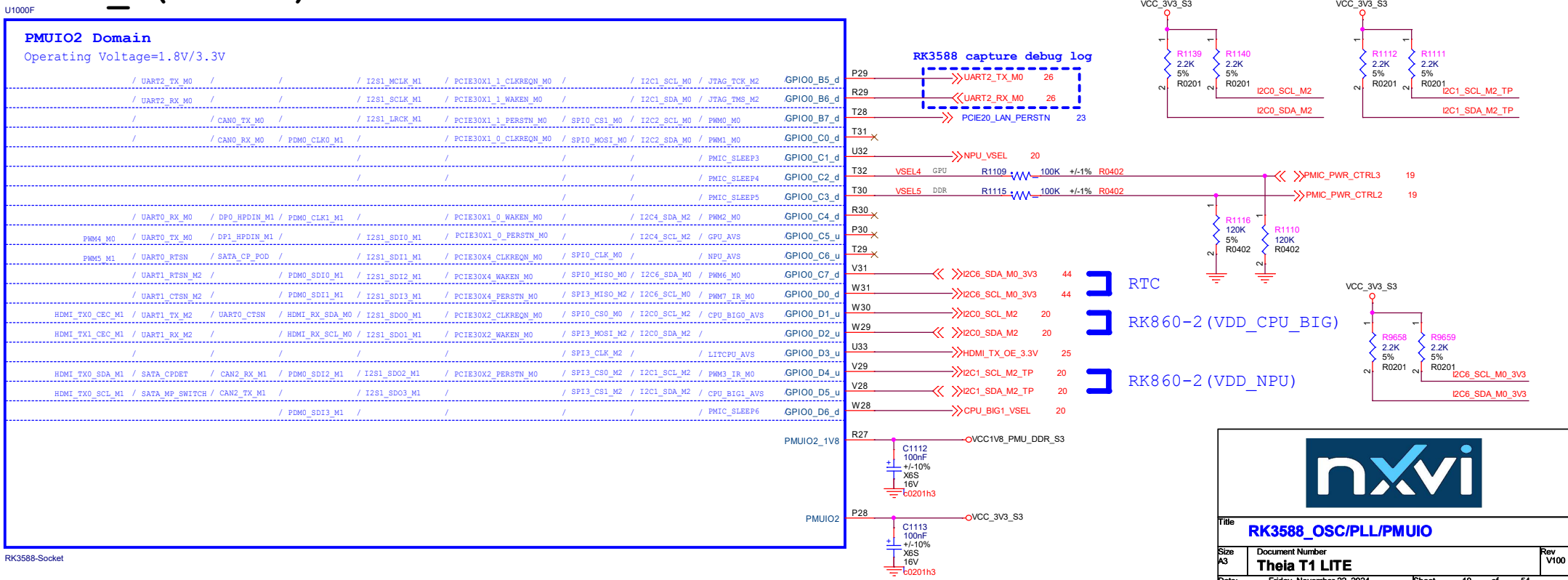
Note:
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<12pF



SDMMC_DET	H	L
1.8V_S3	JTAG	SDMMC

RK3588_F(PMUIO2)



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RK3588_S(HDMI2.1 TX)

U1000S

HDMI TX/eDP MUX Port0

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX0_SBDP/EDP_TX0_AUXP
HDMI_TX0_SBDN/EDP_TX0_AUXN
HDMI_TX0_D0P/EDP_TX0_D0P
HDMI_TX0_D0N/EDP_TX0_D0N
HDMI_TX0_D1P/EDP_TX0_D1P
HDMI_TX0_D1N/EDP_TX0_D1N
HDMI_TX0_D2P/EDP_TX0_D2P
HDMI_TX0_D2N/EDP_TX0_D2N
HDMI_TX0_D3P/EDP_TX0_D3P
HDMI_TX0_D3N/EDP_TX0_D3N
HDMI/EDP_TX0_REXT
HDMI/EDP_TX0_VDD_0V75
HDMI/EDP_TX0_AVDD_0V75
HDMI/EDP_TX0_VDD_IO_1V8
HDMI/EDP_TX0_VDD_CMN_1V8

HDMI TX/eDP MUX Port1

HDMI:V2.1 12Gbps
eDP: V1.3 5.4Gbps

HDMI_TX1_SBDP/EDP_TX1_AUXP
HDMI_TX1_SBDN/EDP_TX1_AUXN
HDMI_TX1_D0P/EDP_TX1_D0P
HDMI_TX1_D0N/EDP_TX1_D0N
HDMI_TX1_D1P/EDP_TX1_D1P
HDMI_TX1_D1N/EDP_TX1_D1N
HDMI_TX1_D2P/EDP_TX1_D2P
HDMI_TX1_D2N/EDP_TX1_D2N
HDMI_TX1_D3P/EDP_TX1_D3P
HDMI_TX1_D3N/EDP_TX1_D3N
HDMI/EDP_TX1_REXT
HDMI/EDP_TX1_VDD_0V75
HDMI/EDP_TX1_AVDD_0V75
HDMI/EDP_TX1_VDD_IO_1V8
HDMI/EDP_TX1_VDD_CMN_1V8

RK3588-Socket

RK3588_T(HDMI20 RX)

U1000T

HDMI RX

HDMI:V2.0

HDMI_RX_D0P
HDMI_RX_D0N
HDMI_RX_D1P
HDMI_RX_D1N
HDMI_RX_D2P
HDMI_RX_D2N
HDMI_RX_CLKP
HDMI_RX_CLKN
HDMI_RX_REXT
HDMI_RX_AVDD0V75
HDMI_RX_VPH3V3
HDMI_RX_DVDD3V3

RK3588-Socket

HDMI TX eARC

HDMI0_TX_SBDP_AUXP
HDMI0_TX_SBDN_AUXN
HDMI0_eARC+
HDMI0_eARC-

HDMI TX DDC

HDMI TX CEC

Note:

The controller only support AC coupled link In order to backward compatibility or to meet HDMI2.0 (1.4b) DC common mode spec and Voff, need do R based level-shift.

Switch on in HDMI2.0(TMDS) mode
Switch off in HDMI2.1(FRL) mode.

Cj<=0.2pF

Chassis GND

Type A Connector Pin Assignment

Pin	Signal Assignment	Pin	Signal Assignment
1	TMDS Data 2+	2	TMDS Data 2 shield
3	TMDS Data 2-	4	TMDS Data 1+
5	TMDS Data 1 shield	6	TMDS Data 1-
7	TMDS Data 0+	8	TMDS Data 0 shield
9	TMDS Data 0-	10	TMDS Clock+
11	TMDS Clock shield	12	TMDS Clock-
13	CEC	14	Utility/ HEAC+
15	SCL	16	SDA
17	DDC/CEC/HEAC GND	18	+5V Power
19	HPD/ HEAC-		

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RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

RK3588-Socket

VCC_1V8_S0

R9750 2.2K 5% R0201

R9751 2.2K 5% R0201

HDMI_CTL_SDA_1V8 25

HDMI_CTL_SCL_1V8 25

R9708 2.2K 5% R0201

R9709 2.2K 5% R0201

HDMI_SRC_SDA_1V8 25

HDMI_SRC_SCL_1V8 25

VCCIO5_1V8

VCCIO5

C1903 100nF +/-10% X6S 16V 0201h3

C1902 100nF +/-10% X6S 16V 0201h3

W26 VCCIO5 change to 1.8V

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

RK3588-Socket

GPIO_LED_G 44

GPIO_LED_R 44

GPIO_LED_B 44

M50A_PCEA_PERSTX 39

M50A_RSTX 38

HDMI1_TX_ON_H 16

HDMI_RX_HPDOUT_M0 25

HDMI_TX0_SCL_M0 16

HDMI_TX0_SDA_M0 16

HDMI_TX0_CEC_M0 16

VCCIO6_1V8

VCCIO6

VCC_1V8_S0

C1909 100nF +/-10% X6S 16V 0201h3

C1908 100nF +/-10% X6S 16V 0201h3

AC26 VCCIO6 change to 1.8V

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

RK3588-Socket

GPIO_FAN_POWER_CTL 45

HDMI_TX0_HPDIN_M0 16

HDMI_TX1_HPDIN_M0 25

FPGA_PCIE_PERST 29

R9722 2.2K 5% R0201

R9723 2.2K 5% R0201

HDMI_TX_SRC_SCL_RK3588 25

HDMI_TX_SRC_SDA_RK3588 25

VCCIO4_1V8

VCCIO4

VCC_1V8_S0

C1907 100nF +/-10% X6S 16V 0201h3

nxvi

Title	RK3588_1.8V/ 3.3V GPIO	
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8.3 Feature Description

8.3.1 4-Level Inputs

The TDP0604 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and place TDP0604 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There are internal pull-up and a pull-down resistors. These resistors are combined with the external resistor connection to achieve the desired voltage level.

Table 8-1. 4-Level Control Pin Settings

LEVEL	SETTINGS
0	Tie 1-kΩ 5% to GND.
R	Tie 20-kΩ 5% to GND.
F	Float (leave pin open)
1	Tie 1-kΩ 5% to V_{CC}.

MODE (Default set to I2C Mode)

Table 8-15. MODE Pin Function

MODE Pin Level	Description
0	Pin Strap with DDC Buffer enabled
R	Pin Strap with DDC Buffer disabled
F	I2C mode
1	Reserved

8.4.1 MODE Control

The MODE pin provides four modes of operation. There are three pin-strap modes and one I²C mode. In all three pin strap modes, DDC snooping feature is enabled. In I²C mode, DDC snoop feature is enabled by default but can be disabled by a register.

8.4.1.1 I²C Mode (MODE = "F")

In I²C mode, all settings of the TDP0604 can be controlled through the registers. The TDP0604 7-bit I2C address is determined by the ADDR/EQ0 pin. All other 4-level and 2-level pins are not used in I²C mode since the functions exist in a register. The SCL/CFG0 pin will function as the I²C clock and the SDA/CFG1 pin will function as the I²C data.

The TDP0604 defaults to power down in I²C mode. Upon completion of initialization of the TDP0604, software must clear the PD_EN field to exit the power down state. The HPD_OUT pin will be asserted low while the PD_EN register is set.

The TDP0604 supports 1.2-V, 1.8-V, and 3.3-V I²C signaling levels. Selection of 1.2-V, 1.8-V, or 3.3-V is determined by the VIO pin as provided in Table 8-2.

ADDR=0x10111100 / BC or 0x10111101 / BD

8.5.2 TDP0604 I²C Address Options

For further programmability, the TDP0604 can be controlled using I²C. The SCL/CFG0 and SDA/CFG1 terminals are used for I²C clock and I²C data respectively.

Table 8-18. TDP0604 I²C Device Address Description

ADDR/EQ0 pin	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)	HEX
0	1	0	1	1	1	1	0	0/1	BC/BD
R	1	0	1	1	1	0	1	0/1	BA/BB
F	1	0	1	1	1	0	0	0/1	B8/B9
1	1	0	1	1	0	1	1	0/1	B6/B7

EQ

8.3.8 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. TDP0604 supports fixed receiver equalizer by setting the EQ0 and EQ1 pins or through I²C register.

The TDP0604 has two sets of CTLE curves (3 Gbps CTLE and 6 Gbps CTLE) with each curve having 16 ac gain settings and 3 dc gain settings. The 16 ac gain settings with GLOBAL_DCG = 0x2 is detailed in Table 8-5.

The TDP0604 in pin-strap mode has two CTLE HDMI Datarate Maps: Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP_SEL pin as detailed in Table 8-7.

In the I²C mode, the default CTLE (3 Gbps or 6 Gbps) used for each HDMI mode can be controlled from a register.

Table 8-5. Receiver EQ Settings when GLOBAL_DCG = 0x2

EQ Setting(1)	RX EQ Level for 3Gbps CTLE (Gain at 1.5 GHz - Gain at 10 MHz)	RX EQ Level for 6Gbps CTLE (Gain at 3 GHz - Gain at 10 MHz)	EQ1 PIN	EQ0 PIN
0(2)	1.0	0.5	0	0
1	2.0	1.0	0	R
2	3.2	2.4	0	F
3	4.2	3.3	0	1
4	5.3	4.4	R	0
5	6.0	5.2	R	R
6	7.0	6.0	R	F
7	7.7	6.8	R	1
8	9.0	7.5	F	0
9	9.5	8.2	F	R
10	10.0	8.8	F	F
11	10.5	9.3	F	1
12	11.0	10.0	1	0
13	11.5	10.5	1	R
14	12.0	11.0	1	F
15	12.3	11.8	1	1

(1) In I2C mode, the receiver EQ setting is determined by D0_EQ_D1_EQ, and D2_EQ registers.
(2) When CTLEBYP_EN = 1 and dcGAIN = 0-dB, EQ settings 0 will be 0-dB due to the CTLE is bypassed.

LINEAR_EN

Table 8-4. Pin-Strap Mode LINEAR_EN Pin Function

LINEAR_EN Pin Level	Description
1	Limited Enabled
F	Linear Enabled. Recommended for HDMI sink application.
R	Reserved
0	Limited Enabled. Recommended for HDMI source application

AC_EN (Default set to AC coupled)

8.3.11 Main Link Outputs

8.3.11.1 Transmitter Bias

The TDP0604 transmitter supports both external (DC-coupled) and internal bias (AC-coupled) to a receiver. Selection between DC and AC-coupled is done through use of the AC_EN pin in pin-strap mode and TX_AC_EN register in I²C mode. The AC_EN pin informs the TDP0604 whether or not an external AC-coupling capacitor is present. When AC_EN is greater than VIH, then TDP0604 transmitters are internally biased to approximately V_{CC}. For AC-coupled application, the AC_EN pin should be connected to greater than VIH and an external AC-coupling capacitor should be placed on each of the OUT_D[2:0] pins and the OUT_CLK pin. If the AC_EN pin is connected to less than VIL, then the AC_EN pin will inform TDP0604 that AC_EN pin is DC-coupled (externally biased) to the far-end HDMI compliant receiver.

HPDOUT_SEL

HPDOUT_SEL	2	I 2-Level (FD)	HPDOUT_SEL Selects whether HPD_OUT pin is push/pull, or open-drain. Open-drain is not supported in pin-strap mode. Therefore this pin should be left floating or pull-down to GND.

CTLEMAP_SEL

The TDP0604 in pin-strap mode has two CTLE HDMI Datarate Maps: Map B and Map C. These maps are detailed in Table 8-6. The expectation is Map B or C should be used if TDP0604 is used in a source application and Map B for a sink application.

When the TDP0604 is configured for pin-strap mode, the default CTLE HDMI data rate map will be determined by the sampled state of the CTLEMAP_SEL pin as detailed in Table 8-7.

Table 8-6. CTLE HDMI Datarate Map B and C

HDMI Mode	Map B	Map C
1.4	3 Gbps CTLE	6 Gbps CTLE
2.0	6 Gbps CTLE	6 Gbps CTLE

Table 8-7. Pin-Strap Mode CTLE HDMI Datarate Mapping

	Sampled State of CTLEMAP_SEL Pin			
	"0"	"R"	"F"	"1"
CTLE HDMI Datarate Map	Reserved	Map C	Reserved	Map B

Note

The clock lane EQ when operating in HDMI 1.4 or 2.0 will use the 3-Gbps CTLE and will be set to the zero EQ setting.

TXPRE

8.3.11.4 TX Pre-Emphasis and De-Emphasis Control

The TDP0604 provides pre-emphasis and de-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TDP0604 outputs and a TMDS receiver. Pre-emphasis and de-emphasis is not implemented on the clock lane. There are two methods to implement pre-emphasis, pin strapping or through I²C programming. TX pre-emphasis and de-emphasis control is only supported in limited mode.

When using pin strap mode, the TXPRE pin controls four different global pre-emphasis and de-emphasis values for all data lanes when TDP0604 is operating in HDMI 1.4 or HDMI 2.0. These pre-emphasis and de-emphasis values are described in Table 8-11.

Table 8-11. Pin-Strap TXPRE Pin Function

TXPRE Pin	HDMI 1.4 or HDMI 2.0
0	3.5 dB pre-emphasis
R	-2.5 dB de-emphasis
F	0 dB
1	6.0 dB pre-emphasis

TXSWG

8.3.11.5 TX Swing Control

The TDP0604 transmitter swing level can be adjusted in both pin strap and I²C mode. In I²C mode, TX swing settings are controlled independently for each lane (both clock and data) through registers.

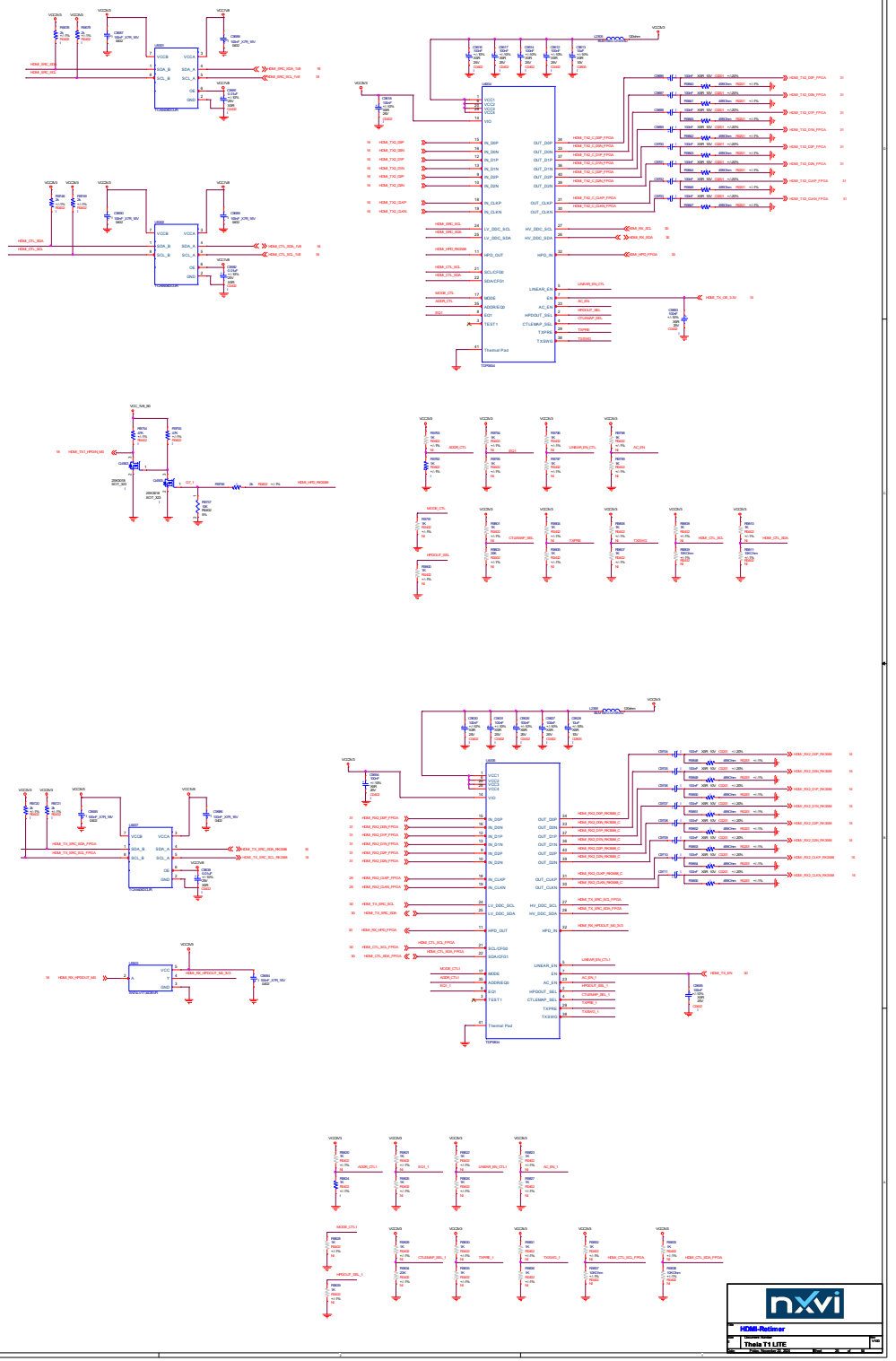
In I2C mode, the TX swing used when operating in HDMI 1.4 and HDMI 2.0 can be independently controlled through HDMI14_VOD and HDMI20_VOD registers.

In pin strap mode with limited enabled, the TXSWG pin adjusts the default 1000 mV swing as detailed in Table 8-12. In HDMI 1.4 the TXSWG pin controls the swing for both the data and clock lanes. In HDMI 2.0, the TXSWG pin controls the swing for data lanes while the clock lane will remain at default value.

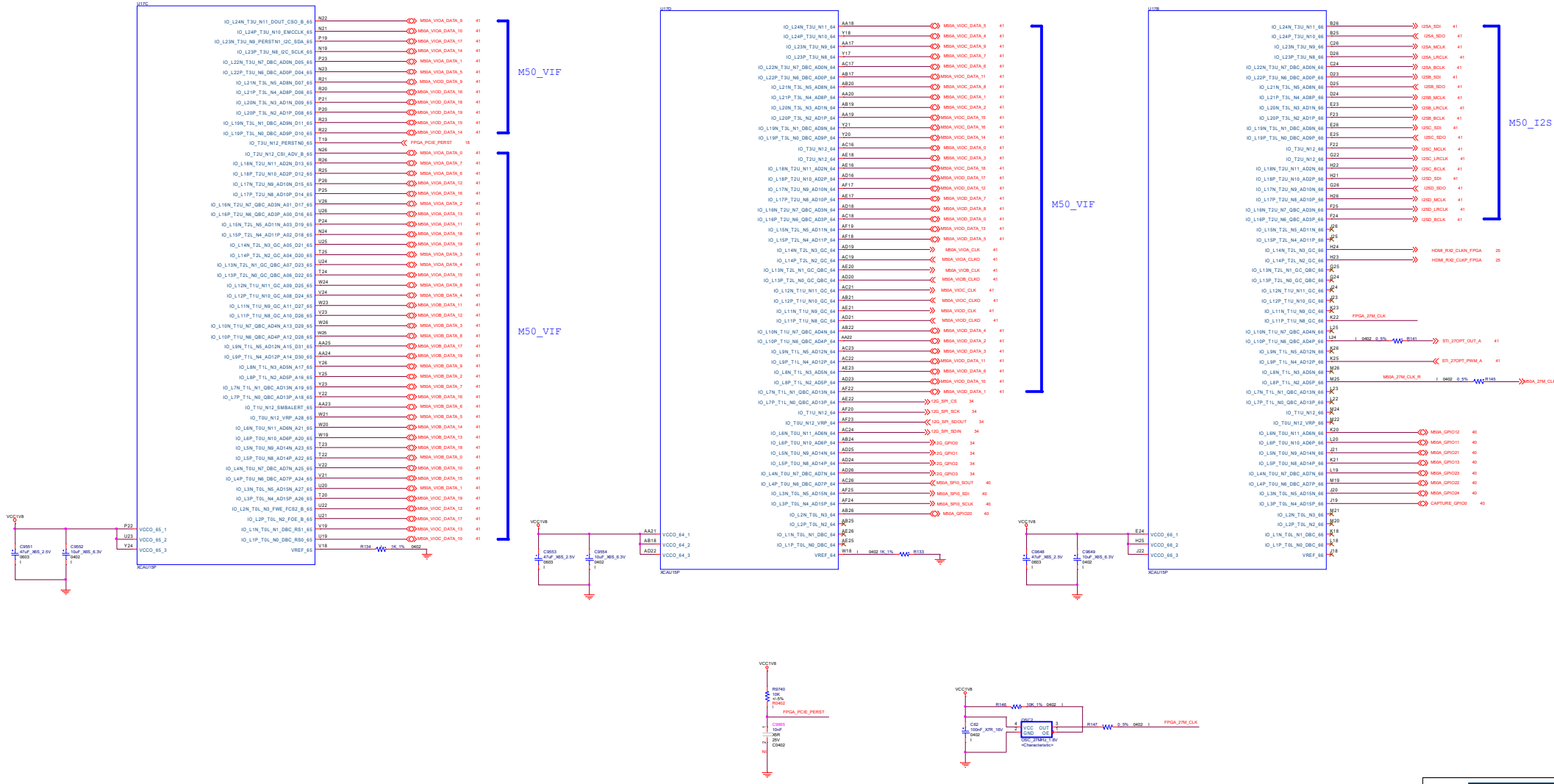
In pin-strap mode with linear enabled, the linearity range is fixed at the highest level (1200 mVpp) and therefore TXSWG pin is not used. In I²C mode, the linearity range can be adjusted from a register.

Table 8-12. Pin Strap TXSWG Control

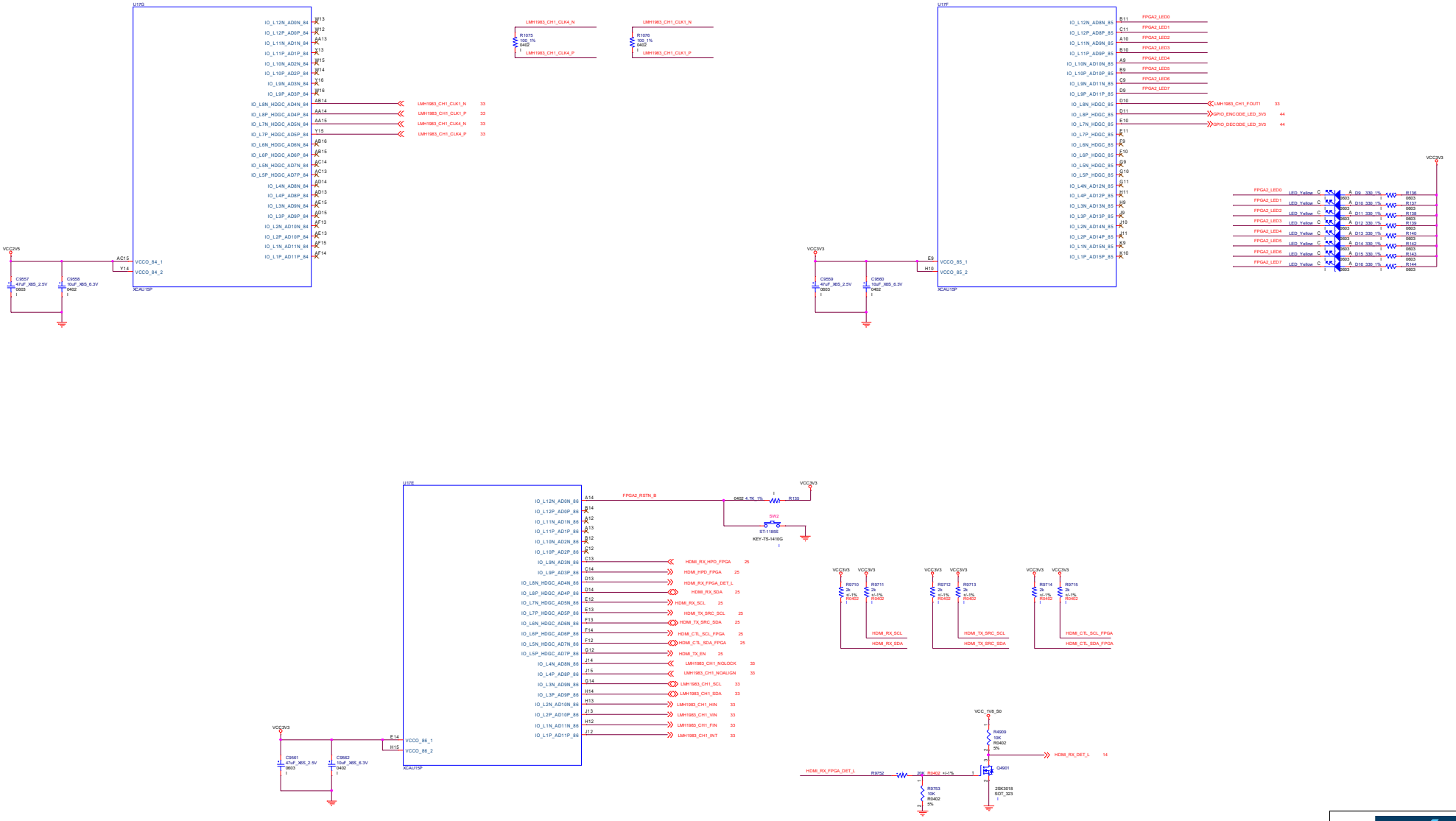
TXSWG pin	Limited Mode for HDMI 1.4	Limited Mode for HDMI 2.0	Linear Mode
0	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
R	Default - 5%	Default - 5%	1200 mVpp
F	Default (1000 mVpp)	Default (1000 mVpp)	1200 mVpp
1	Default (1000 mVpp)	Default + 5%	1200 mVpp



HP BANKS (1V~1.8V)



HD BANKS (1V~3.3V)



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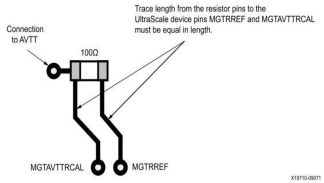
GTY Transceivers



U17H

XCAU15P

MGTRREF_R	AD9	R148 100_1%_0402	MGTAVTT_FPGA2	
MGTAVTTRCAL_R	AD8			
MGTHRXN0_224	AF1		PCIE30_FPGA_TX0N	17
MGTHRXN1_224	AE3		PCIE30_FPGA_TX1N	17
MGTHRXN2_224	AD1			
MGTHRXN3_224	AB1			
MGTHRXP0_224	AF2		PCIE30_FPGA_TX0P	17
MGTHRXP1_224	AE4		PCIE30_FPGA_TX1P	17
MGTHRXP2_224	AD2			
MGTHRXP3_224	AB2			
MGTHTXN0_224	AF6	C0201 10V X5R 220nF C65	PCIE30_FPGA_RX0N	17
MGTHTXN1_224	AE8	C0201 10V X5R 220nF C9675	PCIE30_FPGA_RX1N	17
MGTHTXN2_224	AD6			
MGTHTXN3_224	AC4			
MGTHTXP0_224	AF7	C0201 10V X5R 220nF C9650	PCIE30_FPGA_RX0P	17
MGTHTXP1_224	AE9	C0201 10V X5R 220nF C9676	PCIE30_FPGA_RX1P	17
MGTHTXP2_224	AD7			
MGTHTXP3_224	AC5			
MGTREFCLK0N_224	AB6		PCIE30_REFCLKN_FPGA	27
MGTREFCLK0P_224	AB7		PCIE30_REFCLKP_FPGA	27
MGTREFCLK1N_224	Y6			
MGTREFCLK1P_224	Y7			

To RK3588

U17J

XCAU15P

MGTHRXN0_226	M1	12G_RX0_N	34
MGTHRXN1_226	K1		
MGTHRXN2_226	H1		
MGTHRXN3_226	F1		
MGTHRXP0_226	M2	12G_RX0_P	34
MGTHRXP1_226	K2		
MGTHRXP2_226	H2		
MGTHRXP3_226	F2		
MGTHTXN0_226	N4	12G_TX0_N	34
MGTHTXN1_226	L4		
MGTHTXN2_226	J4		
MGTHTXN3_226	G4		
MGTHTXP0_226	N5	12G_TX0_P	34
MGTHTXP1_226	L5		
MGTHTXP2_226	J5		
MGTHTXP3_226	G5		
MGTREFCLK0N_226	P6	LMH1983_CH1_CLK2_N	33
MGTREFCLK0P_226	P7	LMH1983_CH1_CLK2_P	33
MGTREFCLK1N_226	M6	LMH1983_CH1_CLK3_N	33
MGTREFCLK1P_226	M7	LMH1983_CH1_CLK3_P	33

U17I

XCAU15P

MGTHRXN0_225	Y1		HDMI_TX2_D0N_FPGA	25
MGTHRXN1_225	V1		HDMI_TX2_D1N_FPGA	25
MGTHRXN2_225	T1		HDMI_TX2_D2N_FPGA	25
MGTHRXN3_225	P1			
MGTHRXP0_225	Y2		HDMI_TX2_D0P_FPGA	25
MGTHRXP1_225	V2		HDMI_TX2_D1P_FPGA	25
MGTHRXP2_225	T2		HDMI_TX2_D2P_FPGA	25
MGTHRXP3_225	P2			
MGTHTXN0_225	AA4	+/-20% C0201 10V X5R 100nF C9604	HDMI_RX2_D0N_FPGA	25
MGTHTXN1_225	W4	+/-20% C0201 10V X5R 100nF C9605	HDMI_RX2_D1N_FPGA	25
MGTHTXN2_225	U4	+/-20% C0201 10V X5R 100nF C9606	HDMI_RX2_D2N_FPGA	25
MGTHTXN3_225	R4			
MGTHTXP0_225	AA5	+/-20% C0201 10V X5R 100nF C9607	HDMI_RX2_D0P_FPGA	25
MGTHTXP1_225	W5	+/-20% C0201 10V X5R 100nF C9608	HDMI_RX2_D1P_FPGA	25
MGTHTXP2_225	U5	+/-20% C0201 10V X5R 100nF C9609	HDMI_RX2_D2P_FPGA	25
MGTHTXP3_225	R5			
MGTREFCLK0N_225	V6		HDMI_TX2_CLKN_FPGA	25
MGTREFCLK0P_225	V7		HDMI_TX2_CLKP_FPGA	25
MGTREFCLK1N_225	T6			
MGTREFCLK1P_225	T7			

To RK3588 HDMI

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