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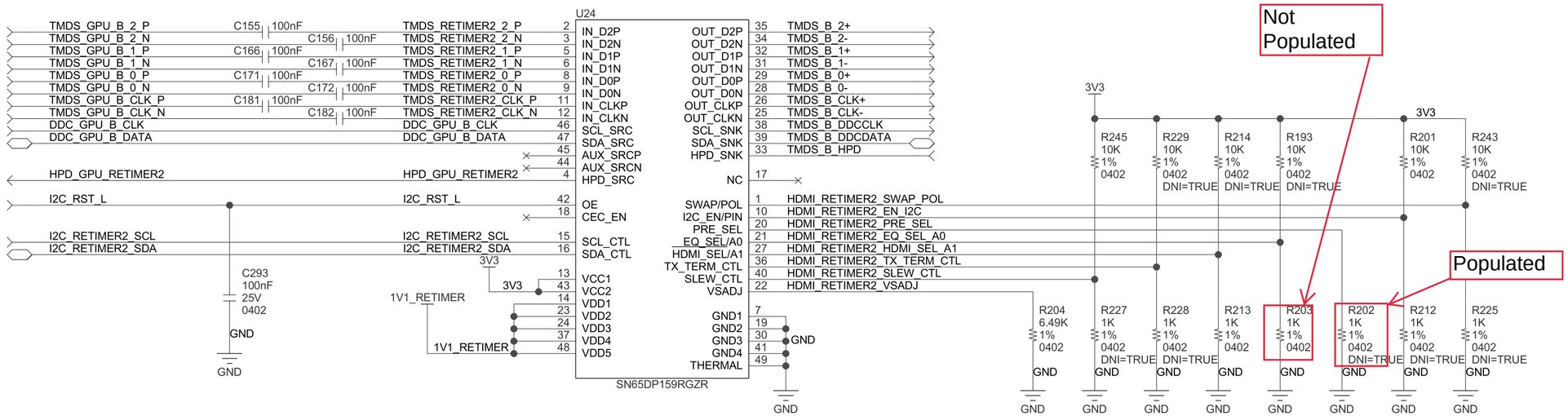
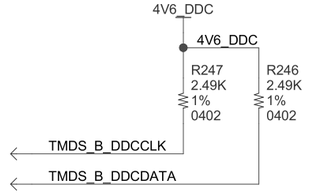
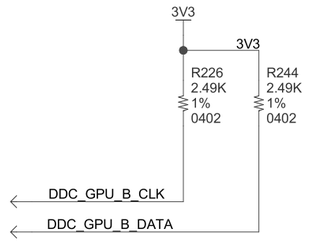
I2C Address - 0x5E
I2C Address (7bit) - 101 1110b



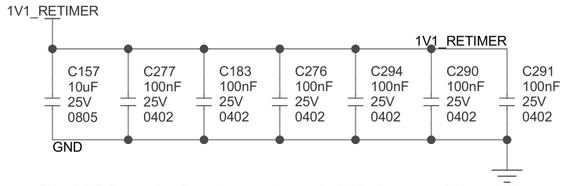
Sink DDC Terminations



Source DDC Terminations

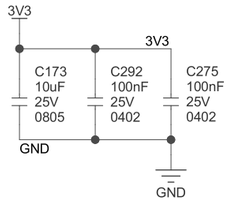


VDD Decoupling Capacitors



Place VDD Decoupling Capacitors as close to the VDD pins as possible.

VCC Decoupling Capacitors



Place VCC Decoupling Capacitors as close to the VCC pins as possible.

SN65DP159RGZR PIN STRAPS:

INPUT LANE SWAP & POLARITY CONTROL PIN STRAP WHEN I2C_EN_PIN = LOW:
SWAP/POL= H : RECEIVE LANE POLARITY SWAP (RETIMER MODE ONLY)
SWAP/POL= L : RECEIVE LANES SWAP (RETIMER AND REDRIVER MODE)
SWAP/POL= NC : NORMAL OPERATION

I2C_EN/PIN STRAP:
I2C_EN/PIN = H: PUTS THE DEVICE INTO I2C CONTROL MODE
I2C_EN/PIN = L: PUTS THE DEVICE INTO PIN STRAP MODE

DE-EMPHASIS PIN STRAP WHEN I2C_EN/PIN = LOW:
PRE_SEL = L: - 2 dB DE-EMPHASIS
PRE_SEL = NC: 0 dB
PRE_SEL = H: RESERVED

HDMI_SEL/A1 PIN STRAP WHEN I2C_EN/PIN = LOW:
HDMI_SEL/A1 = H : DEVICE CONFIGURED FOR DVI
HDMI_SEL/A1 = L : DEVICE CONFIGURED FOR HDMI
WHEN I2C_EN/PIN = HIGH THIS PIN IS ADDRESS bit 2

INPUT RECEIVE EQUALIZATION PIN STRAP WHEN I2C_EN/PIN = LOW:
EQ_SEL = L: FIXED EQ at 7.5 dB
EQ_SEL = NC: ADAPTIVE EQ
EQ_SEL = H: FIXED at 14 dB
When I2C_EN/PIN = HIGH THIS PIN IS ADDRESS bit 1
Note: (3 level for pin strap programming but 2 level when I2C address)

TRANSMIT TERMINATION CONTROL PIN STRAP WHEN I2C_EN/PIN = LOW:
TX_TERM_CTL = H : NO TRANSMIT TERMINATION
TX_TERM_CTL = L : TRANSMIT TERMINATION IMPEDANCE IN 75 O to ABOUT 150 O
TX_TERM_CTL = NC : AUTOMATICALLY SELECTS THE TERMINATION IMPEDANCE

SLEW RATE CONTROL PIN STRAP WHEN I2C_EN/PIN = LOW:
SLEW_CTL = H : FASTEST DATA RATE
SLEW_CTL = L : 5 ps SLOW
SLEW_CTL = NC : 10 ps SLOW

HDMI RETIMER 2

SIZE	CAGE CODE	DWG NO	REV
B	6GSC8	10000841	A
SCALE NONE		SHEET 50 OF 60	