How to utilize diagnostic test suite of Ethernet PHY

Oct. 2022

Gerome Cacho

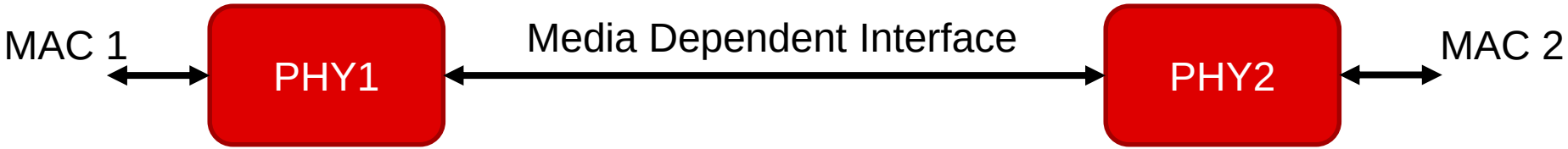
Checking link’s health with Packet Generator/Checker

What is PRBS Packet Generation and Checking?

- What is it?
  - Pseudo-Random Bit Sequence (PRBS) Built-in Self Test (BIST) is a way to test PHY's internal and on-board data path
  - Self-sufficient with no dependency on MAC or external data generator
- What is needed?
  - 2x Ethernet PHY boards
  - 1x Cable
- For this presentation, DP83867 will be utilized, but these features are available on several of our Ethernet PHYs
  - Note: The registers may be in a different address depending on the PHY. It is important to confirm locations in the datasheet prior to operation

Using PRBS Generating and Checking

- PRBS consists of a self-generated sequence which is transmitted from PHY out to its link partner (LP) on MDI cable
  - Note: On many of TI PHYs PRBS packets can also be generated directly towards MAC side

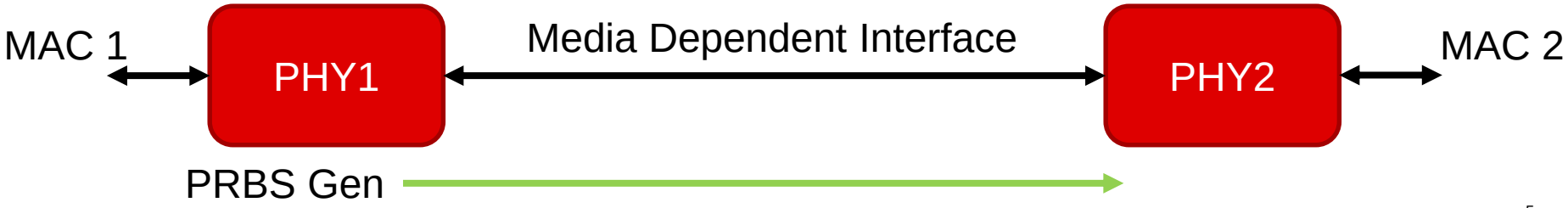


Using PRBS Generating and Checking

- In this example, we configure PHY1, a DP83867 device, into continuous PRBS generation mode
  - For PHY1, we program Reg 0x16 = 0xD000

Table 30. BIST Control Register (BISCR), Address 0x0016

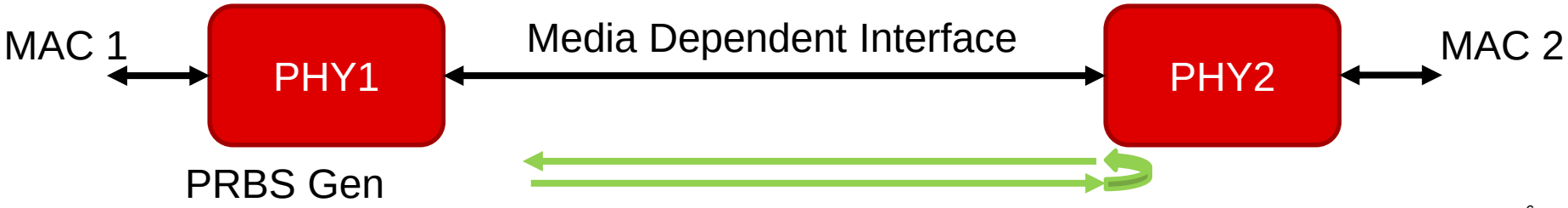
BIT	BIT NAME	DEFAULT	DESCRIPTION
15	PRBS_COUNT_MODE	0, RW	PRBS Continuous Mode: 1 = Continuous mode enabled. When one of the PRBS counters reaches the maximum value, a pulse is generated and the counter starts counting from zero again. This bit must be set for proper PRBS operation. 0 = PRBS continuous mode disabled. PRBS operation is not supported for this setting.
14	GEN_PRBS_PACKET	0, RW	Generated PRBS Packets: 1 = When the packet generator is enabled, it will generate continuous packets with PRBS data. When the packet generator is disabled, the PRBS checker is still enabled. 0 = When the packet generator is enabled, it will generate a single packet with constant data. PRBS generation and checking is disabled.
13	PACKET_GEN_64BIT_MODE	0, RW	BIST Packet Size: 1 = Transmit 64 byte packets in packet generation mode. 0 = Transmit 1518 byte packets in packet generation mode
12	PACKET_GEN_EN	0, RW	Packet BIST Enable: 1 = Enable packet/PRBS generator 0 = Disable packet/PRBS generator



Using PRBS Generating and Checking

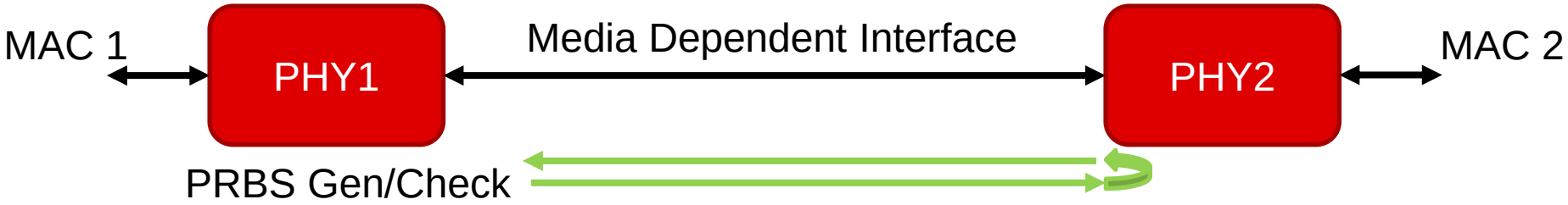
- The pattern should be rerouted (or “looped back”) to PHY1 somehow
  - For data on the MDI, enable **Reverse Loopback**
  - In this example, PHY2 is another instance of DP83867. We set Reg 0x16[5] = ‘1’

5:2	LOOPBACK_MODE	0, RW	Loopback Mode Select: PCS Loopback must be disabled (Bits [1:0] =00) prior to selecting the loopback mode. 1000: Reverse loop 0100: External loop 0010: Analog loop 0001: Digital loop



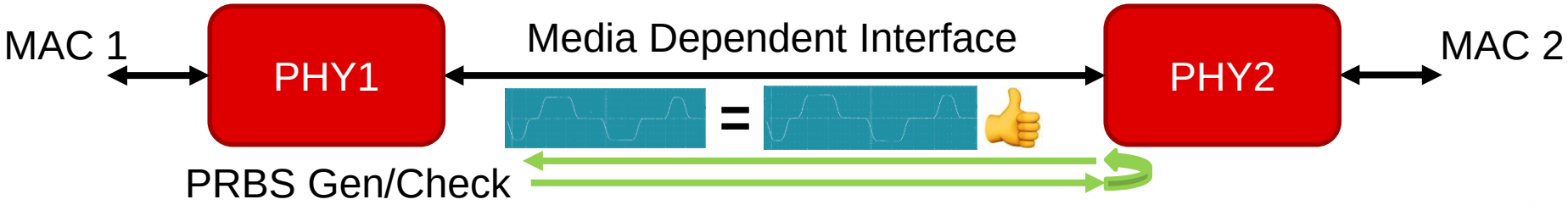
Using PRBS Generating and Checking

- A checker then checks the incoming sequence against the generated sequence
  - Depending on PHY, the checker may be set automatically along with generator, or it can be set separately



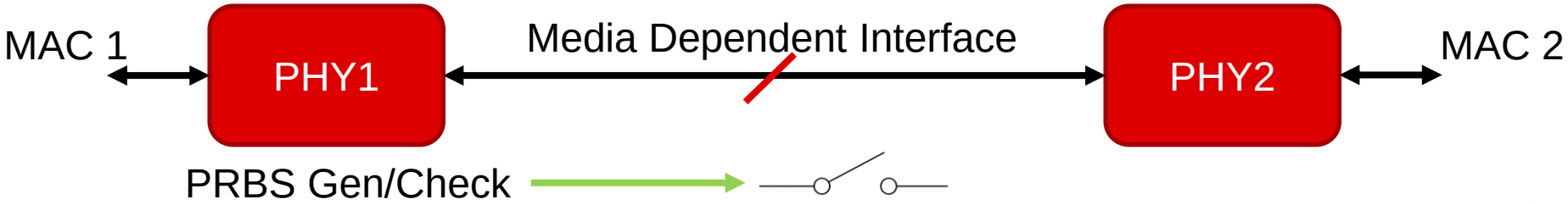
Using PRBS Generating and Checking

- Assuming clean data transmission, both the generated and received (checked) packets will be the same



Using PRBS Generating and Checking

- However, if data is corrupted or no data is received, this would indicate an issue on the signal chain that needs to be addressed
  - Here, there is a break in the MDI. Data cannot reach PHY2 and subsequently cannot be looped back to PHY1

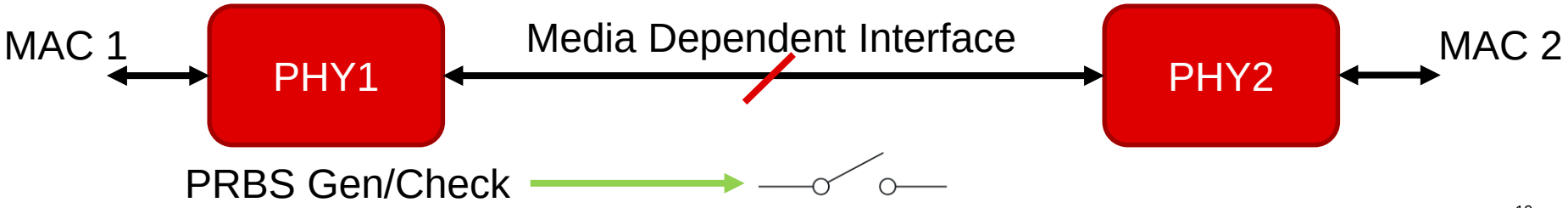


Using PRBS Generating and Checking

- There are registers that determine if the checker has received any bytes
  - This is good to validate the functionality of an interface; if there is an open somewhere completely preventing packets from reaching their destination

Table 50. BIST Control and Status Register 1 (BICSR1), Address 0x0071

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PRBS_BYTE_CNT	0x0000, RO	Holds the number of total bytes received by the PRBS checker. Value in this register is locked when write is done to register BICSR2 bit[0] or bit[1]. The count stops at 0xFFFF when PRBS_COUNT_MODE in BISCR register (0x0016) is set to 0.

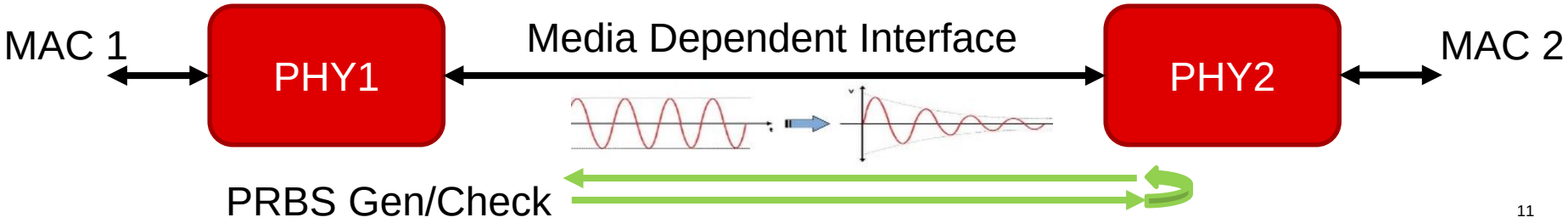


Using PRBS Generating and Checking

- There are also registers that can determine if the received bytes have been corrupted
  - After confirming there are no opens present, this confirms that the pathway is not attenuating or distorting the signal too much

Table 51. BIST Control and Status Register 2 (BICSR2), Address 0x0072

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	Reserved	0x00, RO	Ignored on Read
10	PRBS_PKT_CNT_OVF	0, RO	PRBS Checker Packet Count Overflow If set, PRBS Packet counter has reached overflow. Overflow is cleared when PRBS counters are cleared by setting bit #1 of this register.
9	PRBS_BYTE_CNT_OVF	0, RO	PRBS Byte Count Overflow If set, PRBS Byte counter has reached overflow. Overflow is cleared when PRBS counters are cleared by setting bit #1 of this register.
8	Reserved	0,RO	Ignore on Read
7:0	PRBS_ERR_CNT	0x00, RO	Holds number of error bytes that are received by PRBS checker. Value in this register is locked when write is done to bit[0] or bit[1] When PRBS Count Mode set to zero, count stops on 0xFF (see register 0x0016) Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters



Using registers to analyze PRBS results

- To analyze results from PRBS, it is important to latch the checker's output to the register
  - In DP83867, this is done setting Register 0x72 = 0x1
  - Once written, the values of the checker will be latched onto appropriate registers
    - In DP83867, Reg 0x71 can be used to check if packets are being received
    - Reg 0x72 can identify when the received packets are corrupted

Table 50. BIST Control and Status Register 1 (BICSR1), Address 0x0071

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:0	PRBS_BYTE_CNT	0x0000, RO	Holds the number of total bytes received by the PRBS checker. Value in this register is locked when write is done to register BICSR2 bit[0] or bit[1]. The count stops at 0xFFFF when PRBS_COUNT_MODE in BISCR register (0x0016) is set to 0.

Table 51. BIST Control and Status Register 2 (BICSR2), Address 0x0072

BIT	BIT NAME	DEFAULT	DESCRIPTION
15:11	Reserved	0x00, RO	Ignored on Read
10	PRBS_PKT_CNT_OVF	0, RO	PRBS Checker Packet Count Overflow If set, PRBS Packet counter has reached overflow. Overflow is cleared when PRBS counters are cleared by setting bit #1 of this register.
9	PRBS_BYTE_CNT_OVF	0, RO	PRBS Byte Count Overflow If set, PRBS Byte counter has reached overflow. Overflow is cleared when PRBS counters are cleared by setting bit #1 of this register.
8	Reserved	0,RO	Ignore on Read
7:0	PRBS_ERR_CNT	0x00, RO	Holds number of error bytes that are received by PRBS checker. Value in this register is locked when write is done to bit[0] or bit[1] When PRBS Count Mode set to zero, count stops on 0xFF (see register 0x0016) Notes: Writing bit 0 generates a lock signal for the PRBS counters. Writing bit 1 generates a lock and clear signal for the PRBS counters

Checking link’s health with PHY’s SNR output

How can I use SNR to determine link health?

- Our PHY can obtain the Mean Squared Error to determine
- In DP83867, we give indicators for MSE (Mean Square Error) per channel
  - For Channel A, register 0x225
  - For Channel B, register 0x265
  - For Channel C, register 0x2A5
  - For Channel D, register 0x2E5
- Once the value is read in one of these registers, input the decimal equivalent into this equation to obtain SNR:

$$SNR = -10log_{10}\left(\frac{MSE}{2^{17}}\right) - 3$$

- Once obtained, the SNR can be categorized to the following:

Poor link quality = SNR < 19 Good link quality = 19 < SNR < 21 Excellent link quality = SNR > 21