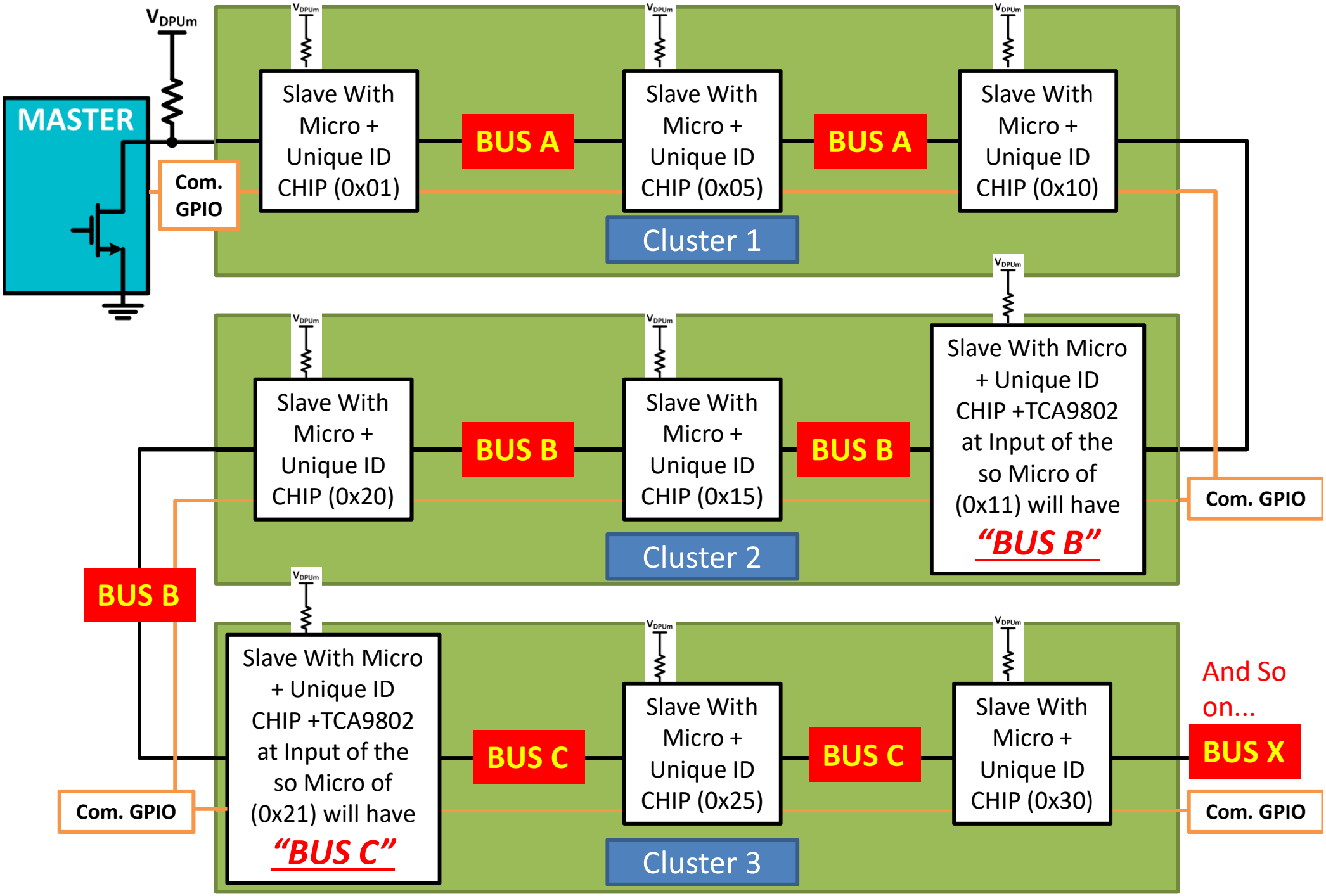
MASTER
V_{DPUm}
Com. GPIO
Slave With Micro + Unique ID CHIP (0x01)
BUS A
Slave With Micro + Unique ID CHIP (0x05)
BUS A
Slave With Micro + Unique ID CHIP (0x10)
Cluster 1
Slave With Micro + Unique ID CHIP (0x20)
BUS B
Slave With Micro + Unique ID CHIP (0x15)
BUS B
Slave With Micro + Unique ID CHIP +TCA9802 at Input of the so Micro of (0x11) will have "BUS B"
Com. GPIO
Cluster 2
BUS B
Slave With Micro + Unique ID CHIP +TCA9802 at Input of the so Micro of (0x21) will have "BUS C"
BUS C
Slave With Micro + Unique ID CHIP (0x25)
BUS C
Slave With Micro + Unique ID CHIP (0x30)
And So on...
BUS X
Com. GPIO
Com. GPIO
Cluster 3