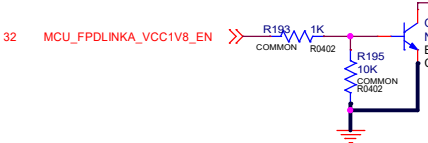


Display-DSI To FPD-LINK III A

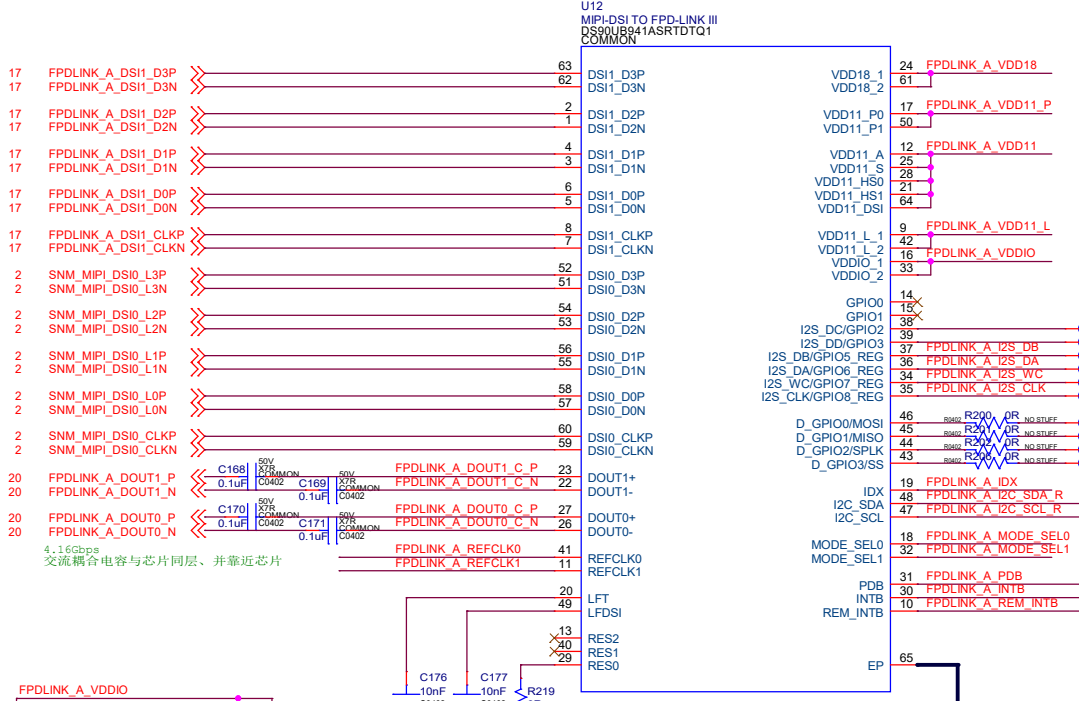
FPD-LINK A VCC1V8 PWR

FPD-LINK A VCC1V8供电由核心板控制

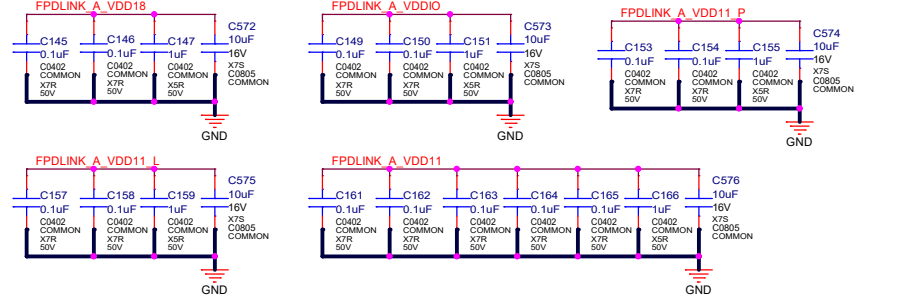


FPD-LINK A VCC1V1 PWR

FPD-LINK A VCC1V1供电由核心板控制



0.1uF去耦电容靠近供电引脚布局



I2C Addr : 7bit 0x0C ; 8bit 0x18

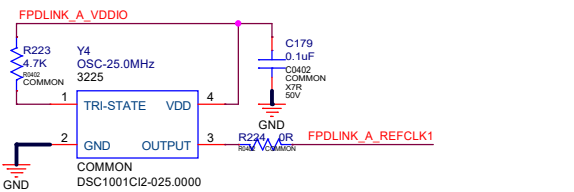
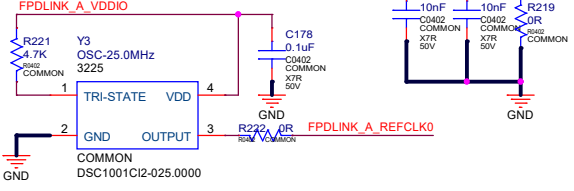


表 8-9 Strap 配置 MODE_SEL0

MODE 编号	Vdd 电压	Vdd 目标电压	建议的 STRAP 配置电阻器 (1% TOL)	SPLITTER	DSI LINES			
	Vmin	Vtyp	Vmax					
0	0	0	0.126 * V _{DDIO}	前开	10.0	0	1	
1	0.179 * V _{DDIO}	0.211 * V _{DDIO}	0.244 * V _{DDIO}	0.380	73.2	20.0	0	2
2	0.286 * V _{DDIO}	0.325 * V _{DDIO}	0.364 * V _{DDIO}	0.585	60.4	30.1	0	3
3	0.404 * V _{DDIO}	0.441 * V _{DDIO}	0.472 * V _{DDIO}	0.794	51.1	40.2	0	4
4	0.526 * V _{DDIO}	0.556 * V _{DDIO}	0.590 * V _{DDIO}	1.001	40.2	51.1	1	1
5	0.643 * V _{DDIO}	0.673 * V _{DDIO}	0.708 * V _{DDIO}	1.211	30.1	61.9	1	2
6	0.763 * V _{DDIO}	0.790 * V _{DDIO}	0.825 * V _{DDIO}	1.421	18.7	71.5	1	3
7	0.880 * V _{DDIO}	V _{DDIO}	V _{DDIO}	1.8	10.0	前开	0	1

表 8-10 Strap 配置 MODE_SEL1

MODE 编号	Vdd 电压	Vdd 目标电压	建议的 STRAP 配置电阻器 (1% TOL)	CLOCK	COAX	DISABLE DSI		
	Vmin	Vtyp	Vmax					
0	0	0	0.126 * V _{DDIO}	前开	10.0	1	0	0
1	0.179 * V _{DDIO}	0.211 * V _{DDIO}	0.244 * V _{DDIO}	0.380	73.2	20.0	1	0
2	0.286 * V _{DDIO}	0.325 * V _{DDIO}	0.364 * V _{DDIO}	0.585	60.4	30.1	1	1
3	0.404 * V _{DDIO}	0.441 * V _{DDIO}	0.472 * V _{DDIO}	0.794	51.1	40.2	1	1
4	0.526 * V _{DDIO}	0.556 * V _{DDIO}	0.590 * V _{DDIO}	1.001	40.2	51.1	0	0
5	0.643 * V _{DDIO}	0.673 * V _{DDIO}	0.708 * V _{DDIO}	1.211	30.1	61.9	0	1
6	0.763 * V _{DDIO}	0.790 * V _{DDIO}	0.825 * V _{DDIO}	1.421	18.7	71.5	0	1
7	0.880 * V _{DDIO}	V _{DDIO}	V _{DDIO}	1.8	10.0	前开	0	1

表 8-12 IDX 的串行控制总线地址

编号	Vdd 电压范围	Vdd 目标电压	建议的 STRAP 配置电阻器 (1% TOL)	分配的 I2C 地址
	Vmin	Vtyp	Vmax	
0	0	0	0.135 * V _{DDIO}	0
1	0.178 * V _{DDIO}	0.213 * V _{DDIO}	0.247 * V _{DDIO}	0x0C
2	0.289 * V _{DDIO}	0.327 * V _{DDIO}	0.363 * V _{DDIO}	0x0E
3	0.407 * V _{DDIO}	0.441 * V _{DDIO}	0.467 * V _{DDIO}	0x10
4	0.526 * V _{DDIO}	0.556 * V _{DDIO}	0.590 * V _{DDIO}	0x12
5	0.640 * V _{DDIO}	0.671 * V _{DDIO}	0.701 * V _{DDIO}	0x14
6	0.757 * V _{DDIO}	0.787 * V _{DDIO}	0.814 * V _{DDIO}	0x16
7	0.877 * V _{DDIO}	V _{DDIO}	V _{DDIO}	0x18

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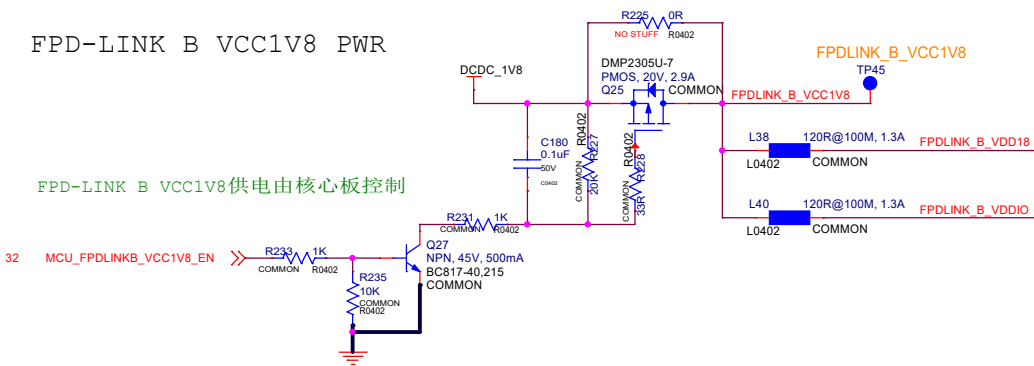
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Display-DSI To FPD-LINK III B

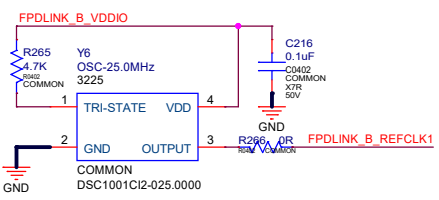
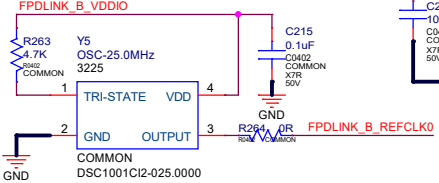
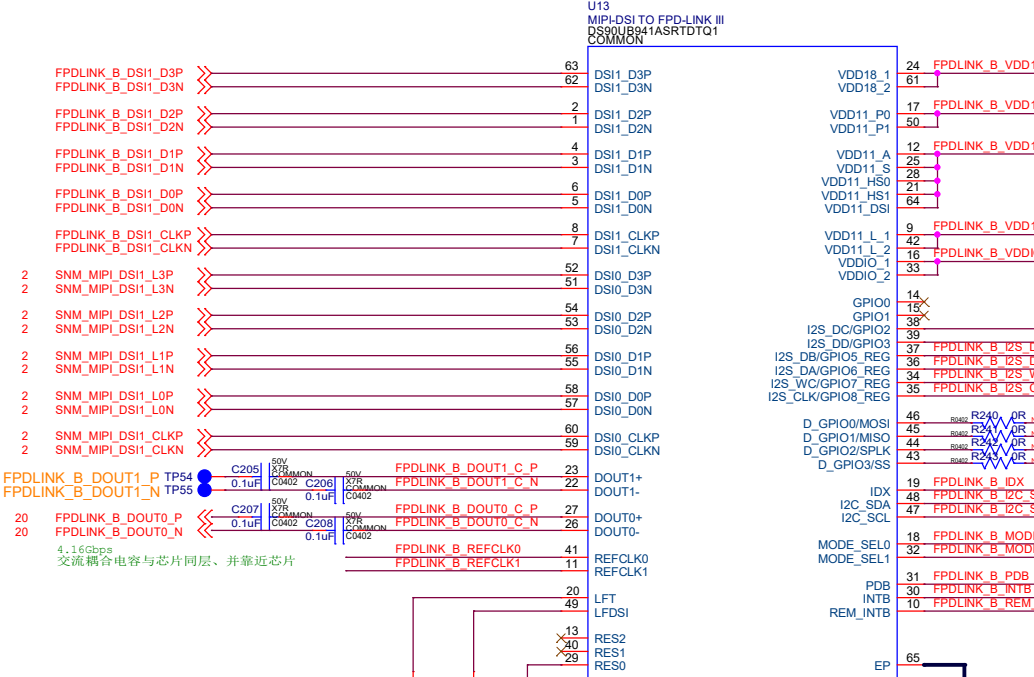
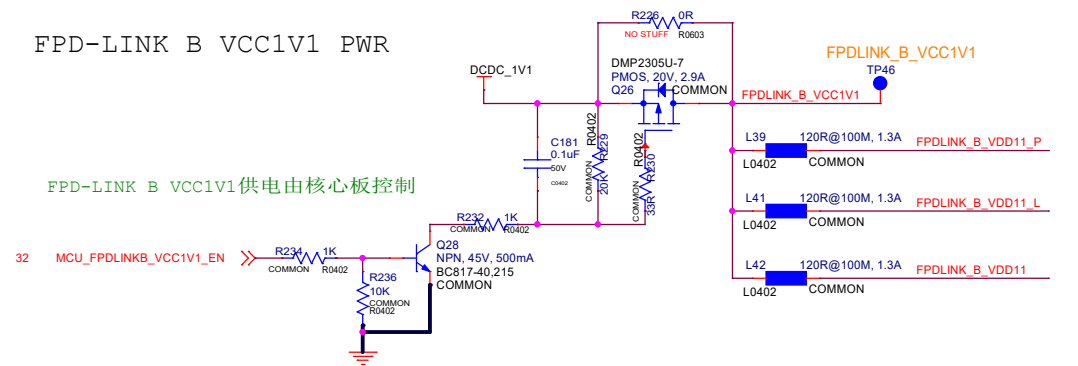
FPD-LINK B VCC1V8 PWR

FPD-LINK B VCC1V8供电由核心板控制



FPD-LINK B VCC1V1 PWR

FPD-LINK B VCC1V1供电由核心板控制



4.15Gbps 交流耦合电容与芯片同层、并靠近芯片

0.1uF去耦电容靠近供电引脚布局

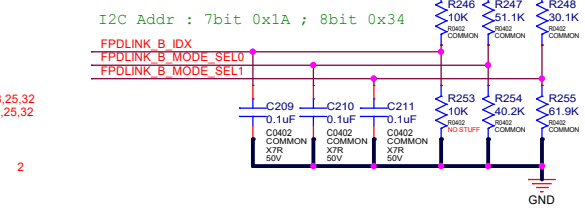
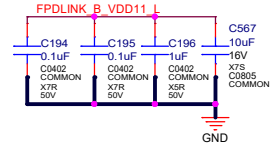
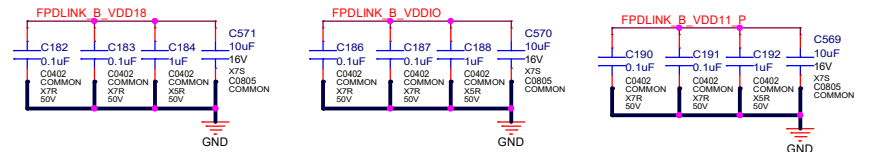


表 8-9 Strap 配置 MODE_SEL0

MODE 编号	Vdd 电压	Vdd 目标电压 (1% TOL)	Vdd 目标电压 (1% TOL)	建议的 STRAP 配置电阻器 (kΩ)	R1 (kΩ)	R2 (kΩ)	SPLITTER	DSI LANES
0	0	0	0.126 * Vdd0	100	10.0	0	1	1
1	0.179 * Vdd0	0.211 * Vdd0	0.244 * Vdd0	0.380	73.2	20.0	0	2
2	0.286 * Vdd0	0.325 * Vdd0	0.364 * Vdd0	0.585	60.4	30.1	0	3
3	0.404 * Vdd0	0.441 * Vdd0	0.472 * Vdd0	0.794	51.1	40.2	0	4
4	0.526 * Vdd0	0.556 * Vdd0	0.590 * Vdd0	1.001	40.2	51.1	1	1
5	0.643 * Vdd0	0.673 * Vdd0	0.708 * Vdd0	1.211	30.1	61.9	1	2
6	0.763 * Vdd0	0.790 * Vdd0	0.825 * Vdd0	1.421	18.7	71.5	1	3
7	0.880 * Vdd0	0.908 * Vdd0	0.948 * Vdd0	1.8	10.0	100	1	4

表 8-10 Strap 配置 MODE_SEL1

MODE 编号	Vdd 电压	Vdd 目标电压 (1% TOL)	Vdd 目标电压 (1% TOL)	建议的 STRAP 配置电阻器 (kΩ)	R1 (kΩ)	R2 (kΩ)	CLOCK	COAX	DISABLE DSI
0	0	0	0.126 * Vdd0	100	10.0	0	0	0	0
1	0.179 * Vdd0	0.211 * Vdd0	0.244 * Vdd0	0.380	73.2	20.0	1	0	1
2	0.286 * Vdd0	0.325 * Vdd0	0.364 * Vdd0	0.585	60.4	30.1	1	1	0
3	0.404 * Vdd0	0.441 * Vdd0	0.472 * Vdd0	0.794	51.1	40.2	1	1	1
4	0.526 * Vdd0	0.556 * Vdd0	0.590 * Vdd0	1.001	40.2	51.1	0	0	0
5	0.643 * Vdd0	0.673 * Vdd0	0.708 * Vdd0	1.211	30.1	61.9	0	0	1
6	0.763 * Vdd0	0.790 * Vdd0	0.825 * Vdd0	1.421	18.7	71.5	0	1	0
7	0.880 * Vdd0	0.908 * Vdd0	0.948 * Vdd0	1.8	10.0	100	0	1	1

表 8-12 IDX 的串行控制总线地址

编号	Vdd 电压范围	Vdd 目标电压 (1% TOL)	Vdd 目标电压 (1% TOL)	建议的 STRAP 配置电阻器 (kΩ)	R1 (kΩ)	R2 (kΩ)	7 位	8 位
0	0	0	0.135 * Vdd0	10.0	10.0	0x0C	0x1C	
1	0.179 * Vdd0	0.213 * Vdd0	0.247 * Vdd0	0.384	73.2	20.0	0x0E	0x1C
2	0.289 * Vdd0	0.327 * Vdd0	0.363 * Vdd0	0.589	60.4	30.1	0x10	0x20
3	0.407 * Vdd0	0.441 * Vdd0	0.487 * Vdd0	0.793	51.1	40.2	0x12	0x24
4	0.526 * Vdd0	0.555 * Vdd0	0.584 * Vdd0	0.999	40.2	51.1	0x14	0x28
5	0.640 * Vdd0	0.671 * Vdd0	0.701 * Vdd0	1.208	30.1	61.9	0x16	0x2C
6	0.757 * Vdd0	0.787 * Vdd0	0.818 * Vdd0	1.417	18.7	71.5	0x18	0x30
7	0.877 * Vdd0	0.908 * Vdd0	0.948 * Vdd0	1.8	10.0	100	0x1A	0x34

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