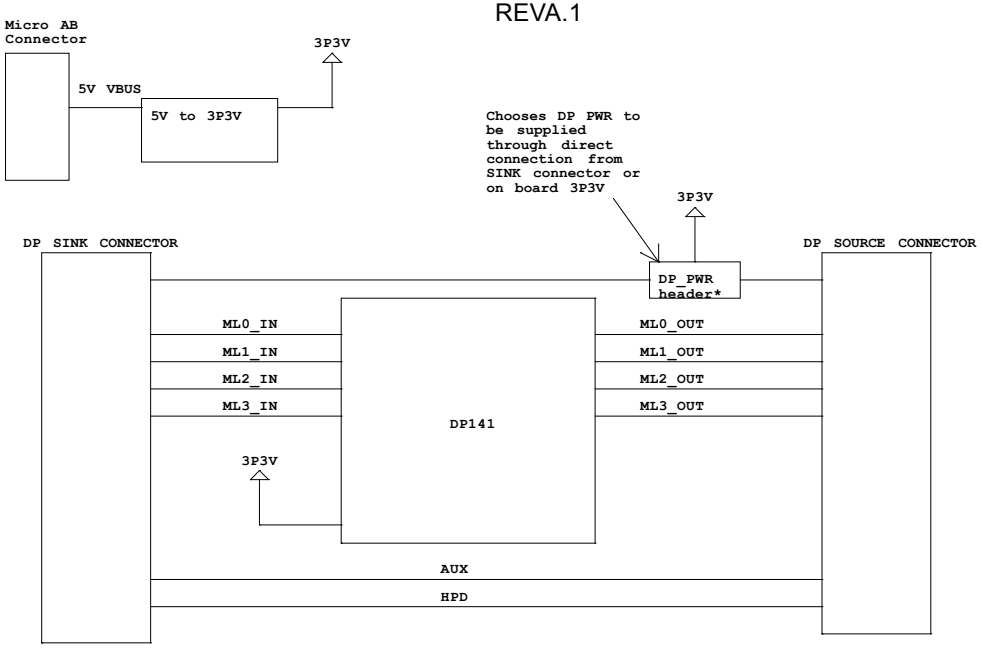
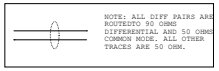
DP141RLJEVM INT029

REVA.1



DESIGN NOTE1 Min of 15 Vias recommended for GND Pad connection

DESIGN NOTE2



DESIGN NOTE3

Value of the cap to vary depending on power rail ramp-up time

DESIGN NOTE4

Device disable/I2C Reset if asserted low

DESIGN NOTE6

Place filter capacitors near DP141

DESIGN NOTE7

indicates default SHUNT position

DESIGN NOTE8

Place on the edge with 500-mil clearance from pin 9 and 10.

DESIGN NOTE5 **SIGNALS to be High-Z, pulled high or low. Refer to the datasheet for config info.**

EQ GAIN in steps of approximately 2dB

EQ1	EQ0	EQ GAIN
LOW	LOW	000
LOW	HIZ	000
LOW	HIGH	001
HIZ	LOW	010
HIZ	HIZ	011
HIZ	HIGH	100
HIGH	LOW	101
HIGH	HIZ	110
HIGH	HIGH	111

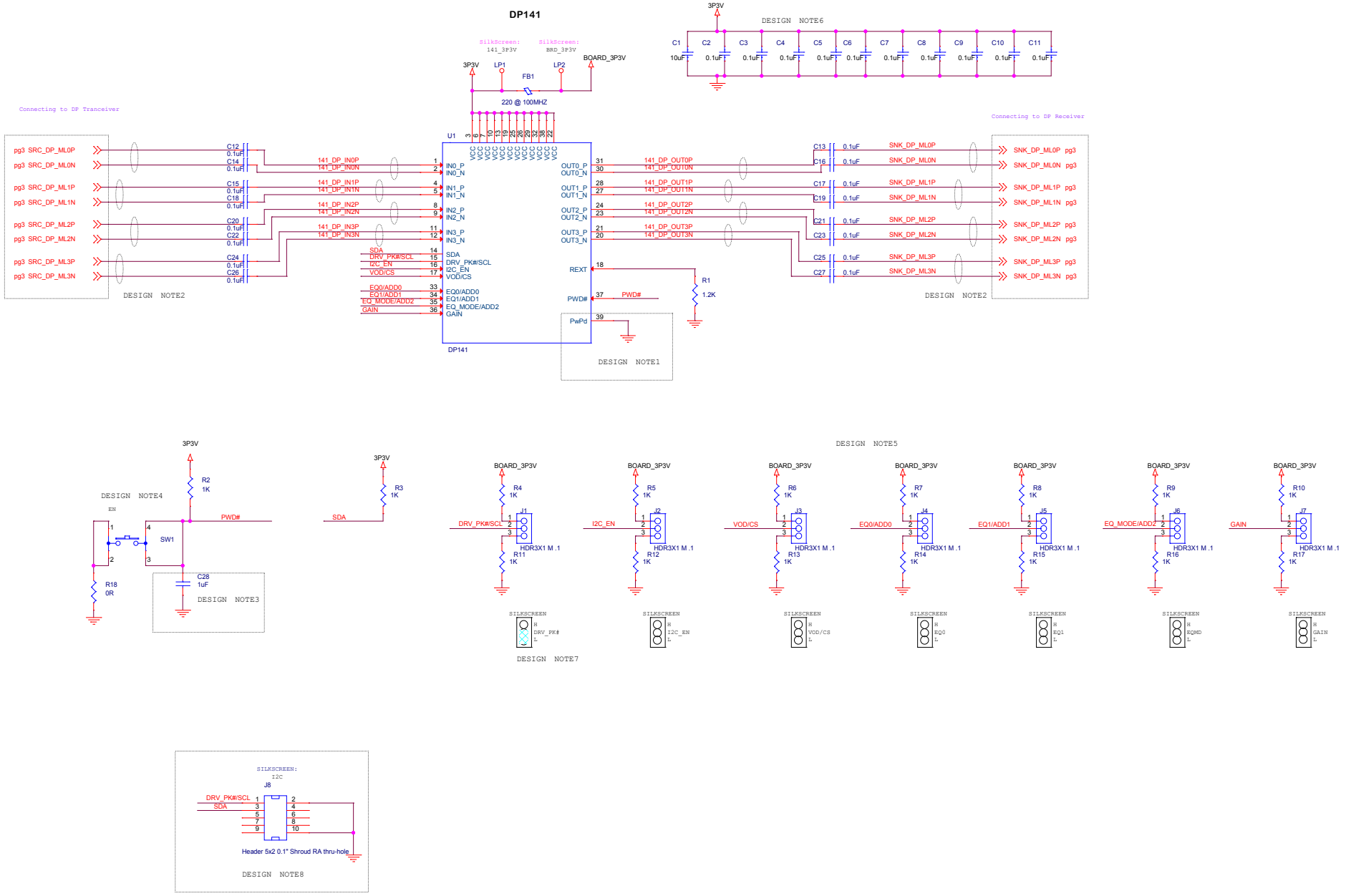
FINAL EQ Gain

EQ0 GAIN	GAIN	DC GAIN(dB)	EQ GAIN(dB)
000 - 111	LOW	-6	1 - 9
000 - 111	HIZ	-6	7 - 17
000 - 111	VCC	0	1 - 9

TEXAS INSTRUMENTS

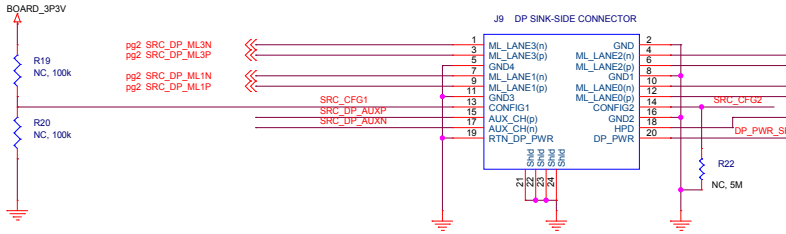
DP141RLJEVM INT029 Schematic

SIZE	DWG NO:	
Custom		
SCALE: NONE	Thursday, February 18, 2016	Sheet 1 of 3

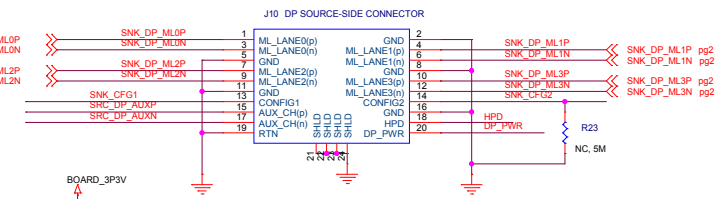


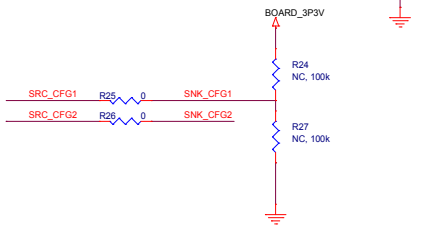
Title	DP141RLJEVM INT029: DP141	
Size C	Document Number <Doc>	Rev A.0
Date: Thursday, February 25, 2016	Sheet 2 of 3	

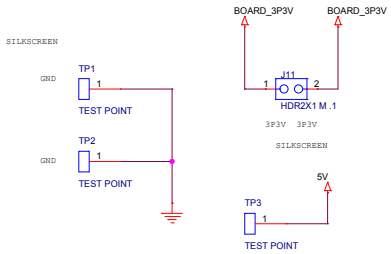
DisplayPort Source Connection

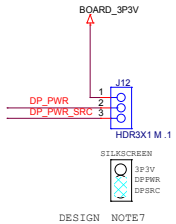


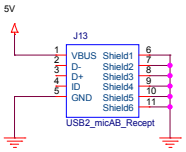
DisplayPort Sink Connection

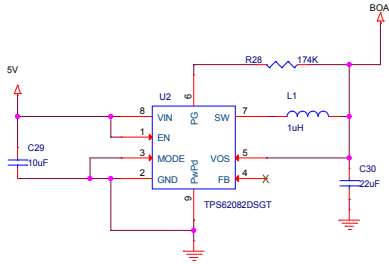


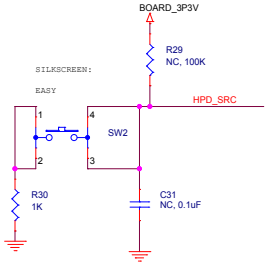












Title: DP141RLJEVM INT029: DP Connectors		
Size: C	Document Number: <Doc>	Rev: <RevCode>
Date: Friday, February 26, 2016	Sheet 3 of 3	