IT6505

DispalyPort 1.1a Transmitter

Specification V1.1

General Description

The IT6505 is a high-performance DisplayPort 1.1a transmitter, fully compliant with DisplayPort 1.1a, HDCP 1.3 specifications. The IT6505 supports color depth of up to 36 bits (12 bits/color) and ensures robust transmission of high-quality uncompressed video content, along with uncompressed and compressed digital audio content.

Aside from the various video output formats supported, the IT6505 also encodes and transmits up to 8 channels of I^2S digital audio, with sampling rate up to 192kHz and sample size up to 24 bits. In addition, an S/PDIF input port takes in compressed audio of up to 192kHz frame rate.

Each IT6505 chip comes preprogrammed with an unique HDCP key, in compliance with the HDCP 1.3 standard so as to provide secure transmission of high-definition content. Users of the IT6505 need not purchase any HDCP keys or ROMs.

Features

- DisplayPort 1.1a transmitter
- Compliant with DisplayPort 1.1a, HDCP 1.3 specifications
- Supporting two link speeds, HBR(2.7Gbps) and RBR(1.62Gbps).
- Various video input interface supporting digital video standards such as:
  - 18/24/30/36-bit RGB/YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (CCIR-656)
  - 36/48/60/72-bit dual-bus interface (double data bus width, half clock rate) for RGB/YCbCr 4:4:4
- Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color spaces with programmable coefficients.
- Up/down sampling between YCbCr 4:4:4 and YCbCr 4:2:2
- Dithering for conversion from 12-bit/10-bit component to 8-bit
- Digital audio input interface supporting
  - up to four I^2S interface supporting 8-channel audio, with sample rates of 32~192 kHz and sample sizes of 16~24 bits
  - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
  - Compatible with IEC 60958 and IEC 61937
  - Audio down-sampling of 2X and 4X
- Software programmable DispalyPort output swing and pre-emphasis level
- MCLK input is optional for audio operation. Users could opt to implement audio input interface with or without MCLK.

- Integrated pre-programmed HDCP keys
- Purely hardware HDCP engine increasing the robustness and security of HDCP operation
- Embedded full-function pattern generator
- MCCS over AUX channel
- Intelligent, programmable power management
- 144-pin LQFP package
- RoHS Compliant (100% Green available)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6505E	0~70	144-pin LQFP	Green

Pin Diagram

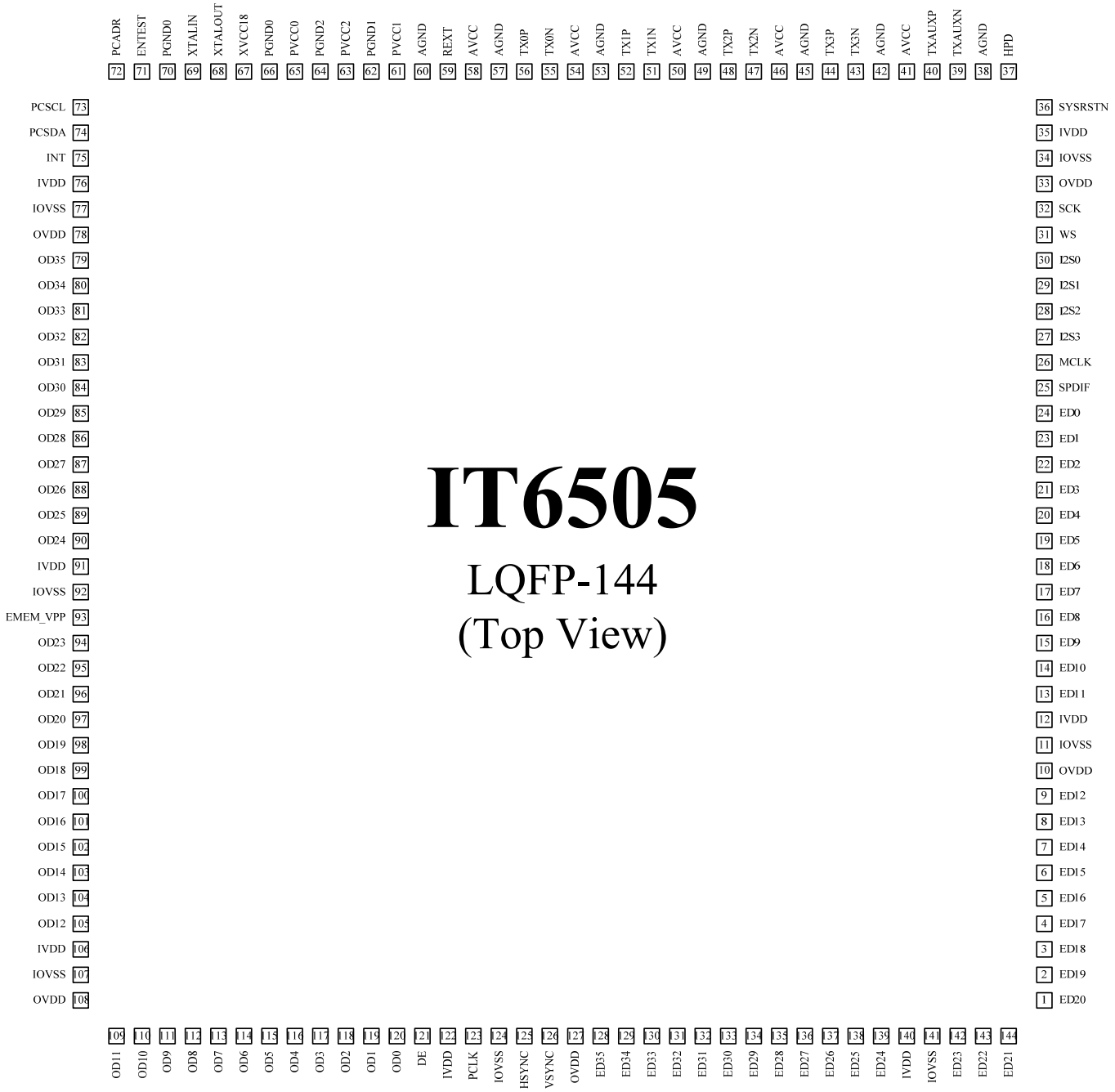


Figure 1. IT6505 pin diagram

Pin Description

Digital Video Input Pins

Pin Name	Direction	Description	Type	Pin No.
OD[35:0] ED[35:0]	Input	Digital video input pins.	LVTTL	79-90, 94-105, 109-120, 128-139 142-144, 1-9, 13-24
DE	Input	Data enable	LVTTL	121
HSYNC	Input	Horizontal sync. signal	LVTTL	125
VSYNC	Input	Vertical sync. signal	LVTTL	126
PCLK	Input	Input data clock	LVTTL	123

Digital Audio Input Pins

Pin Name	Direction	Description	Type	Pin No.
SCK	Input	I2S serial clock input	LVTTL	32
WS	Input	I2S word select input	LVTTL	31
I2S0	Input	I2S serial data input	LVTTL	30
I2S1	Input	I2S serial data input	LVTTL	29
I2S2	Input	I2S serial data input	LVTTL	28
I2S3	Input	I2S serial data input	LVTTL	27
MCLK	Input	Audio master clock input	LVTTL	26
SPDIF	Input	S/PDIF audio input	LVTTL	25

Programming Pins

Pin Name	Direction	Description	Type	Pin No.
INT#	Output	Interrupt output. Default active-low (5V-tolerant)	LVTTL	75
SYSRSTN	Input	Hardware reset pin. Active LOW (5V-tolerant)	Schmitt	36
PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	Schmitt	73
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	Schmitt	74
PCADR	Input	Serial programming device address select	LVTTL	72
HPD	Input	Hot Plug Detection (5V-tolerant)	LVTTL	37
ENTEST	Input	Must be tied low via a resistor.	LVTTL	71

DisplayPort front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
TX3P	Analog	DisplayPort Lane 3 positive output	DP	44

TX3N	Analog	DisplayPort Lane 3 negative output	DP	43
TX2P	Analog	DisplayPort Lane 2 positive output	DP	48
TX2N	Analog	DisplayPort Lane 2 negative output	DP	47
TX1P	Analog	DisplayPort Lane 1 positive output	DP	52
TX1N	Analog	DisplayPort Lane 1 negative output	DP	51
TX0P	Analog	DisplayPort Lane 0 positive output	DP	56
TX0N	Analog	DisplayPort Lane 0 negative output	DP	55
TXAUXP	Analog	DisplayPort AUX channel positive signal	DP	40
TXAUXN	Analog	DisplayPort AUX channel negative signal	DP	39
XTALIN	Analog	DisplayPort AFE crystal input (27MHz)	Analog	69
XTALOUT	Analog	DisplayPort AFE crystal output (27MHz)	Analog	68
REXT	Analog	External resistor for setting DisplayPort output level. Default tied to AVCC via a 820-Ohm SMD resistor.	Analog	59

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD	Digital logic power (1.8V)	Power	12, 35, 76, 91, 106, 122, 140
OVDD	I/O Pin power (3.3V)	Power	10, 33, 78, 108, 127
IOVSS	Digital logic and I/O pin common ground	Ground	11, 34, 77, 92, 107, 124, 141
AVCC	DisplayPort analog frontend power (1.8V)	Power	41, 46, 50, 54, 58
AGND	DisplayPort analog frontend ground	Ground	38, 42, 45, 49, 53, 57, 60
PVCC0	DisplayPort core PLL power (1.8V)	Power	65
PGND0	DisplayPort core PLL ground	Ground	66, 70
PVCC1	DisplayPort core PLL power (1.8V)	Power	61
PGND1	DisplayPort core PLL ground	Ground	62
PVCC2	Filter PLL power (1.8V)	Power	63
PGND2	Filter PLL ground	Ground	64
XVCC18	DisplayPort core PLL power (1.8V)	Power	67
EMEM_VPP	E-Memory write power (tie 10K to GND)	Power	93

Functional Description

The IT6505 provides complete solutions for DisplayPort V1.1a Source systems, supporting processing and transmission of Deep Color video and state-of-the-art digital audio. Advanced processing algorithms are employed to optimize the performance of video processing such as color space conversion and up/down sampling. The functional block diagram of the IT6505 is shown in **Figure 2**, which describes clearly the data flow.

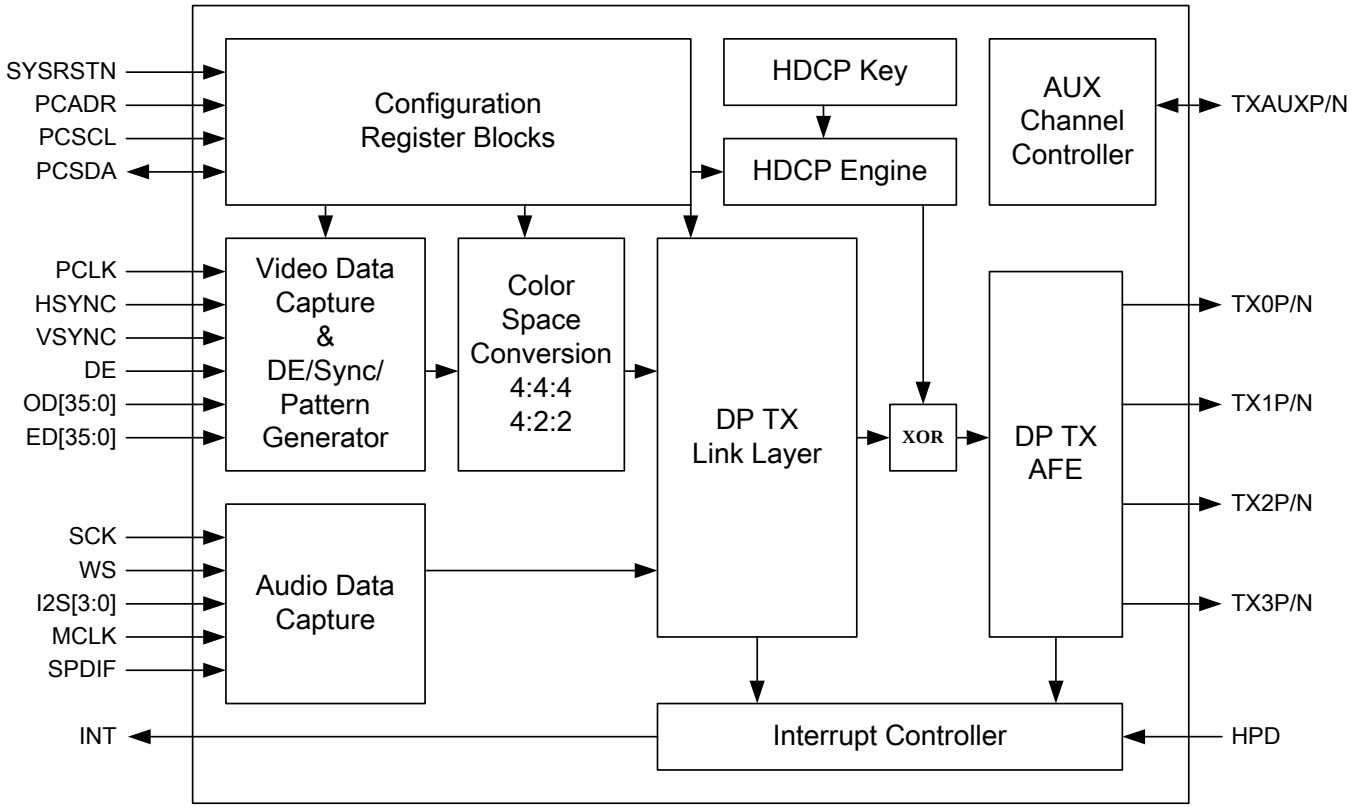


Figure 2. Functional block diagram of IT6505

Video Data Processing Flow

Table 3 depicts the video data processing flow. For the purpose of retaining maximum flexibility, most of the block enablings and path bypassings are controlled through register programming. Please refer to IT6505 Programming Guide for detailed and precise descriptions.

As can be seen from Table 3, the first step of video data processing is to prepare the video data (Data), data enable signal (DE), video clock (Clock), horizontal sync and vertical sync signals (H/VSYNC). While the video data and video clock are always readily available from input pins, the preparation of the data enable and sync signals require special extraction process (Embedded Ctrl. Signals Extraction & DE Generator) depending on the format of input video data.

All the data then undergo a series of video processing including YCbCr up/down-sampling, color-space conversion and dithering. Depending on the selected input and output video formats, different processing blocks are either enabled or bypassed via register control. For the sake of flexibility, this is all done in software register programming. Therefore, extra care should be taken in keeping the selected input-output format combination and the corresponding video processing block selection. Please refer to the IT6505 Programming Guide for suggested register setting.

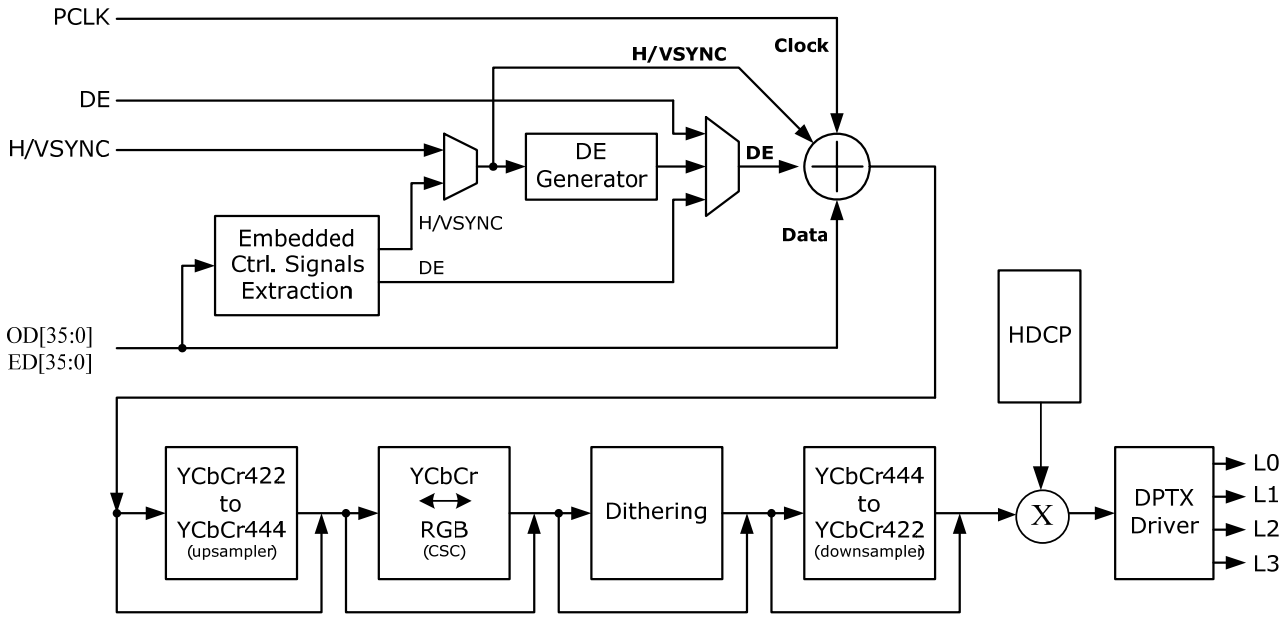


Figure 3. Video data processing flow of the IT6505

Designated as OD[35:0] and ED[35:0], the input video data could take on bus width of 8 bits to 72 bits. This input interface could be configured to support various data formats as listed in Table 1.

All the major video processing blocks in the IT6505 are done in 14 bits per channel in order to minimize rounding errors and other computational residuals that occur during processing. General description of block functions is as follows:

Extraction of embedded control signals (Embedded Ctrl. Signals Extraction)

Input video formats with only embedded sync signals rely on this block to derive the proper Hsync, Vsync and DE signals. Specifically, CCIR-656 video stream includes Start of Active Video (SAV) and End of Active Video (EAV) that this block uses to extract the required control signals.

Generation of data enable signal (DE Generator)

DE signal defines the region of active video data. In cases where the video decoders supply no such DE signals to the IT6505, this block is used to generate appropriate DE signal from Hsync, Vsync and Clock.

Upsampling (YCbCr422 to YCbCr444)

In cases where input signals are in YCbCr 4:2:2 format and output is selected as 4:4:4, this block is

enabled to do the upsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during upsampling.

Bi-directional Color Space Conversion (YCbCr ↔ RGB)

Many video decoders only offer YCbCr outputs, while some receivers support only RGB color space. In order to offer full compatibility between various Source and Sink combination, this block offers bi-directional RGB ↔ YCbCr color space conversion (CSC). To provide maximum flexibility, the matrix coefficients of the CSC engine in the IT6505 are fully programmable. Users could elect to employ their preferred conversion formula.

Dithering (Dithering 12-to-6/8/10)

For outputing to the 6/8/10-bits-per-channel formats, decimation from 12 bits to 6/8/10 bits is required. This block performs the necessary dithering for decimation to prevent visible artifacts from appearing.

Downsampling (YCbCr444 to YCbCr422)

In cases where input signals are in YCbCr 4:4:4 format and output is selected as YCbCr 4:2:2, this block is enabled to do the downsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during downsampling.

HDCP engine (HDCP)

The HDCP engine in the IT6505 handles all the processing required by HDCP mechanism in hardware. Software intervention is not necessary except checking for revocation. Preprogrammed HDCP keys are also embedded in the IT6505. Users need not worry about the purchasing and management of the HDCP keys.

DPTX driver (DPTX Driver)

The final step of the data processing flow is DPTX serializer. The DPTX driver serializes the input parallel data and drive out the proper electrical signals to the DisplayPort cable. The output current level is controlled through connecting a precision resistor of proper value to Pin 59 (REXT).

Input Video Data Bus Mappings

The IT6505 supports various input data mappings and formats, including those with embedded control signals only. Corresponding register setting is to be taken care of for any chosen input data mappings. Refer to IT6505 Programming Guide for detailed instruction.

Color Space	Video Format	Bus Width	H/Vsync	Clocking	Table
RGB	4:4:4	18/24/30/36	Separate	1X	2
		36/48/60/72			
		12/15/18	Separate	Dual-edged	3
YCbCr	4:4:4	18/24/30/36	Separate	1X	2
		36/48/60/72			
		12/15/18	Separate	Dual-edged	3
	4:2:2	16/20/24	Separate	1X	4
			Embedded	1X	5
		8/10/12	Separate	2X	6
			Embedded	2X	7

Table 1. Input video format supported by the IT6505

RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs

	RGB				YCbCr			
Pin Name	72/36-bit	60/30-bit	48/24-bit	36/18-bit	72/36-bit	60/30-bit	48/24-bit	36/18-bit
OD0	B0	GND	GND	GND	Cb0	GND	GND	GND
OD1	B1	GND	GND	GND	Cb1	GND	GND	GND
OD2	B2	B0	GND	GND	Cb2	Cb0	GND	GND
OD3	B3	B1	GND	GND	Cb3	Cb1	GND	GND
OD4	B4	B2	B0	GND	Cb4	Cb2	Cb0	GND
OD5	B5	B3	B1	GND	Cb5	Cb3	Cb1	GND
OD6	B6	B4	B2	B0	Cb6	Cb4	Cb2	Cb0
OD7	B7	B5	B3	B1	Cb7	Cb5	Cb3	Cb1
OD8	B8	B6	B4	B2	Cb8	Cb6	Cb4	Cb2
OD9	B9	B7	B5	B3	Cb9	Cb7	Cb5	Cb3
OD10	B10	B8	B6	B4	Cb10	Cb8	Cb6	Cb4
OD11	B11	B9	B7	B5	Cb11	Cb9	Cb7	Cb5
OD12	G0	GND	GND	GND	Y0	GND	GND	GND
OD13	G1	GND	GND	GND	Y1	GND	GND	GND
OD14	G2	G0	GND	GND	Y2	Y0	GND	GND
OD15	G3	G1	GND	GND	Y3	Y1	GND	GND
OD16	G4	G2	G0	GND	Y4	Y2	Y0	GND
OD17	G5	G3	G1	GND	Y5	Y3	Y1	GND
OD18	G6	G4	G2	G0	Y6	Y4	Y2	Y0
OD19	G7	G5	G3	G1	Y7	Y5	Y3	Y1
OD20	G8	G6	G4	G2	Y8	Y6	Y4	Y2
OD21	G9	G7	G5	G3	Y9	Y7	Y5	Y3
OD22	G10	G8	G6	G4	Y10	Y8	Y6	Y4
OD23	G11	G9	G7	G5	Y11	Y9	Y7	Y5
OD24	R0	GND	GND	GND	Cr0	GND	GND	GND
OD25	R1	GND	GND	GND	Cr1	GND	GND	GND
OD26	R2	R0	GND	GND	Cr2	Cr0	GND	GND
OD27	R3	R1	GND	GND	Cr3	Cr1	GND	GND
OD28	R4	R2	R0	GND	Cr4	Cr2	Cr0	GND
OD29	R5	R3	R1	GND	Cr5	Cr3	Cr1	GND
OD30	R6	R4	R2	R0	Cr6	Cr4	Cr2	Cr0
OD31	R7	R5	R3	R1	Cr7	Cr5	Cr3	Cr1
OD32	R8	R6	R4	R2	Cr8	Cr6	Cr4	Cr2
OD33	R9	R7	R5	R3	Cr9	Cr7	Cr5	Cr3
OD34	R10	R8	R6	R4	Cr10	Cr8	Cr6	Cr4
OD35	R11	R9	R7	R5	Cr11	Cr9	Cr7	Cr5
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE
ED0	B0	GND	GND	GND	Cb0	GND	GND	GND
ED1	B1	GND	GND	GND	Cb1	GND	GND	GND
ED2	B2	B0	GND	GND	Cb2	Cb0	GND	GND
ED3	B3	B1	GND	GND	Cb3	Cb1	GND	GND

ED4	B4	B2	B0	GND	Cb4	Cb2	Cb0	GND
ED5	B5	B3	B1	GND	Cb5	Cb3	Cb1	GND
ED6	B6	B4	B2	B0	Cb6	Cb4	Cb2	Cb0
ED7	B7	B5	B3	B1	Cb7	Cb5	Cb3	Cb1
ED8	B8	B6	B4	B2	Cb8	Cb6	Cb4	Cb2
ED9	B9	B7	B5	B3	Cb9	Cb7	Cb5	Cb3
ED10	B10	B8	B6	B4	Cb10	Cb8	Cb6	Cb4
ED11	B11	B9	B7	B5	Cb11	Cb9	Cb7	Cb5
ED12	G0	GND	GND	GND	Y0	GND	GND	GND
ED13	G1	GND	GND	GND	Y1	GND	GND	GND
ED14	G2	G0	GND	GND	Y2	Y0	GND	GND
ED15	G3	G1	GND	GND	Y3	Y1	GND	GND
ED16	G4	G2	G0	GND	Y4	Y2	Y0	GND
ED17	G5	G3	G1	GND	Y5	Y3	Y1	GND
ED18	G6	G4	G2	G0	Y6	Y4	Y2	Y0
ED19	G7	G5	G3	G1	Y7	Y5	Y3	Y1
ED20	G8	G6	G4	G2	Y8	Y6	Y4	Y2
ED21	G9	G7	G5	G3	Y9	Y7	Y5	Y3
ED22	G10	G8	G6	G4	Y10	Y8	Y6	Y4
ED23	G11	G9	G7	G5	Y11	Y9	Y7	Y5
ED24	R0	GND	GND	GND	Cr0	GND	GND	GND
ED25	R1	GND	GND	GND	Cr1	GND	GND	GND
ED26	R2	R0	GND	GND	Cr2	Cr0	GND	GND
ED27	R3	R1	GND	GND	Cr3	Cr1	GND	GND
ED28	R4	R2	R0	GND	Cr4	Cr2	Cr0	GND
ED29	R5	R3	R1	GND	Cr5	Cr3	Cr1	GND
ED30	R6	R4	R2	R0	Cr6	Cr4	Cr2	Cr0
ED31	R7	R5	R3	R1	Cr7	Cr5	Cr3	Cr1
ED32	R8	R6	R4	R2	Cr8	Cr6	Cr4	Cr2
ED33	R9	R7	R5	R3	Cr9	Cr7	Cr5	Cr3
ED34	R10	R8	R6	R4	Cr10	Cr8	Cr6	Cr4
ED35	R11	R9	R7	R5	Cr11	Cr9	Cr7	Cr5

Table 2. RGB & YCbCr 4:4:4 Mappings

Notes:
1. Single pixel mode uses only a single data bus, OD[35:0] or ED[35:0]. When OD[35:0] is used, ED[35:0] must be tied to GND and vice versa.
2. Dual pixel mode uses both OD[35:0] and ED[35:0]. OD[35:0] is defined as the first pixel and ED[35:0] is defined as second pixel.

These are the simplest formats, with a complete definition of every pixel in each clock period. Figure 4 and Figure 5 give two examples for single pixel mode and Figure 6 give an example for dual pixel mode.

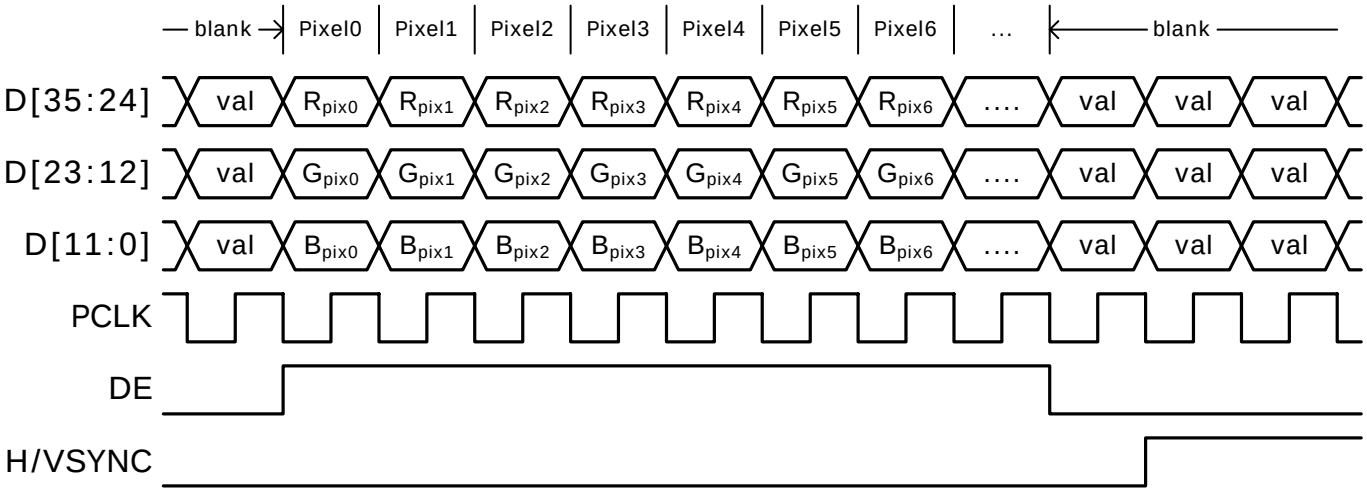


Figure 4. 36-bit RGB 4:4:4 Timing Diagram

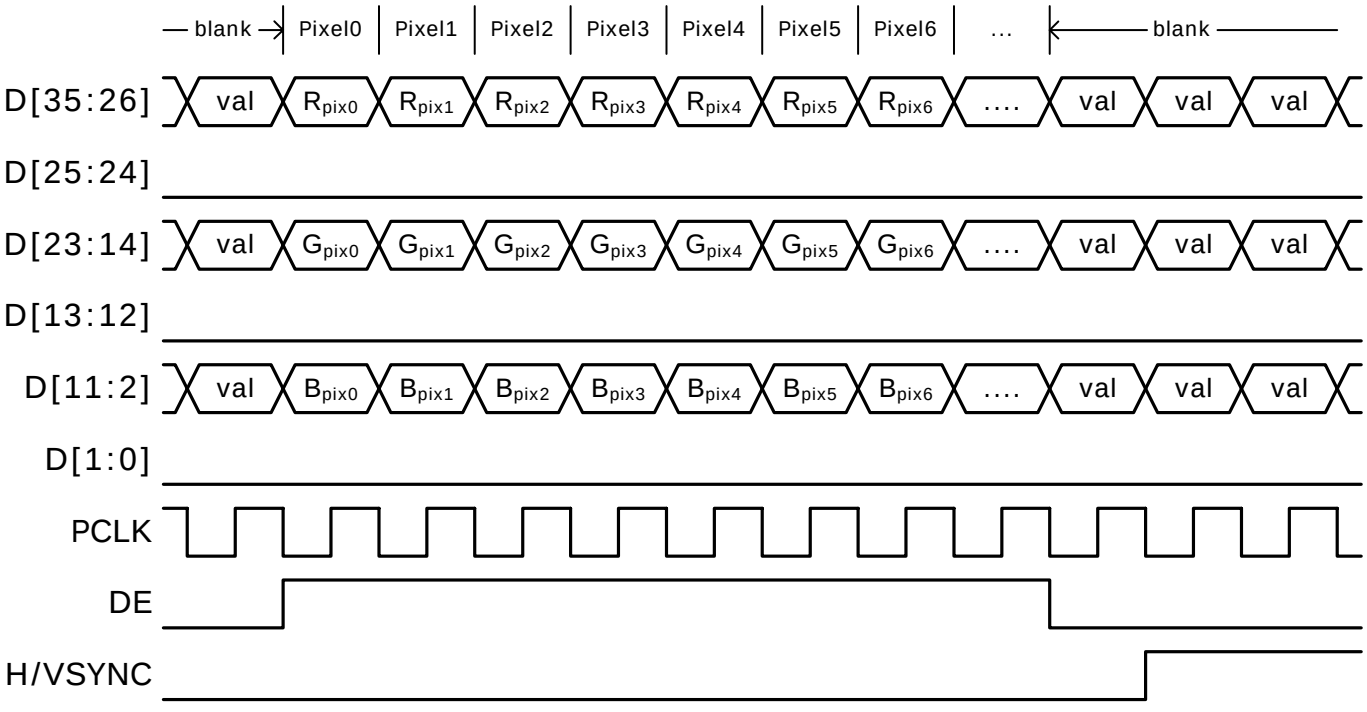


Figure 5. 30-bit RGB 4:4:4 Timing Diagram

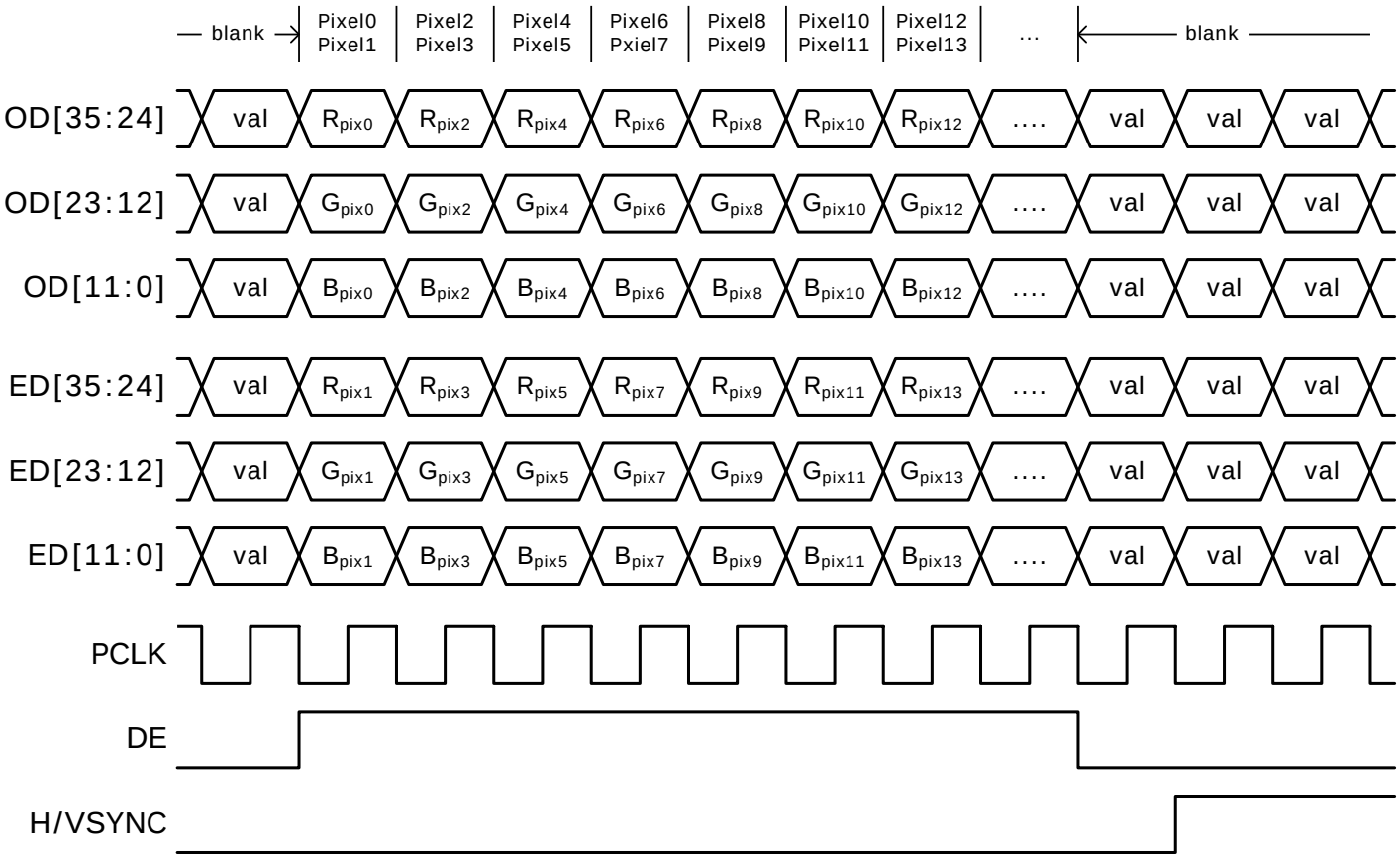


Figure 6. 72-bit RGB 4:4:4 Timing Diagram

18/15/12-bit RGB 4:4:4 and YCbCr 4:4:4 Using Dual-Edge Triggering

	RGB					
	18-bit		15-bit		12-bit	
Pin Name	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge
OD0	B0	G6	GND	GND	GND	GND
OD1	B1	G7	GND	GND	GND	GND
OD2	B2	G8	B0	G5	GND	GND
OD3	B3	G9	B1	G6	GND	GND
OD4	B4	G10	B2	G7	B0	G4
OD5	B5	G11	B3	G8	B1	G5
OD6	B6	R0	B4	G9	B2	G6
OD7	B7	R1	B5	R0	B3	G7
OD8	B8	R2	B6	R1	B4	R0
OD9	B9	R3	B7	R2	B5	R1
OD10	B10	R4	B8	R3	B6	R2
OD11	B11	R5	B9	R4	B7	R3
OD12	G0	R6	GND	GND	GND	GND
OD13	G1	R7	GND	GND	GND	GND
OD14	G2	R8	G0	R5	GND	GND
OD15	G3	R9	G1	R6	GND	GND
OD16	G4	R10	G2	R7	G0	R4
OD17	G5	R11	G3	R8	G1	R5
OD18	GND	GND	G4	R9	G2	R6
OD19	GND	GND	GND	GND	G3	R7
OD20	GND	GND	GND	GND	GND	GND
OD21	GND	GND	GND	GND	GND	GND
OD22	GND	GND	GND	GND	GND	GND
OD23	GND	GND	GND	GND	GND	GND
OD24	GND	GND	GND	GND	GND	GND
OD25	GND	GND	GND	GND	GND	GND
OD26	GND	GND	GND	GND	GND	GND
OD27	GND	GND	GND	GND	GND	GND
OD28	GND	GND	GND	GND	GND	GND
OD29	GND	GND	GND	GND	GND	GND
OD30	GND	GND	GND	GND	GND	GND
OD31	GND	GND	GND	GND	GND	GND
OD32	GND	GND	GND	GND	GND	GND
OD33	GND	GND	GND	GND	GND	GND
OD34	GND	GND	GND	GND	GND	GND
OD35	GND	GND	GND	GND	GND	GND
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE
	YCbCr					
	18-bit		15-bit		12-bit	
Pin Name	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge

OD0	Cb0	Y6	GND	GND	GND	GND
OD1	Cb1	Y7	GND	GND	GND	GND
OD2	Cb2	Y8	Cb0	Y5	GND	GND
OD3	Cb3	Y9	Cb1	Y6	GND	GND
OD4	Cb4	Y10	Cb2	Y7	Cb0	Y4
OD5	Cb5	Y11	Cb3	Y8	Cb1	Y5
OD6	Cb6	Cr0	Cb4	Y9	Cb2	Y6
OD7	Cb7	Cr1	Cb5	Cr0	Cb3	Y7
OD8	Cb8	Cr2	Cb6	Cr1	Cb4	Cr0
OD9	Cb9	Cr3	Cb7	Cr2	Cb5	Cr1
OD10	Cb10	Cr4	Cb8	Cr3	Cb6	Cr2
OD11	Cb11	Cr5	Cb9	Cr4	Cb7	Cr3
OD12	Y0	Cr6	GND	GND	GND	GND
OD13	Y1	Cr7	GND	GND	GND	GND
OD14	Y2	Cr8	Y0	Cr5	GND	GND
OD15	Y3	Cr9	Y1	Cr6	GND	GND
OD16	Y4	Cr10	Y2	Cr7	Y0	Cr4
OD17	Y5	Cr11	Y3	Cr8	Y1	Cr5
OD18	GND	GND	Y4	Cr9	Y2	Cr6
OD19	GND	GND	GND	GND	Y3	Cr7
OD20	GND	GND	GND	GND	GND	GND
OD21	GND	GND	GND	GND	GND	GND
OD22	GND	GND	GND	GND	GND	GND
OD23	GND	GND	GND	GND	GND	GND
OD24	GND	GND	GND	GND	GND	GND
OD25	GND	GND	GND	GND	GND	GND
OD26	GND	GND	GND	GND	GND	GND
OD27	GND	GND	GND	GND	GND	GND
OD28	GND	GND	GND	GND	GND	GND
OD29	GND	GND	GND	GND	GND	GND
OD30	GND	GND	GND	GND	GND	GND
OD31	GND	GND	GND	GND	GND	GND
OD32	GND	GND	GND	GND	GND	GND
OD33	GND	GND	GND	GND	GND	GND
OD34	GND	GND	GND	GND	GND	GND
OD35	GND	GND	GND	GND	GND	GND
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 3. Mappings of 12/15/18-bit 4:4:4 dual-edge triggered

In this double-edge triggering mode, PCLK frequency remains at the nominal pixel clock rate. The halved data pins, however, run at a data rate double that of the nominal pixel clock rate. Each set of data are clocked out by the rising edge and the falling edge alternatively. Overall one complete pixel is output within one PCLK period. This format is only valid for single pixel mode. Figure 7 and Figure 8 give two examples.

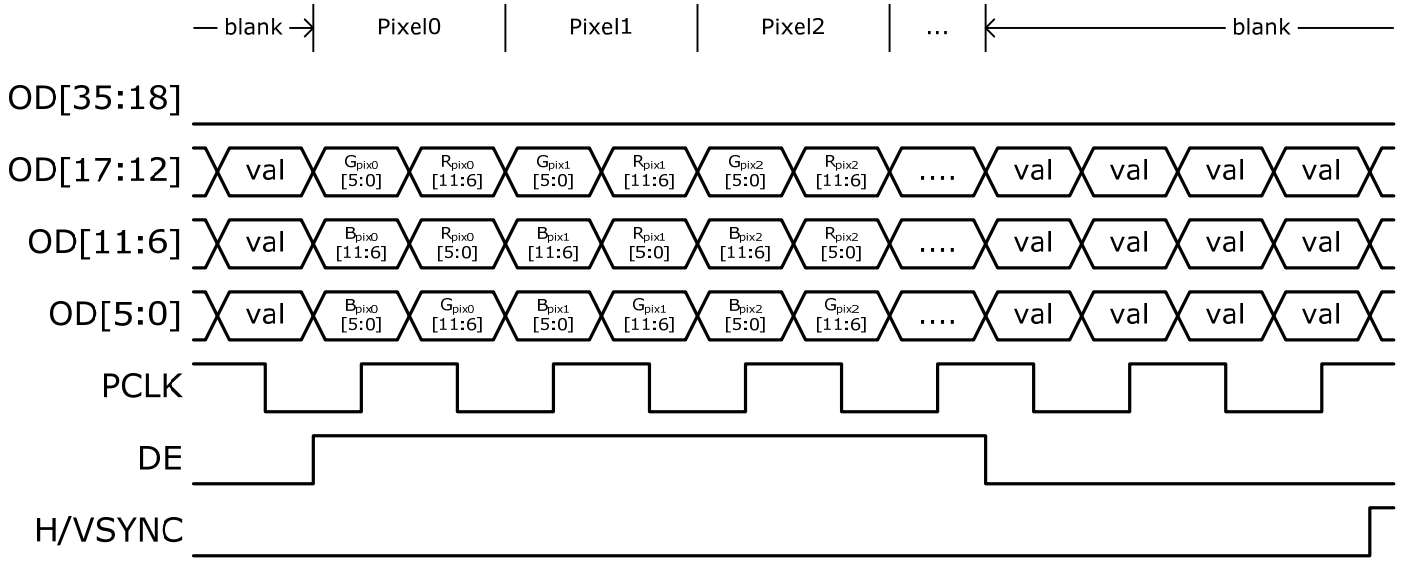


Figure 7. 18-bit RGB 4:4:4 dual-edge triggered

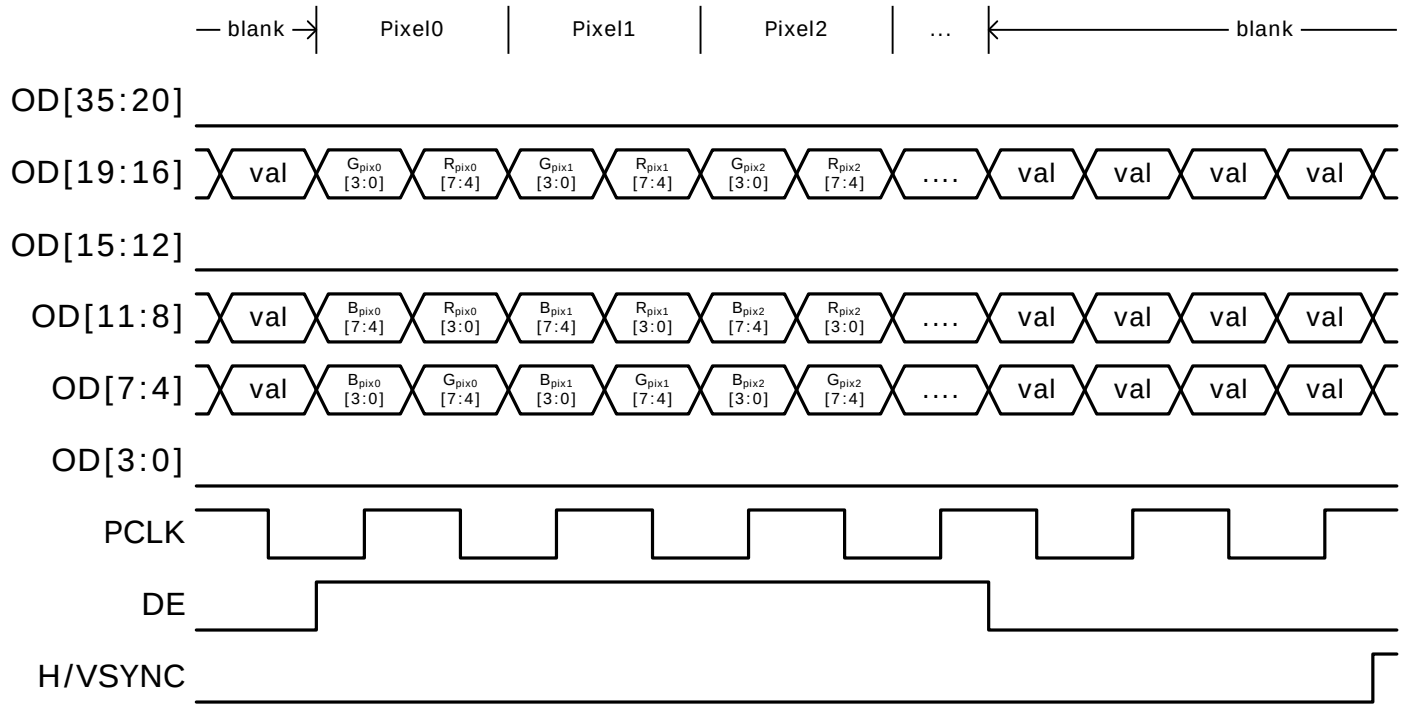


Figure 8. 12-bit RGB 4:4:4 dual-edge triggered

YCbCr 4:2:2 with Separate Syncs

	24-bit		20-bit		16-bit	
Pin Name	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1
OD0	GND	GND	GND	GND	GND	GND
OD1	GND	GND	GND	GND	GND	GND
OD2	GND	GND	GND	GND	GND	GND
OD3	GND	GND	GND	GND	GND	GND
OD4	Y0	Y0	GND	GND	GND	GND
OD5	Y1	Y1	GND	GND	GND	GND
OD6	Y2	Y2	Y0	Y0	GND	GND
OD7	Y3	Y3	Y1	Y1	GND	GND
OD8	Cb0	Cr0	GND	GND	GND	GND
OD9	Cb1	Cr1	GND	GND	GND	GND
OD10	Cb2	Cr2	Cb0	Cr0	GND	GND
OD11	Cb3	Cr3	Cb1	Cr1	GND	GND
OD12	GND	GND	GND	GND	GND	GND
OD13	GND	GND	GND	GND	GND	GND
OD14	GND	GND	GND	GND	GND	GND
OD15	GND	GND	GND	GND	GND	GND
OD16	Y4	Y4	Y2	Y2	Y0	Y0
OD17	Y5	Y5	Y3	Y3	Y1	Y1
OD18	Y6	Y6	Y4	Y4	Y2	Y2
OD19	Y7	Y7	Y5	Y5	Y3	Y3
OD20	Y8	Y8	Y6	Y6	Y4	Y4
OD21	Y9	Y9	Y7	Y7	Y5	Y5
OD22	Y10	Y10	Y8	Y8	Y6	Y6
OD23	Y11	Y11	Y9	Y9	Y7	Y7
OD24	GND	GND	GND	GND	GND	GND
OD25	GND	GND	GND	GND	GND	GND
OD26	GND	GND	GND	GND	GND	GND
OD27	GND	GND	GND	GND	GND	GND
OD28	Cb4	Cr4	Cb2	Cr2	Cb0	Cr0
OD29	Cb5	Cr5	Cb3	Cr3	Cb1	Cr1
OD30	Cb6	Cr6	Cb4	Cr4	Cb2	Cr2
OD31	Cb7	Cr7	Cb5	Cr5	Cb3	Cr3
OD32	Cb8	Cr8	Cb6	Cr6	Cb4	Cr4
OD33	Cb9	Cr9	Cb7	Cr7	Cb5	Cr5
OD34	Cb10	Cr10	Cb8	Cr8	Cb6	Cr6
OD35	Cb11	Cr11	Cb9	Cr9	Cb7	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 4. Mappings of YCbCr 4:2:2 with separate syncs

YCbCr 4:2:2 format does not have one complete pixel for every clock period. Luminace channel (Y) is given for every pixel, while the two chroma channels are given alternatively on every other clock period. The average bit amount of Y is twice that of Cb or Cr. Depending on the bus width, each component could take on different lengths. The DE period should contain an even number of clock periods. This format is only valid for single pixel mode. Figure 9 and Figure 10 give two timing examples.

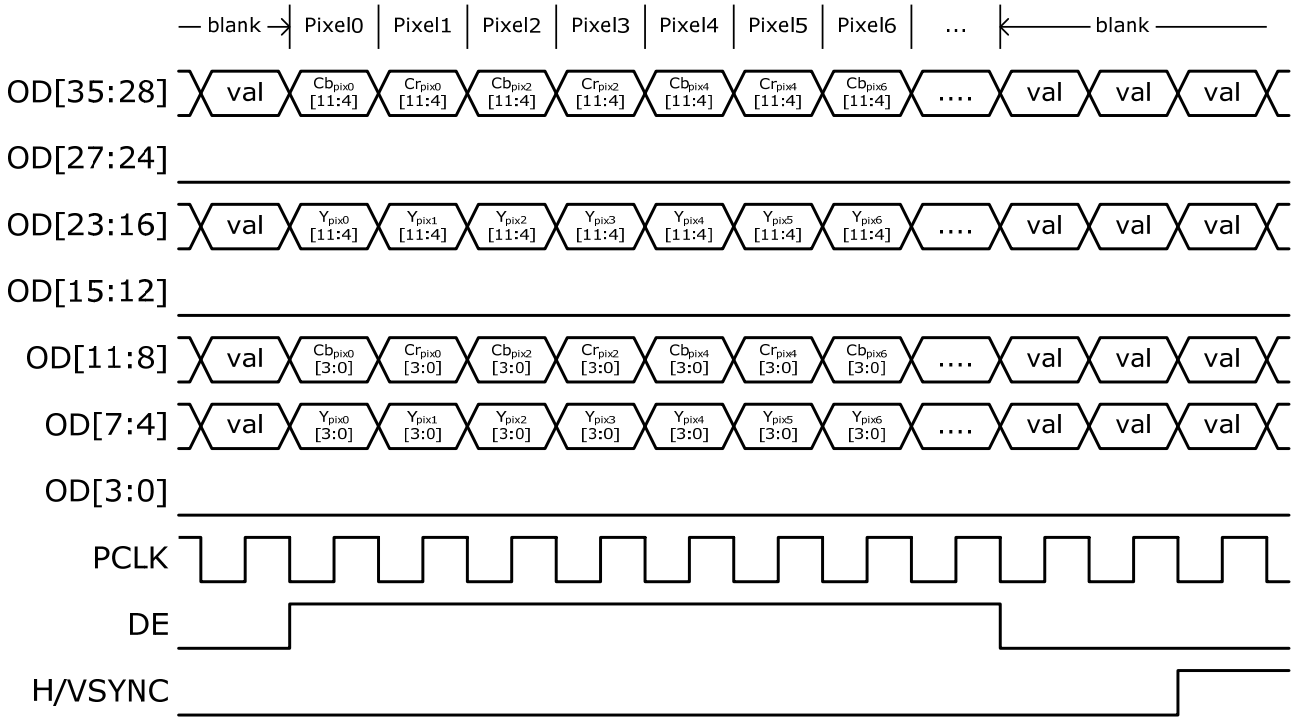


Figure 9. 24-bit YCbCr 4:2:2 with separate syncs

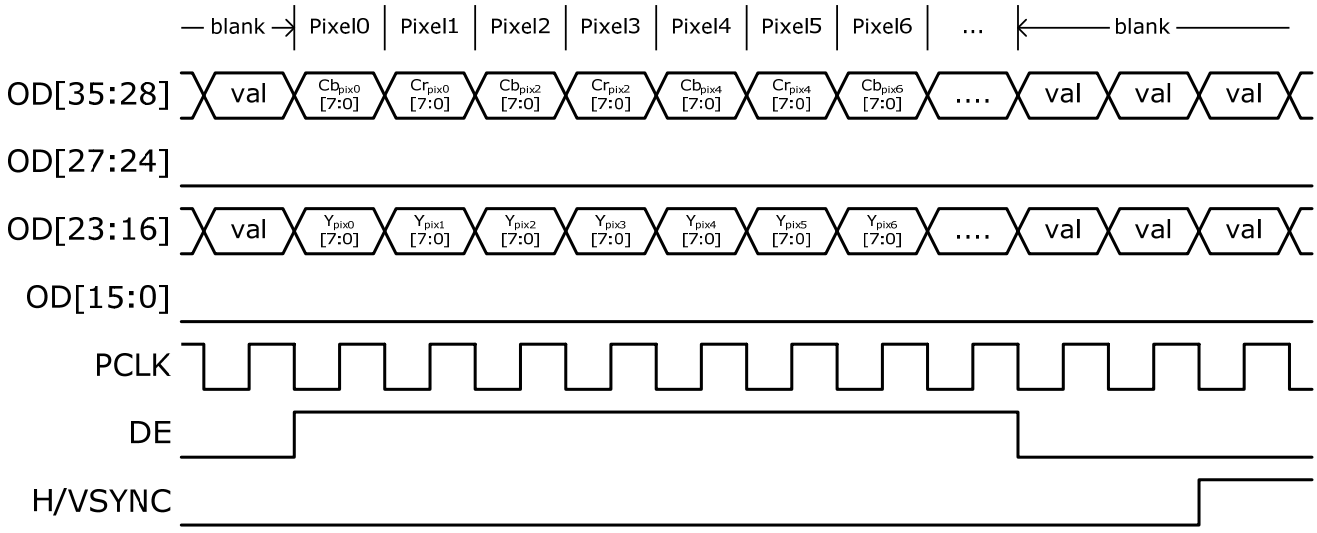


Figure 10. 16-bit YCbCr 4:2:2 with separate syncs

YCbCr 4:2:2 with Embedded Syncs

	24-bit		20-bit		16-bit	
Pin Name	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1
OD0	GND	GND	GND	GND	GND	GND
OD1	GND	GND	GND	GND	GND	GND
OD2	GND	GND	GND	GND	GND	GND
OD3	GND	GND	GND	GND	GND	GND
OD4	Y0	Y0	GND	GND	GND	GND
OD5	Y1	Y1	GND	GND	GND	GND
OD6	Y2	Y2	Y0	Y0	GND	GND
OD7	Y3	Y3	Y1	Y1	GND	GND
OD8	Cb0	Cr0	GND	GND	GND	GND
OD9	Cb1	Cr1	GND	GND	GND	GND
OD10	Cb2	Cr2	Cb0	Cr0	GND	GND
OD11	Cb3	Cr3	Cb1	Cr1	GND	GND
OD12	GND	GND	GND	GND	GND	GND
OD13	GND	GND	GND	GND	GND	GND
OD14	GND	GND	GND	GND	GND	GND
OD15	GND	GND	GND	GND	GND	GND
OD16	Y4	Y4	Y2	Y2	Y0	Y0
OD17	Y5	Y5	Y3	Y3	Y1	Y1
OD18	Y6	Y6	Y4	Y4	Y2	Y2
OD19	Y7	Y7	Y5	Y5	Y3	Y3
OD20	Y8	Y8	Y6	Y6	Y4	Y4
OD21	Y9	Y9	Y7	Y7	Y5	Y5
OD22	Y10	Y10	Y8	Y8	Y6	Y6
OD23	Y11	Y11	Y9	Y9	Y7	Y7
OD24	GND	GND	GND	GND	GND	GND
OD25	GND	GND	GND	GND	GND	GND
OD26	GND	GND	GND	GND	GND	GND
OD27	GND	GND	GND	GND	GND	GND
OD28	Cb4	Cr4	Cb2	Cr2	Cb0	Cr0
OD29	Cb5	Cr5	Cb3	Cr3	Cb1	Cr1
OD30	Cb6	Cr6	Cb4	Cr4	Cb2	Cr2
OD31	Cb7	Cr7	Cb5	Cr5	Cb3	Cr3
OD32	Cb8	Cr8	Cb6	Cr6	Cb4	Cr4
OD33	Cb9	Cr9	Cb7	Cr7	Cb5	Cr5
OD34	Cb10	Cr10	Cb8	Cr8	Cb6	Cr6
OD35	Cb11	Cr11	Cb9	Cr9	Cb7	Cr7
HSYNC	GND	GND	GND	GND	GND	GND
VSYNC	GND	GND	GND	GND	GND	GND
DE	GND	GND	GND	GND	GND	GND

Table 5. Mappings of YCbCr 4:2:2 with embedded syncs

Notes:
1. Embedded sync signals are defined by CCIR-656 standard, using SAV/EAV sequences of FF, 00, 00, XY.

Similar to YCbCr 4:2:2 with Separate Sync. The only difference is that the syncs are now non-explicit, i.e. embedded. Bus width could be 16-bit, 20-bit or 24-bit. This format is only valid for single pixel mode. Figure 1 and Figure 12 give two timing examples

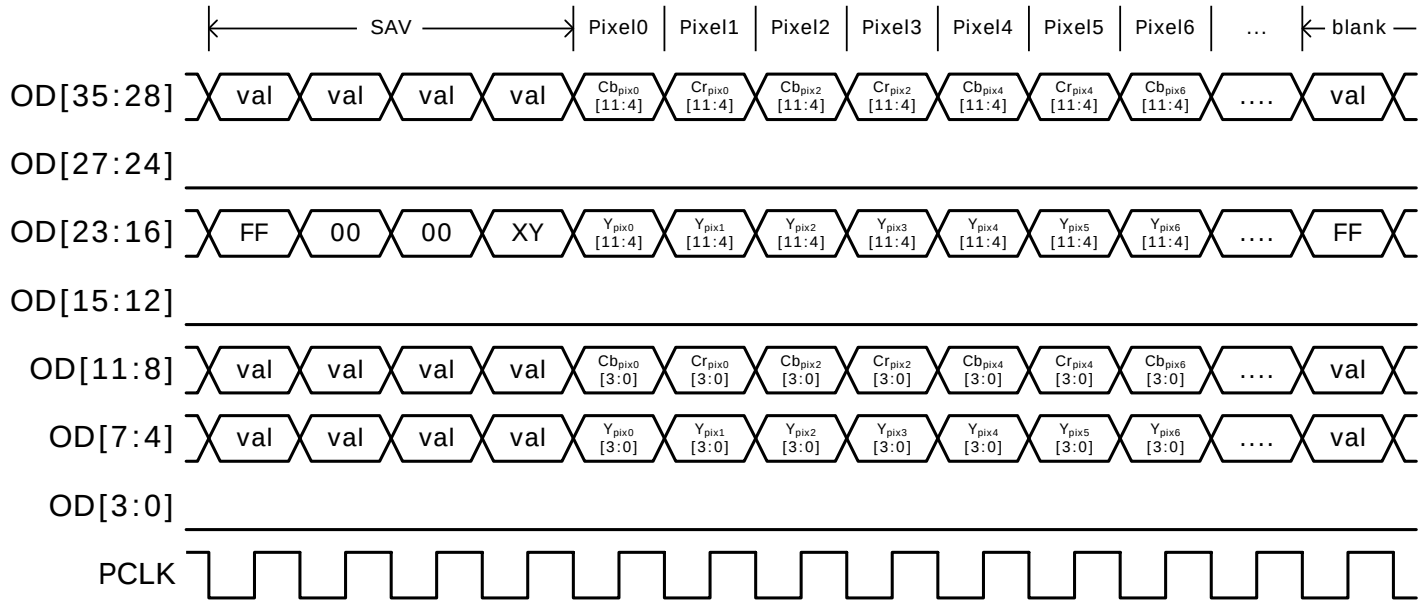


Figure 11. 24-bit YCbCr 4:2:2 with embedded syncs

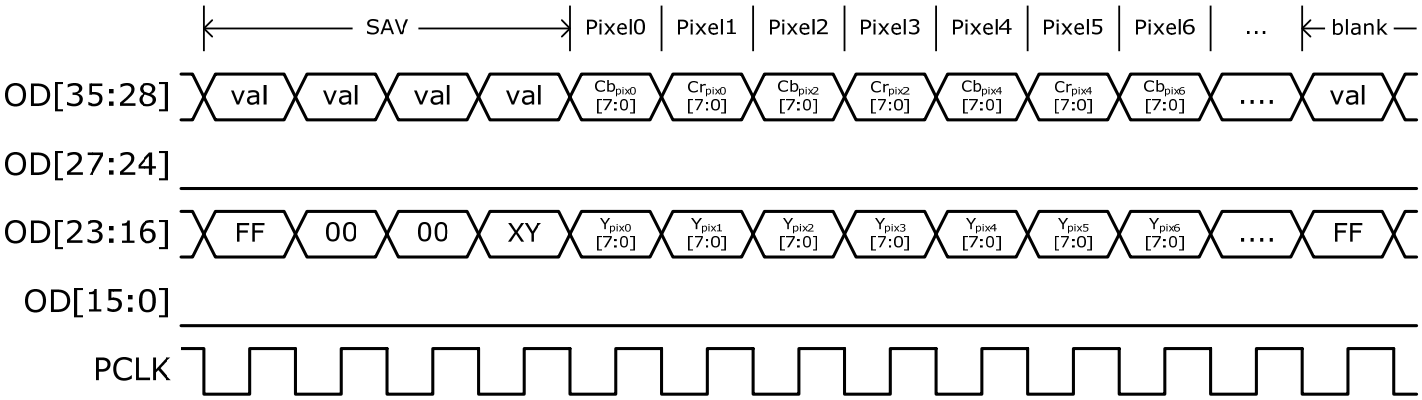


Figure 12. 16-bit YCbCr 4:2:2 with embedded syncs

CCIR-656 Format

	12-bit		10-bit		8-bit	
Pin Name	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1
OD0	GND	GND	GND	GND	GND	GND
OD1	GND	GND	GND	GND	GND	GND
OD2	GND	GND	GND	GND	GND	GND
OD3	GND	GND	GND	GND	GND	GND
OD4	C0	Y0	GND	GND	GND	GND
OD5	C1	Y1	GND	GND	GND	GND
OD6	C2	Y2	C0	Y0	GND	GND
OD7	C3	Y3	C1	Y1	GND	GND
OD8	GND	GND	GND	GND	GND	GND
OD9	GND	GND	GND	GND	GND	GND
OD10	GND	GND	GND	GND	GND	GND
OD11	GND	GND	GND	GND	GND	GND
OD12	GND	GND	GND	GND	GND	GND
OD13	GND	GND	GND	GND	GND	GND
OD14	GND	GND	GND	GND	GND	GND
OD15	GND	GND	GND	GND	GND	GND
OD16	C4	Y4	C2	Y2	C0	Y0
OD17	C5	Y5	C3	Y3	C1	Y1
OD18	C6	Y6	C4	Y4	C2	Y2
OD19	C7	Y7	C5	Y5	C3	Y3
OD20	C8	Y8	C6	Y6	C4	Y4
OD21	C9	Y9	C7	Y7	C5	Y5
OD22	C10	Y10	C8	Y8	C6	Y6
OD23	C11	Y11	C9	Y9	C7	Y7
OD24	GND	GND	GND	GND	GND	GND
OD25	GND	GND	GND	GND	GND	GND
OD26	GND	GND	GND	GND	GND	GND
OD27	GND	GND	GND	GND	GND	GND
OD28	GND	GND	GND	GND	GND	GND
OD29	GND	GND	GND	GND	GND	GND
OD30	GND	GND	GND	GND	GND	GND
OD31	GND	GND	GND	GND	GND	GND
OD32	GND	GND	GND	GND	GND	GND
OD33	GND	GND	GND	GND	GND	GND
OD34	GND	GND	GND	GND	GND	GND
OD35	GND	GND	GND	GND	GND	GND
HSYNC	GND	GND	GND	GND	GND	GND
VSYNC	GND	GND	GND	GND	GND	GND
DE	GND	GND	GND	GND	GND	GND

Table 6. Mappings of CCIR-656

The CCIR-656 format is yet another variation of the YCbCr formats. The bus width is further reduced by half compared from the previous YCbCr 4:2:2 formats, to either 8-bit, 10-bit or 12-bit. To compensate for the halving of data bus, PCLK frequency is doubled. With the double-rate output clock, luminance channel (Y) and chroma channels (Cb or Cr) are alternated. CCIR-656 format supports embedded syncs only and the DE period should contain an even number pixels. This format is only valid for single pixel mode. Figure 13 and Figure 14 give two examples.

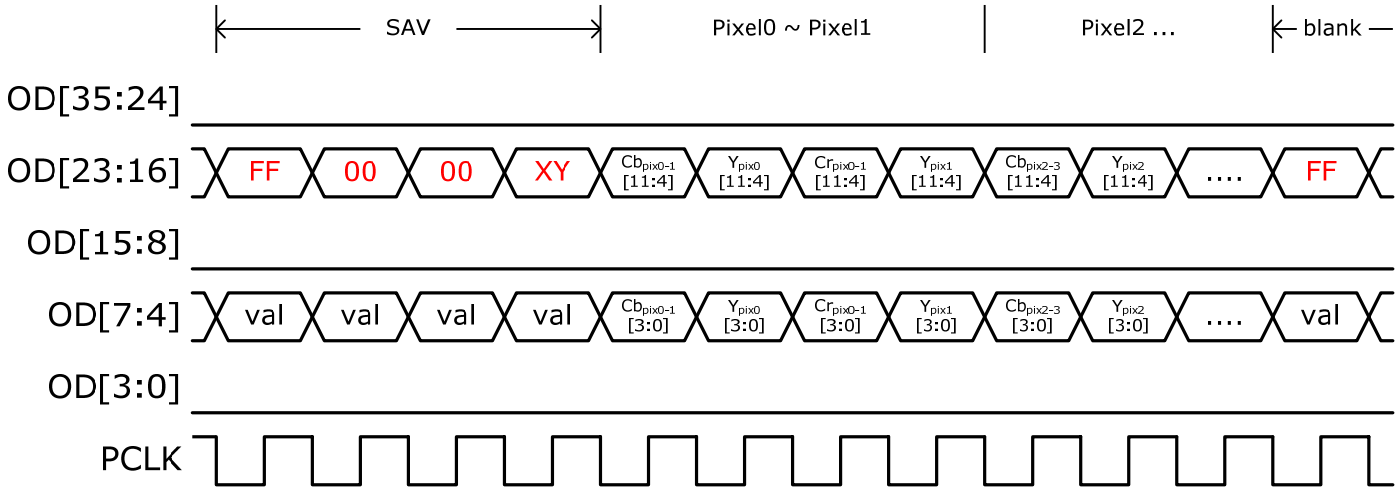


Figure 13. 12-bit CCIR-656

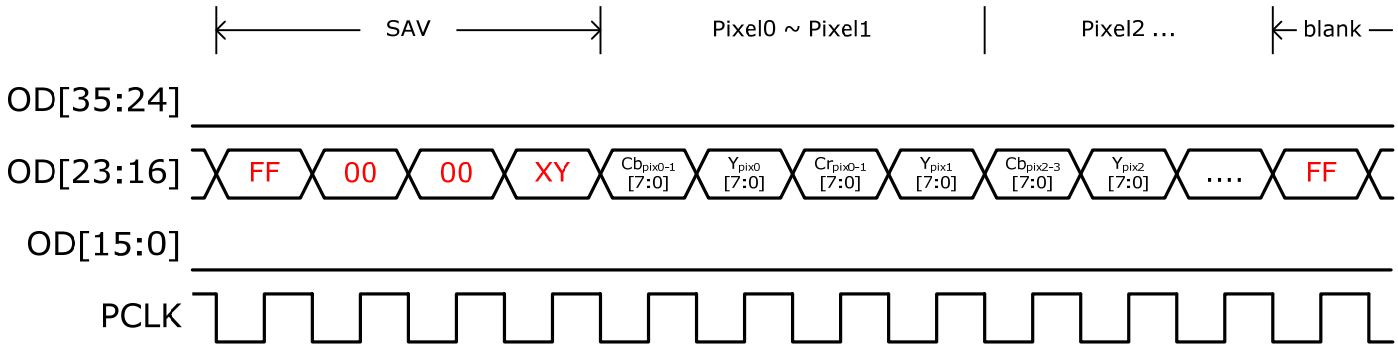


Figure 14. 8-bit CCIR-656

CCIR-656 + separate syncs

	12-bit		10-bit		8-bit	
Pin Name	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1	PCLK#2N	PCLK#2N+1
OD0	GND	GND	GND	GND	GND	GND
OD1	GND	GND	GND	GND	GND	GND
OD2	GND	GND	GND	GND	GND	GND
OD3	GND	GND	GND	GND	GND	GND
OD4	C0	Y0	GND	GND	GND	GND
OD5	C1	Y1	GND	GND	GND	GND
OD6	C2	Y2	C0	Y0	GND	GND
OD7	C3	Y3	C1	Y1	GND	GND
OD8	GND	GND	GND	GND	GND	GND
OD9	GND	GND	GND	GND	GND	GND
OD10	GND	GND	GND	GND	GND	GND
OD11	GND	GND	GND	GND	GND	GND
OD12	GND	GND	GND	GND	GND	GND
OD13	GND	GND	GND	GND	GND	GND
OD14	GND	GND	GND	GND	GND	GND
OD15	GND	GND	GND	GND	GND	GND
OD16	C4	Y4	C2	Y2	C0	Y0
OD17	C5	Y5	C3	Y3	C1	Y1
OD18	C6	Y6	C4	Y4	C2	Y2
OD19	C7	Y7	C5	Y5	C3	Y3
OD20	C8	Y8	C6	Y6	C4	Y4
OD21	C9	Y9	C7	Y7	C5	Y5
OD22	C10	Y10	C8	Y8	C6	Y6
OD23	C11	Y11	C9	Y9	C7	Y7
OD24	GND	GND	GND	GND	GND	GND
OD25	GND	GND	GND	GND	GND	GND
OD26	GND	GND	GND	GND	GND	GND
OD27	GND	GND	GND	GND	GND	GND
OD28	GND	GND	GND	GND	GND	GND
OD29	GND	GND	GND	GND	GND	GND
OD30	GND	GND	GND	GND	GND	GND
OD31	GND	GND	GND	GND	GND	GND
OD32	GND	GND	GND	GND	GND	GND
OD33	GND	GND	GND	GND	GND	GND
OD34	GND	GND	GND	GND	GND	GND
OD35	GND	GND	GND	GND	GND	GND
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 7. Mappings of CCIR-656 + separate syncs

This format is not specified by CCIR-656. It's simply the previously mentioned CCIR-656 format plus separate syncs. This format is only valid for single pixel mode. Figure 15 and Figure 16 give two examples

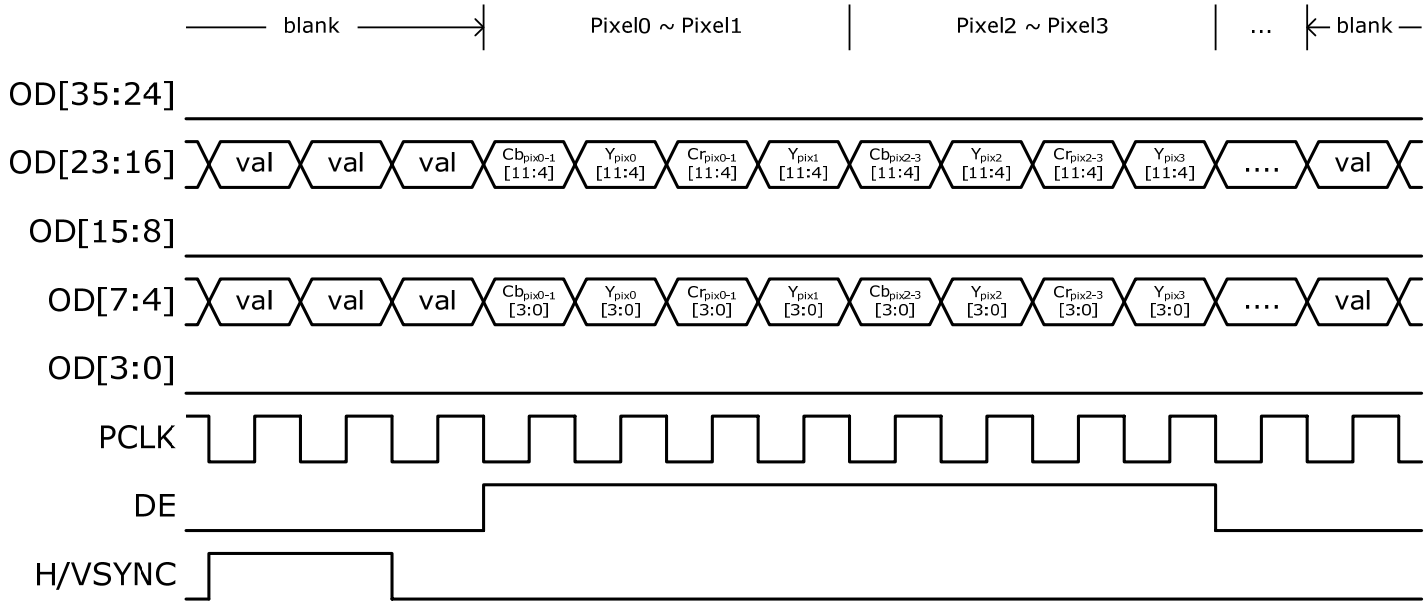


Figure 15. 12-bit CCIR-656 + separate syncs

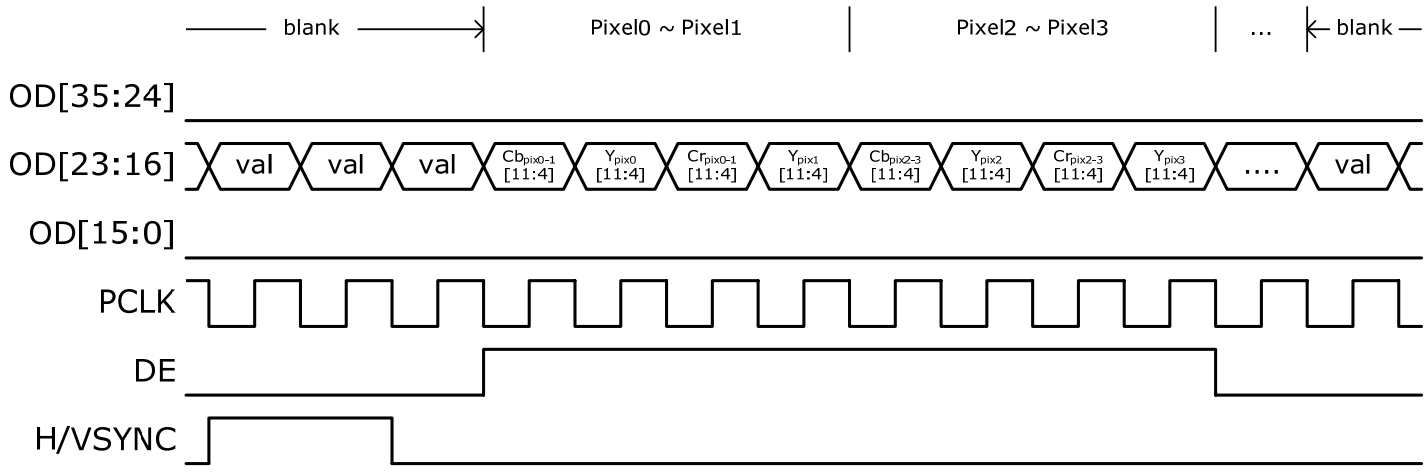


Figure 16. 8-bit CCIR-656 + separate syncs

Supported Input Video Timing

The maximum video timing supported by IT6505 with various input formats are listed in Table 8.

Color Space	Video Format	Bus Width	Maximum Input Clock Frequency (MHz)	Clocking	Maximum Supported Video Timing
RGB YCbCr	4:4:4	18/24/30/36 Single-Pixel	225	1X	VESA 1792x1344P60
		36/48/60/72 Dual-Pixel	135	1X	VESA 2560x1600RB60 (WQXGA)
		12/15/18 Half-Bus Mode	165	Dual-edged	VESA 1600x1200P60 (UXGA)
YCbCr	4:2:2	16/20/24 16-Bit YCbCr	225	1X	VESA 1792x1344P60
		8/10/12 8-Bit CCIR656	225	2X	VESA 1280x1024P60 (SXGA)

Table 8. Input video formats supported by the IT6505

Audio Data Capture and Processing

The IT6505 supports all audio formats specified by the IEC 609580-3/4 and IEC61937 through I^2S and S/PDIF interfaces.

I^2S

Four I^2S inputs are provided to support 8-channel uncompressed audio data at up to 192kHz sample rate. If the input audio data come with a multiple (master) clock, pin 26 (MCLK) takes in the clock to facilitate audio processing. Note that this is optional. By default IT6505 generates the MCLK internally to process the audio. Neither I^2S nor S/PDIF inputs requires MCLK input, coherent or not. However, when using S/PDIF interface, MCLK from external audio source is preferred to prevent the issue caused by the non-balanced duty cycle of the S/PDIF signal. Such configuration could be enabled through register setting. Refer to IT6505 Programming Guide for such setting. The supported multiplied factor and sample frequency as well as the resultant MCLK frequencies are summarized in Table 9.

S/PDIF

The S/PDIF input supports 2-channel uncompressed PCM data (IEC 60958) or compressed multi-channel data (IEC 61937) at up to 192kHz. By default the clock of S/PDIF is carried within the data stream itself via coding. The IT6505 could also process the S/PDIF audio with coherent MCLK

input as indicated in Table 9.

Multiple of audio sample frequency	Audio sample frequency						
	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
128	4.096	5.645	6.144	11.290	12.288	22.579	24.576
256	8.192	11.290	12.288	22.579	24.576	45.158	49.152
512	16.384	22.579	24.576	45.158	49.152	90.317	98.304
1024	32.768	45.158	49.152	90.316	98.304	180.634	196.608

Table 9. Input MCLK frequencies (MHz) supported by the IT6505

Audio Downsampling

Audio data can be down sampled in cases where the sinks only support audio with lower sampling rates. The IT6505 offers audio down-sampling of both a factor of two and a factor of four. Refer to Table 10 for supported down-samplings.

Down-sampling factor of 2	192kHz → 96kHz	176.4kHz → 88.2kHz
	96kHz → 48kHz	88.2kHz → 44.1kHz
Down-sampling factor of 4	192kHz → 48kHz	176.4kHz → 44.1kHz

Table 10. Audio down-samplings supported by the IT6505

Interrupt Generation

The system micro-controller should monitor the interrupt output by the IT6505 at PIN 75 (INT). The IT6505 generates an interrupt signal with events involving various situations. This interrupt pin can be configured as push-pull or open-drain I/O with active high or active low. Please refer to the IT6505 Programming Guide to make use of theses interrupt events.

Configuration and Function Control

The IT6505 includes one serial programming port by default (i.e. with embedded HDCP keys) for interfacing with micro-controller. This port is a slave interface, comprising PCSCL (Pin 73) and PCSDA (Pin 73). The micro-controller uses this interface to monitor all the statuses and control all the functions. Two device addresses are available, depending on the input logic level of PCADR (Pin 72). If PCADR is pulled high by the user, the device address is **0xBA**. If pulled low, **0xB8**.

The IT6505 allows the user to access DisplayPort AUX channel through serial programming port. It can be used for accessing EDID or DPCD data on Sink side. For temporarily storing the acquired

EDID data, the IT6505 embedded a dedicated FIFO of 16 bytes. The micro-controller may command the IT6505 to acquire 16 bytes of EDID information at a time, read them back and then continue to read the next 16 bytes until all necessary EDID information are retrieved.

The HDCP protocol of the IT6505 is completely implemented in hardware. No software intervention is needed except for revocation list checking. Various HDCP-related statuses are stored in HDCP registers for the reference of micro-controller. Refer to IT6505 Programming Guide for detailed register descriptions.

The serial programming interface conforms to standard I^2C transactions and operates at up to 100kHz.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	-0.3		2.5	V
OVDD	I/O pins supply voltage	-0.3		4.0	V
AVCC	DispalyPort analog frontend supply voltage	-0.3		2.5	V
PVCC0	DispalyPort core PLL supply voltage	-0.3		2.5	V
PVCC1	DispalyPort core PLL supply voltage	-0.3		2.5	V
PVCC2	Filter PLL supply voltage	-0.3		2.5	V
XVCC18	Oscillator supply voltage	-0.3		2.5	V
V_I	Input voltage	-0.3		OVDD+0.3	V
V_O	Output voltage	-0.3		OVDD+0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.
2. Refer to Functional Operation Conditions for normal operation.

Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD	Core logic supply voltage	1.62	1.8	1.98	V
OVDD	I/O pins supply voltage	2.97	3.3	3.63	V
AVCC	DispalyPort analog frontend supply voltage	1.71	1.8	1.89	V
PVCC0	DispalyPort core PLL supply voltage	1.62	1.8	1.98	V
PVCC1	DispalyPort core PLL supply voltage	1.62	1.8	1.98	V
PVCC2	Filter PLL supply voltage	1.62	1.8	1.98	V
XVCC18	Oscillator supply voltage	1.62	1.8	1.98	V
$V_{CCNOISE}$	Supply noise			100	mV_{pp}
T_A	Ambient temperature	0	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance				°C/W

Notes:
1. AVCC, PVCC0, PVCC1 and PVCC2 should be regulated.
2. See System Design Consideration for supply decoupling and regulation.

Operation Supply Current Specification

Symbol	Video Timing (VESA)	PCLK (MHz)	4-Lane High Bit Rate			2-Lane High Bit Rate			1-Lane High Bit Rate			Pwr Dn	Unit
			Max	Typ	Min	Max	Typ	Min	Max	Typ	Min		
I_{IVDD}	640x480P60 (VGA)	25.2	166.9	150.8	132.8	163.6	145.6	127.8	161.9	144.3	125.4	0.60	mA
	800x600P60 (SVGA)	40	180.8	166.9	144.5	174.8	155.5	137.4	173.1	154.2	135.4	0.90	mA
	1024x768P60 (XGA)	65	201.8	179.9	160.7	196.2	177	157	194.5	181.2	156.2	1.10	mA
	1280x1024P60 (SXGA)	108	242.5	216.2	192.6	237.5	215.2	187.9				1.70	mA
	1600x1200P60 (UXGA)	162	290.7	262.9	230.8	285.8	260.1	229.5				2.20	mA
	1792x1344P60	204.75	328.9	298.7	262.1							3.00	mA
	2560x1600RB60 (WQXGA)	268.5	369.6	335.4	294.4							4.00	mA
I_{OVDD}	640x480P60 (VGA)	25.2	0.3	0.3	0.0	0.3	0.3	0.0	0.3	0.3	0.0	NA	mA
	800x600P60 (SVGA)	40	0.4	0.3	0.1	0.4	0.3	0.1	0.4	0.3	0.1	NA	mA
	1024x768P60 (XGA)	65	0.4	0.4	0.1	0.4	0.4	0.1	0.4	0.4	0.1	NA	mA
	1280x1024P60 (SXGA)	108	0.5	0.4	0.2	0.5	0.4	0.2				NA	mA
	1600x1200P60 (UXGA)	162	0.6	0.5	0.2	0.6	0.5	0.2				NA	mA
	1792x1344P60	204.75	0.7	0.6	0.2							NA	mA
	2560x1600RB60 (WQXGA)	268.5	0.7	0.5	0.2							NA	mA
I_{AVCC}	640x480P60 (VGA)	25.2	138.1	132.7	123.6	86.6	81.9	76.9	58.1	54.5	51.3	NA	mA
	800x600P60 (SVGA)	40	138.1	132.7	123.6	86.6	81.9	76.9	58.1	54.5	51.3	NA	mA
	1024x768P60 (XGA)	65	138.1	132.7	123.6	86.6	81.9	76.9	58.1	54.5	51.3	NA	mA
	1280x1024P60 (SXGA)	108	138.1	132.7	123.6	86.6	81.9	76.9				NA	mA
	1600x1200P60 (UXGA)	162	138.1	132.7	123.6	86.6	81.9	76.9				NA	mA
	1792x1344P60	204.75	138.1	132.7	123.6							NA	mA
	2560x1600RB60 (WQXGA)	268.5	138.1	132.7	123.6							NA	mA
I_{PVCC0}	640x480P60 (VGA)	25.2	11.1	10.4	9.8	11.1	10.4	9.8	11.1	10.4	9.8	0.10	mA
	800x600P60 (SVGA)	40	11.1	10.4	9.8	11.1	10.4	9.8	11.1	10.4	9.8	0.10	mA
	1024x768P60 (XGA)	65	11.1	10.4	9.8	11.1	10.4	9.8	11.1	10.4	9.8	0.10	mA
	1280x1024P60 (SXGA)	108	11.1	10.4	9.8	11.1	10.4	9.8				0.10	mA
	1600x1200P60 (UXGA)	162	11.1	10.4	9.8	11.1	10.4	9.8				0.10	mA
	1792x1344P60	204.75	11.1	10.4	9.8							0.10	mA
	2560x1600RB60 (WQXGA)	268.5	11.1	10.4	9.8							0.10	mA
I_{PVCC1}	640x480P60 (VGA)	25.2	11.8	11.1	10.3	11.8	11.1	10.3	11.8	11.1	10.3	0.03	mA
	800x600P60 (SVGA)	40	11.8	11.1	10.3	11.8	11.1	10.3	11.8	11.1	10.3	0.03	mA
	1024x768P60 (XGA)	65	11.8	11.1	10.3	11.8	11.1	10.3	11.8	11.1	10.3	0.03	mA
	1280x1024P60 (SXGA)	108	11.8	11.1	10.3	11.8	11.1	10.3				0.03	mA
	1600x1200P60 (UXGA)	162	11.8	11.1	10.3	11.8	11.1	10.3				0.03	mA

	1792x1344P60	204.75	11.8	11.1	10.3							0.03	mA
	2560x1600RB60 (WQXGA)	268.5	11.8	11.1	10.3							0.03	mA
I_{PVCC2}	640x480P60 (VGA)	25.2	1.9	1.7	1.5	1.9	1.7	1.5	1.9	1.7	1.5	0.07	mA
	800x600P60 (SVGA)	40	2.0	1.7	1.5	2.0	1.7	1.5	2.0	1.7	1.5	0.09	mA
	1024x768P60 (XGA)	65	2.0	1.8	1.6	2.0	1.8	1.6	2.0	1.8	1.6	0.14	mA
	1280x1024P60 (SXGA)	108	2.1	1.8	1.6	2.1	1.8	1.6				0.21	mA
	1600x1200P60 (UXGA)	162	2.1	1.9	1.7	2.1	1.9	1.7				0.31	mA
	1792x1344P60	204.75	2.2	2.0	1.7							0.38	mA
	2560x1600RB60 (WQXGA)	268.5	2.4	2.1	1.8							0.49	mA
I_{XVCC18}	640x480P60 (VGA)	25.2	0.7	0.6	0.5	0.7	0.6	0.5	0.7	0.6	0.5	0.58	mA
	800x600P60 (SVGA)	40	0.7	0.6	0.5	0.7	0.6	0.5	0.7	0.6	0.5	0.58	mA
	1024x768P60 (XGA)	65	0.7	0.6	0.5	0.7	0.6	0.5	0.7	0.6	0.5	0.58	mA
	1280x1024P60 (SXGA)	108	0.7	0.6	0.5	0.7	0.6	0.5				0.58	mA
	1600x1200P60 (UXGA)	162	0.7	0.6	0.5	0.7	0.6	0.5				0.58	mA
	1792x1344P60	204.75	0.7	0.6	0.5							0.58	mA
	2560x1600RB60 (WQXGA)	268.5	0.7	0.6	0.5							0.58	mA
PW_{TOTAL}	640x480P60 (VGA)	25.2	643.3	597.6	540.4	539.4	491.4	442.3	482.1	437.0	389.2	2.47	mW
	800x600P60 (SVGA)	40	670.9	629.6	564.0	561.7	511.1	461.6	504.4	456.7	409.3	3.05	mW
	1024x768P60 (XGA)	65	712.9	655.6	596.2	604.4	554.0	500.6	547.2	510.5	450.7	3.50	mW
	1280x1024P60 (SXGA)	108	793.9	727.9	659.6	686.7	630.0	562.0				4.71	mW
	1600x1200P60 (UXGA)	162	889.9	820.9	735.7	782.9	719.4	644.8				5.78	mW
	1792x1344P60	204.75	966.0	892.1	797.7							7.36	mW
	2560x1600RB60 (WQXGA)	268.5	1046.6	964.8	861.6							9.35	mW

Symbol	Video Timing (VESA)	PCLK (MHz)	4-Lane Reduce Bit Rate			2-Lane Reduce Bit Rate			1-Lane Reduce Bit Rate			Pwr Dn	Unit
			Max	Typ	Min	Max	Typ	Min	Max	Typ	Min		
I_{IVDD}	640x480P60 (VGA)	25.2	117.6	105.2	93.2	113.8	102.5	90.9	112.9	101.8	90.1	0.60	mA
	800x600P60 (SVGA)	40	132.7	119.2	105.6	129.2	116.2	102.1	127.3	105.1	101.1	0.90	mA
	1024x768P60 (XGA)	65	156.2	140.9	124.5	154.3	138.9	123.1				1.10	mA
	1280x1024P60 (SXGA)	108	199.4	178.9	158.2	196.9	176.4	156.1				1.70	mA
	1600x1200P60 (UXGA)	162	249.6	225.9	199.5							2.20	mA
	1792x1344P60	204.75	291.3	260.9	228.8							3.00	mA
	2560x1600RB60 (WQXGA)	268.5										4.00	mA
I_{OVDD}	640x480P60 (VGA)	25.2	0.3	0.2	0.1	0.3	0.2	0.1	0.3	0.2	0.1	NA	mA
	800x600P60 (SVGA)	40	0.3	0.3	0.1	0.3	0.3	0.1	0.3	0.3	0.1	NA	mA
	1024x768P60 (XGA)	65	0.4	0.3	0.1	0.4	0.3	0.1				NA	mA
	1280x1024P60 (SXGA)	108	0.5	0.4	0.1	0.5	0.4	0.1				NA	mA
	1600x1200P60 (UXGA)	162	0.6	0.5	0.2							NA	mA
	1792x1344P60	204.75	0.7	0.5	0.2							NA	mA
	2560x1600RB60 (WQXGA)	268.5										NA	mA
I_{AVCC}	640x480P60 (VGA)	25.2	128.2	121.8	115.3	79.2	75.7	71.0	52.6	49.5	46.8	NA	mA
	800x600P60 (SVGA)	40	128.2	121.8	115.3	79.2	75.7	71.0	52.6	49.5	46.8	NA	mA
	1024x768P60 (XGA)	65	128.2	121.8	115.3	79.2	75.7	71.0				NA	mA
	1280x1024P60 (SXGA)	108	128.2	121.8	115.3	79.2	75.7	71.0				NA	mA
	1600x1200P60 (UXGA)	162	128.2	121.8	115.3							NA	mA
	1792x1344P60	204.75	128.2	121.8	115.3							NA	mA
	2560x1600RB60 (WQXGA)	268.5										NA	mA
I_{PVCC0}	640x480P60 (VGA)	25.2	11.0	10.4	9.8	11.0	10.4	9.8	11.0	10.4	9.8	0.10	mA
	800x600P60 (SVGA)	40	11.0	10.4	9.8	11.0	10.4	9.8	11.0	10.4	9.8	0.10	mA
	1024x768P60 (XGA)	65	11.0	10.4	9.8	11.0	10.4	9.8				0.10	mA
	1280x1024P60 (SXGA)	108	11.0	10.4	9.8	11.0	10.4	9.8				0.10	mA
	1600x1200P60 (UXGA)	162	11.0	10.4	9.8							0.10	mA
	1792x1344P60	204.75	11.0	10.4	9.8							0.10	mA
	2560x1600RB60 (WQXGA)	268.5										0.10	mA
I_{PVCC1}	640x480P60 (VGA)	25.2	6.7	6.3	5.9	6.7	6.3	5.9	6.7	6.3	5.9	0.03	mA
	800x600P60 (SVGA)	40	6.7	6.3	5.9	6.7	6.3	5.9	6.7	6.3	5.9	0.03	mA
	1024x768P60 (XGA)	65	6.7	6.3	5.9	6.7	6.3	5.9				0.03	mA
	1280x1024P60 (SXGA)	108	6.7	6.3	5.9	6.7	6.3	5.9				0.03	mA
	1600x1200P60 (UXGA)	162	6.7	6.3	5.9							0.03	mA
	1792x1344P60	204.75	6.7	6.3	5.9							0.03	mA

	2560x1600RB60 (WQXGA)	268.5										0.03	mA
I_{PVCC2}	640x480P60 (VGA)	25.2	1.6	1.5	1.3	1.6	1.5	1.3	1.6	1.5	1.3	0.07	mA
	800x600P60 (SVGA)	40	1.7	1.5	1.3	1.7	1.5	1.3	1.7	1.5	1.3	0.09	mA
	1024x768P60 (XGA)	65	1.7	1.5	1.3	1.7	1.5	1.3				0.14	mA
	1280x1024P60 (SXGA)	108	1.9	1.6	1.4	1.9	1.6	1.4				0.21	mA
	1600x1200P60 (UXGA)	162	2.0	1.7	1.5							0.31	mA
	1792x1344P60	204.75	2.1	1.9	1.5							0.38	mA
	2560x1600RB60 (WQXGA)	268.5										0.49	mA
I_{XVCC18}	640x480P60 (VGA)	25.2	0.7	0.6	0.5	0.7	0.6	0.5	0.7	0.6	0.5	0.58	mA
	800x600P60 (SVGA)	40	0.7	0.6	0.5	0.7	0.6	0.5	0.7	0.6	0.5	0.58	mA
	1024x768P60 (XGA)	65	0.7	0.6	0.5	0.7	0.6	0.5				0.58	mA
	1280x1024P60 (SXGA)	108	0.7	0.6	0.5	0.7	0.6	0.5				0.58	mA
	1600x1200P60 (UXGA)	162	0.7	0.6	0.5							0.58	mA
	1792x1344P60	204.75	0.7	0.6	0.5							0.58	mA
	2560x1600RB60 (WQXGA)	268.5										0.58	mA
PW_{TOTAL}	640x480P60 (VGA)	25.2	515.8	476.2	437.1	415.6	383.8	348.8	363.6	333.0	301.5	2.47	mW
	800x600P60 (SVGA)	40	545.9	504.1	461.7	446.3	411.0	371.0	392.3	339.7	323.3	3.05	mW
	1024x768P60 (XGA)	65	592.8	547.4	499.2	496.4	456.3	412.7				3.50	mW
	1280x1024P60 (SXGA)	108	679.0	623.0	566.2	581.3	531.0	478.4				4.71	mW
	1600x1200P60 (UXGA)	162	779.0	716.7	648.3							5.78	mW
	1792x1344P60	204.75	862.1	786.5	706.6							7.36	mW
	2560x1600RB60 (WQXGA)	268.5										9.35	mW

Notes:
1. Setup condition: 8-bpc RGB, ColorRamp pattern, 8-channel 192k audio, HDCP off, SSC on
2. Max: OVDD=AVCC33=3.6V, IVDD=AVCC18=PVCC1=PVCC2=1.98V
   Typ: OVDD=AVCC33=3.3V, IVDD=AVCC18=PVCC1=PVCC2=1.8V
   Min: OVDD=AVCC33=3.0V, IVDD=AVCC18=PVCC1=PVCC2=1.62V
3. Table with / means current configuration of DisplayPort bandwidth is not enough to support this video timing.
4. PW_{TOTAL_OP} are calculated by multiplying the supply currents with their corresponding supply voltage and summing up all the items.
5. Measured by FLUKE 187

DC Electrical Specification

Under functional operation conditions

Symbol	Parameter	Pin Type	Conditions	Min.	Typ	Max	Unit
V_{IH}	Input high voltage[1]	LVTTL		2.0			V
V_{IL}	Input low voltage[1]	LVTTL				0.8	V
V_T	Switching threshold[1]	LVTTL			1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage[1]	Schmitt		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]	Schmitt			1.6	2.0	V
V_{OL}	Output low voltage[1]	LVTTL	I_{OL}=2~16mA			0.4	
V_{OH}	Output high voltage[1]	LVTTL	I_{OH}=-2~-16mA	2.4			
I_{IN}	Input leakage current[1]	all	V_{IN}=5.5V or 0		±5		μA
I_{OZ}	Tri-state output leakage current[1]	all	V_{IN}=5.5V or 0		±10		μA
I_{OL}	Serial programming output sink current[2]	Schmitt	V_{OUT}=0.2V	4		16	mA
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level1}$	Differential Peak-to-peak Output Voltage Level 1 [3]	DPTX	R_{EXT}=820Ω	340	400	460	mV
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level2}$	Differential Peak-to-peak Output Voltage Level 2 [3]	DPTX	R_{EXT}=820Ω	510	600	680	mV
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level3}$	Differential Peak-to-peak Output Voltage Level 3 [3]	DPTX	R_{EXT}=820Ω	690	800	920	mV
$V_{TX\text{-}DIFFp\text{-}p\text{-}Level4}$	Differential Peak-to-peak Output Voltage Level 4 [3]	DPTX	R_{EXT}=820Ω	1020	1200	1380	mV

Notes:

1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real serial programming environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of the IT6505 are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to IT6505 Programming Guide for proper register setting.
3. Refer to DisplayPort V1.1a specification.

Audio AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
F_{S_I2S}	I^2S sample rate	Up to 8 channels	32		192	kHz
F_{S_SPDIF}	S/PDIF sample rate	2 channels	32		192	kHz

Video AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
T_{pixel}	PCLK pixel clock period[1]	Single-edged clocking	4.44		40	ns
F_{pixel}	PCLK pixel clock frequency[1]		25		225	MHz
T_{CDE}	PCLK dual-edged clock period[2]	Dual-edged clocking	6.06		40	ns
F_{CDE}	PCLK dual-edged clock frequency[2]		25		165	MHz
T_{PDUTY}	PCLK clock duty cycle		40%		60%	
T_{PJ}	PCLK worst-case jitter				1.5	ns
T_S	Video data setup time[3]	Single-edged clocking		1		ns
T_H	Video data hold time[3]			0.8		ns
T_{SDE}	Video data setup time[3]	Dual-edged clocking		1		ns
T_{HDE}	Video data hold time[3]			0.8		ns

Notes:

1. Fpixel is the inverse of Tpixel. Operating frequency range is given here while the actual video clock frequency should comply with all video timing standards.
2. All setup time and hold time specifications are with respect to the latching edge of PCLK selected by the user through register programming.

System Design Consideration

The IT6505 is a very high-speed interface chip. It takes in TTL signals at up to 166MHz with 72-bit data bus and transmits DisplayPort differential signals at as high as 2.7Gbps. At such speeds any PCB design imperfection could lead to compromised signal integrity and hence degraded performance. To get the optimum performance the system designers should follow the guideline below when designing the application circuits and PCB layout.

1. Pin 65 (PVCC0), Pin 61 (PVCC1) and Pin 63(PVCC2) and AVCC should be supplied with clean power: ferrite-decoupled and capacitively- bypassed, since this is the power for the transmitter PLL, which is crucial in determining the DisplayPort output signal quality. Excess power noise might degrade the system performance.

2. It is highly recommended that all power pins are decoupled to ground pins via capacitors of 0.1uF. Low-ESL capacitors are preferred. Generally these capacitors should be placed on the same side of the PCB with the IT6505 and as close to the pins as possible, preferably within 0.5cm from the pins. It is also recommended that the power and ground traces run relatively short distances and are connected directly to respective power and ground planes through via holes.

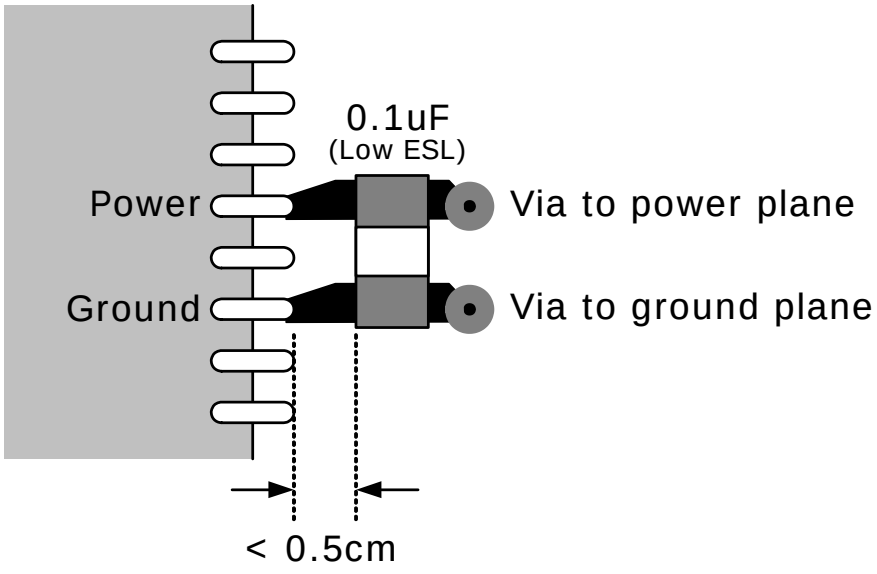


Figure 17. Layout example for decoupling capacitors.

3. The IT6505 supports 72-bit input bus running at as high as 166MHz. To maintain signal integrity and lower EMI, the following guidelines should be followed:

A. Employ **4-layer PCB** design, where a ground or power plane is directly placed under the signal buses at middle layers. The ground and power planes underneath these buses should be continuous in order to provide a solid return path for EM-wave introduced currents.

B. Whenever possible, keep all TTL signal traces on the same layer with the IT6505 and the front-end decoder.
C. TTL input traces from the decoder should be kept as short as possible
D. Depending on the TTL output specifications of the front-end decoder, 33Ω resistors might be placed in series to its output pins. This can slow down the signal rising edges, reduces current spikes and lower the reflections.
E. The PCLK signal should be kept away from other signal traces to avoid crosstalk interference. A general guideline is 2X the dielectric thickness. For example, if the dielectric layer between the signal layer and the immediate power/ground layer is 7 mil, then the PCLK trace should be kept at least 14 mil away from all other signal traces.

4. The impedance of the Source or Sink interconnect should be matched to the impedance of the connector and cable assembly so as to minimize return loss and maximize the transmitted signal. Failure to properly match the impedances will reduce the EYE opening decreasing the allowable Source or Sink interconnect trace length. Protection devices should add no more than 1.5 pF parasitic load to each trace. Series protection resistors are not recommended.
The characteristic impedance of all differential PCB traces should be kept at 100Ω all the way from the DisplayPort connector to the IT6505. This is crucial to the system performance at high speeds. When layouting these differential transmission lines, the following guidelines should be followed:

A. The signals traces should be on the outside layers (TOP layer or BOTTOM layer) while beneath it there should be a continuous ground plane in order to maintain the so-called micro-strip transmission line structure, giving stable and well-defined characteristic impedances.
B. Carefully choose the width and spacing of the differential transmission lines as their characteristic impedance depends on various parameters of the PCB: trace width, trace spacing, copper thickness, dielectric constant, dielectric thickness, etc. Careful 3D EM simulation is the best way to derive a correct dimension that enables a nominal 100Ω differential impedance.
C. Cornering, through holes, crossing and any irregular signal routing should be minimized so as to prevent from disrupting the EM field and creating discontinuity in characteristic impedance.
D. The IT6505 should be placed as close to the DisplayPort connector as possible. As a rule of thumb, the lengths of the DisplayPort differential traces (from the DisplayPort output pins of the IT6505 to the DisplayPort connector) **should be smaller than 5 cm (refer to Figure 18)**, especially for applications that support DisplayPort data rates at 2.7 Gbps. This is because at such high transmission rates, the source-side reflections would seriously impact the output data eyes. Since PCB traces, even when carefully designed, suffer from large impedance variations, it's a must that the reflection route be kept as short as possible.

5. Special care should be taken when adding discrete ESD devices to all differential PCB traces (TX0P/N, TX1P/N, TX2P/N, TX3P/N). The IT6505 is designed to provide ESD protection for up to 2kV at these pins, which is good enough to prevent damages during assembly. To meet the system EMC specification, external discrete ESD diodes might be added. But note that adding discrete ESD diodes inevitably add capacitive loads, therefore degrade the electrical performance at high speeds. If not chosen carefully, these diodes coupled with less-than-optimal layout would degrade the output data eyes, which might fail to pass the SOURCE Data Eye Diagram test in the DisplayPort Compliance Test. One should only use low-capacitance ESD diode to protect these high-speed pins. Commercially available devices such as Semtech's RClamp0524p that take into consideration of all aspects of designing and protecting high-speed transmission lines are recommended.

Notes: DisplayPort Devices implementing this specification may swing the I/O lines as high as ± 0.3V single-ended with respect the common mode bias reference level. The designer must carefully select clamping devices and clamping rail voltages such that ESD devices will not cause clipping of normal signals.

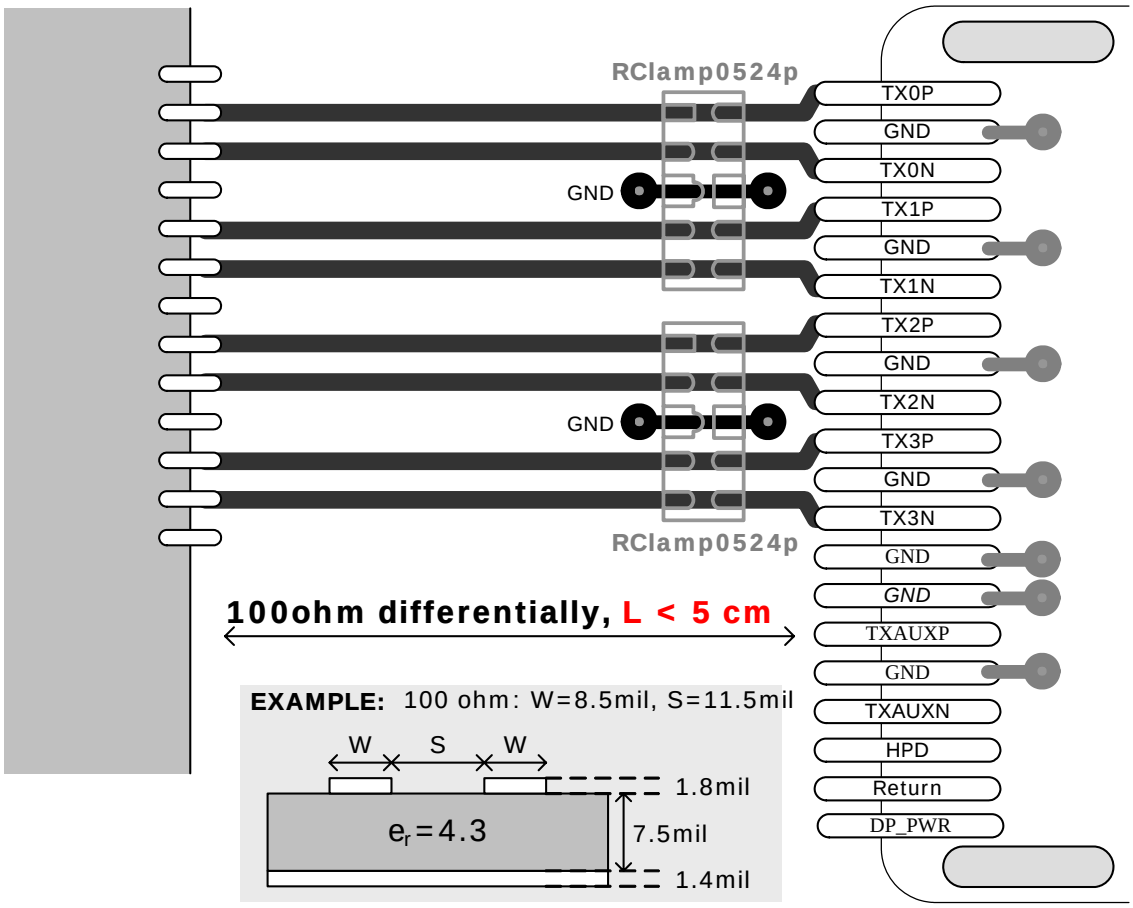
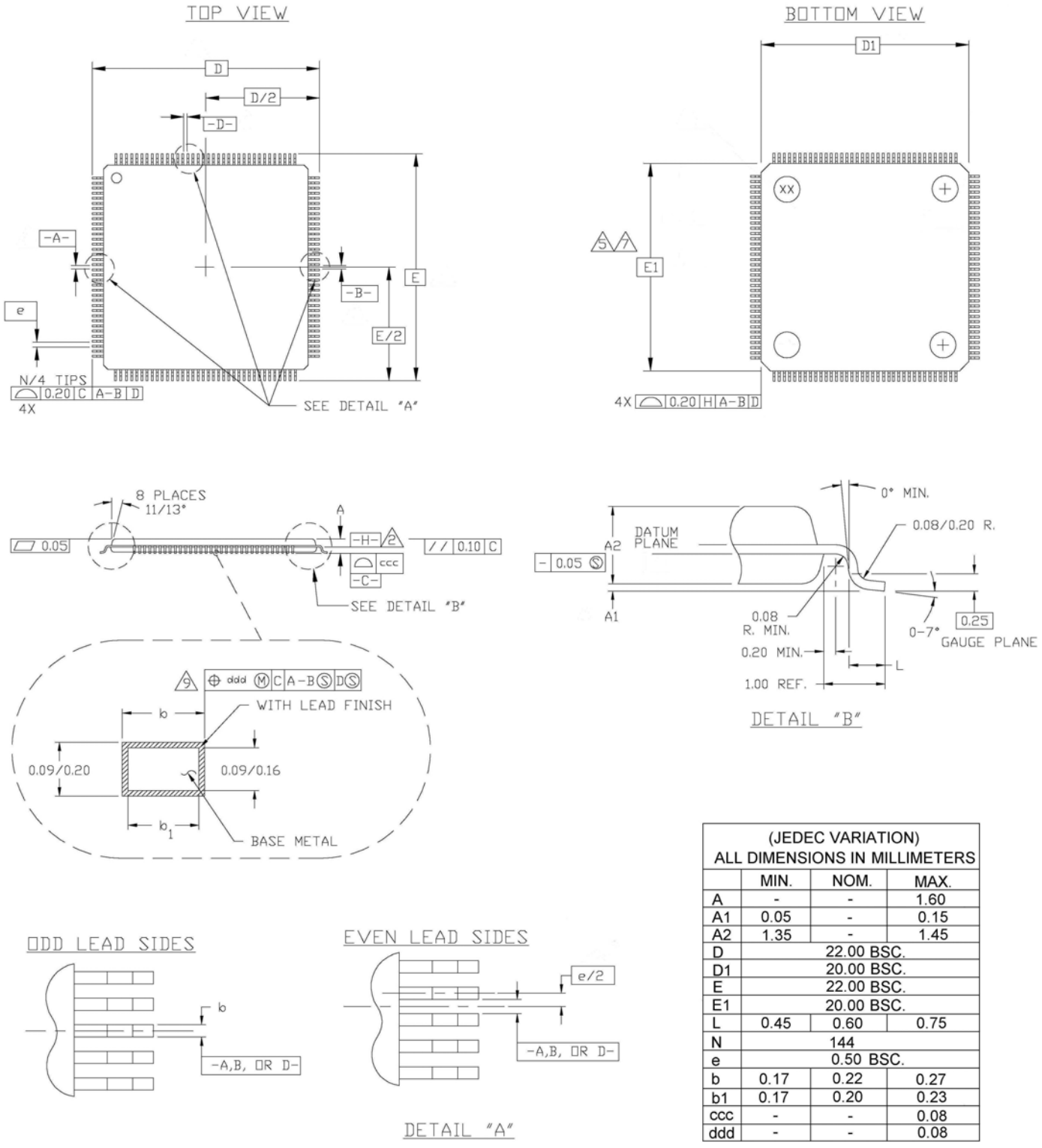


Figure 18. Layout example for high-speed DisplayPort differential signals

6. Pin 59 (REXT) should be connected to AVCC via a 820Ω/1% precision SMD resistor. This resistor is used to calibrate the DisplayPort output current level and should be placed as close as possible to the IT6505.

Package Dimensions



(JEDEC VARIATION) ALL DIMENSIONS IN MILLIMETERS			
	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	-	1.45
D		22.00 BSC.	
D1		20.00 BSC.	
E		22.00 BSC.	
E1		20.00 BSC.	
L	0.45	0.60	0.75
N		144	
e		0.50 BSC.	
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
ccc	-	-	0.08
ddd	-	-	0.08

Figure19. 144-pin LQFP Package Dimensions

Classification Reflow Profiles

Reflow Profile	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3℃/second max.
Preheat -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60-180 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	 217℃ 60-150 seconds
Peak Temperature(Tp)	260 +0 /-5℃
Time within 5 ℃ of actual Peak Temperature(tp)	20-40 seconds
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

Note: All Temperature refer to topside of the package, measured on the package body surface.