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IT8110E

Embedded Controller

Specification V0.2.2

(For C Version)

ITE TECH. INC.

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Revision History

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FIGURES

TABLES

1. Features .

- **8032 Embedded Controller**
  - Twin Turbo version/3-stage pipeline
  - 9.2 MHz for EC domain and 8032 internal timer
  - Variable frequency range to gain the maximum 8032 code-fetch performance
  - Instruction set compatible with standard 8051/2
  - 4K SRAM for code/data space

- **LPC Bus Interface**
  - Compatible with the LPC specification v1.1
  - Supports I/O read/write
  - Supports Memory read/write
  - Supports FWH read/write
  - Serial IRQ
  - Supports LPC 24MHz to 33MHz
  - Supports 3.3V/1.8V level

- **Flash Interface**
  - 128K-byte e-flash (embedded flash)
  - Over 100,000 erase/program cycles
  - Over 10-year data retention
  - Supports 3.3V/1.8V level

- **Crystal-Free**
  - Built-in 32.768 kHz clock generator
  - External crystal oscillator not required

- **SMBus Controller**
  - SMBus spec. 2.0
  - 4 SMBus masters + 2 slaves
  - 4 SMBus channels
  - Compatible with I2C cycles

- **System Wake Up Control**
  - Modem RI# wake up
  - Telephone RING# wake up
  - IRQ/SMI# routing

- **EC Wake Up Control**
  - external/internal wake up events
  - WUI pins

- **Interrupt Controller**
  - interrupt events to EC
  - Fixed priority

- **Timer / Watch Dog Timer**
  - 3 internal 16-bit multi-function timers inside 8032, which is based on EC clock
  - 1 internal WDT inside 8032, which is based on EC clock
  - 1 external 16-bit timer and 1 external 24-bit timer in ETWD module, which are based on 32.768 k clock source
  - 1 external 16-bit WDT in ETWD module, which is based on 32.768 k clock source

- **UART**
  - 1 full duplex UART inside 8032
  - 1 standard serial port (legacy 16C550 COM1/COM2)
    Baud rate up to 460800
  - Receiver/Transmitter can be enabled separately

- **ACPI Power Management Channel**
  - 5 Power management channels
  - Compatible and enhanced mode

- **BRAM**
  - EC registers shared with RTCT SRAM

- **GPIO**
  - Supports 44-port GPIO
  - Programmable pull up/pull down
  - Schmitt trigger for input
  - Supports 19-port 1.8V input level

- **KBC Interface**
  - 8042 style KBC interface
  - Legacy IRQ1 and IRQ12
  - Fast A20G and KB reset

- **ADC**
  - 4 external ADC channels
  - 10-bit resolution (+/- 4LSB)
  - 3 voltage comparators

- **DAC**
  - 1 DAC channel
  - 8-bit DAC

- **PWM**
  - 2 PWM channels
  - Base clock frequency is 32.768 kHz
  - 8 duty cycle resolution
  - 8/16-bit common input clock prescaler
  - 4 prescalers for 8 PWM output used for devices with different frequencies
  - Supports PWM open-drain output
  - Supports two sets tachmetors; each set tachmetor can be switched from two external pins.

- **PECI Host**
  - PECI spec. 2.0/3.0
  - Supports 16-byte write/read length
  - Supports FCS checking mechanism
  - Supports AW_FCS hardwired mechanism
  - Supports adjustable V_{TT} level

- **PS/2 Interface**
  - 1 PS/2 interface
  - Hardware/Software mode selection

- **In-System Programming**
  - ISP via parallel port interface on existing KBS connector
  - Fast flash programming with software provided by ITE

- **Consumer IR**
  - Supports 27-58 KHz, 400-500 KHz device
  - Supports remote power-on switch

- **Power Consumption**
  - Standby with Sleep mode current if Crystal-Free: 45 μA

- **RTCT**
  - Supports 2 alarms

- **Package**
  - LQFP 64

2. General Description

The IT8110 a highly integrated embedded controller with system functions suitable for mobile system applications.

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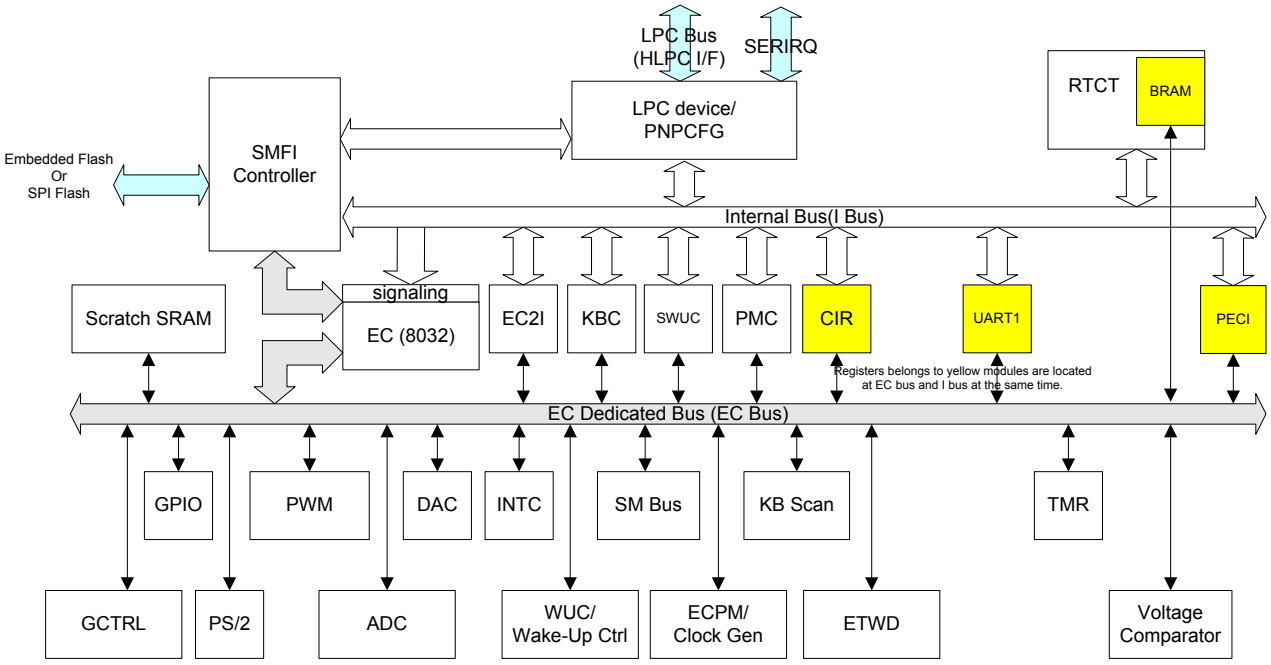
3. System Block Diagram

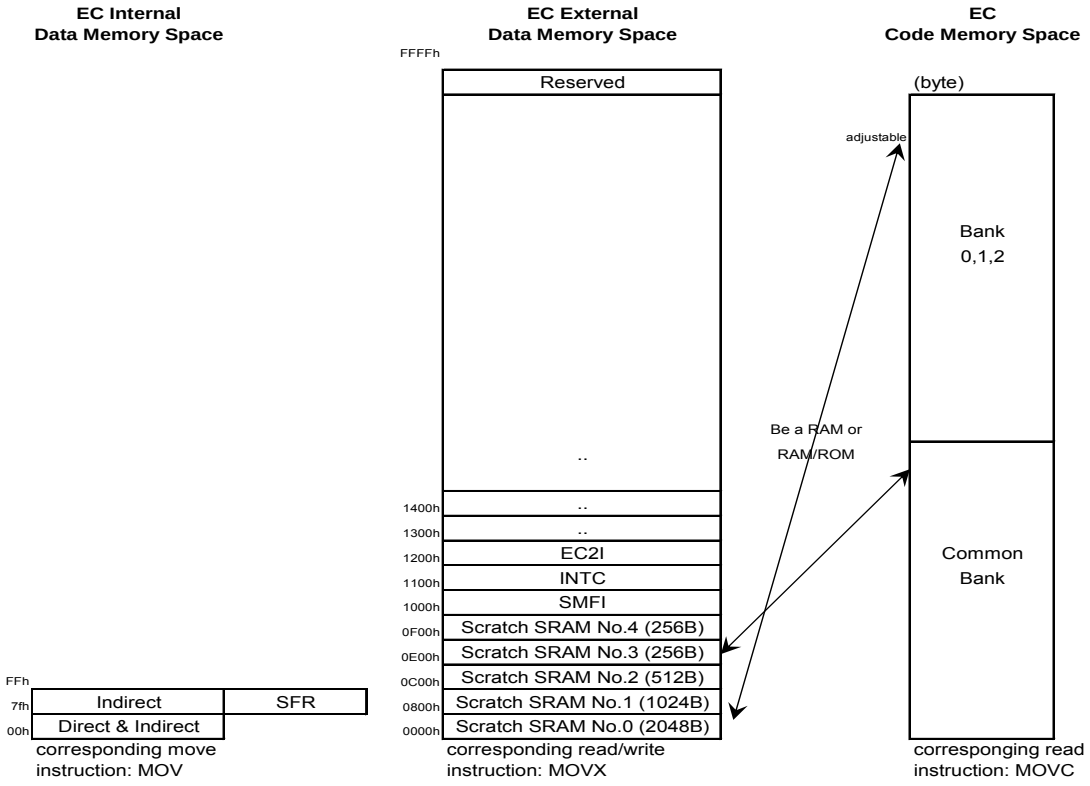
3.1 Block Diagram

IT8110



3.2 EC Mapped Memory Space

Figure 3-1. EC 8032 Data/Code Memory Map



There are five internal Scratch SRAMs No 0-4, which are always mapped into data space and may be mapped into code space if their corresponding code space mapping registers are enabled. It means that Scratch SRAM may be mapped into data and code space at the same time and the firmware on Scratch ROM can access the same Scratch RAM. It is called Scratch RAM when being located at data space (default after reset) and called Scratch ROM when being located at code space.

3.3 Register Abbreviation

The register abbreviations and access rules are listed below:

R	**READ ONLY**. If a register is read only, writing to this register has no effect.
W	**WRITE ONLY**. If a register is write only, reading to this register returns all zero.
R/W	**READ/WRITE**. A register with this attribute can be read and written.
RC	**READ CLEAR**. If a register is read clear, reading to this register clears the register to '0'.
R/WC	**READ/WRITE CLEAR**. A register bit with this attribute can be read and written. However, writing 1 clears the corresponding bit and writing 0 has no effect.

BFNAME@REGNAME	This abbreviation may be shown in figures to represent one bit in a register or one field in a register.

The used radix indicator suffixes in this specification are listed below:
Decimal number: "d" suffix or no suffix
Binary number: "b" suffix
Hexadecimal number: "h" suffix

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4. Pin Configuration

4.1 Top View

IT8110E Top View

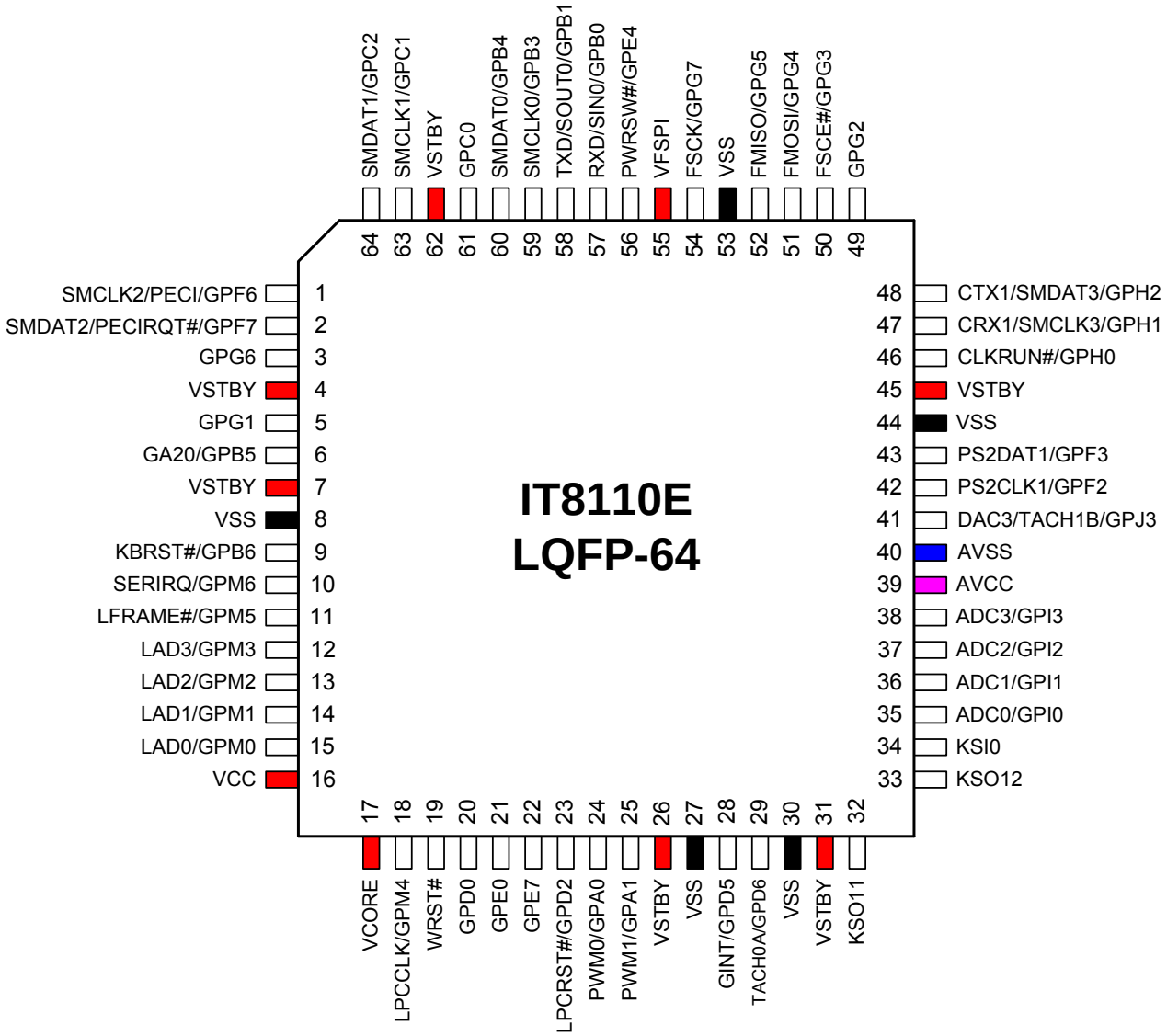

Table 4-1. Pins Listed in Numeric Order (LQFP 64)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	SMCLK2/PECI/GPF6	17	VCORE	33	KSO12	49	GPG2
2	SMDAT2/PECIRQT#/GPF7	18	LPCCLK/GPM4	34	KSI0	50	FSCE#/GPG3
3	GPG6	19	WRST#	35	ADC0/GPI0	51	FMOSI/GPG4
4	VSTBY	20	GPD0	36	ADC1/GPI1	52	FMISO/GPG5
5	GPG1	21	GPE0	37	ADC2/GPI2	53	VSS
6	GA20/GPB5	22	GPE7	38	ADC3/GPI3	54	FSCK/GPG7
7	VSTBY	23	LPCRST#/GPD2	39	AVCC	55	VFSPI
8	VSS	24	PWM0/GPA0	40	AVSS	56	PWRSW#/GPE4
9	KBRST#/GPB6	25	PWM1/GPA1	41	DAC3/TACH1B/GPJ3	57	RXD/SIN0/GPB0
10	SERIRQ/GPM6	26	VSTBY	42	PS2CLK1/GPF2	58	TXD/SOUT0/GPB1
11	LFRAME#/GPM5	27	VSS	43	PS2DAT1/GPF3	59	SMCLK0/GPB3
12	LAD3/GPM3	28	GINT/GPD5	44	VSS	60	SMDAT0/GPB4
13	LAD2/GPM2	29	TACH0A/GPD6	45	VSTBY	61	GPC0
14	LAD1/GPM1	30	VSS	46	CLKRUN#/GPH0	62	VSTBY
15	LAD0/GPM0	31	VSTBY	47	CRX1/SMCLK3/GPH1	63	SMCLK1/GPC1
16	VCC	32	KSO11	48	CTX1/SMDAT3/GPH2	64	SMDAT1/GPC2

5. Pin Description

5.1 Pin Description

Table 5-1. Pin Descriptions of 3.3V/1.8V LPC Bus Interface

Pin(s) No.	Signal	Attribute	Description
LPC Bus Interface (3.3V/1.8V CMOS I/F)			
18	**LPCCLK**	PI	***LPC Clock*** 24MHz to 33MHz clock for LPC domain functions.
12-15	**LAD[3:0]**	PIO	***LPC Address Data***
11	**LFRAME#**	PI	***LPC LFRAME# Signal***
10	**SERIRQ**	PIO	***SERIRQ Signal*** This pin is supplied by VFSPI. VFSPI must be supplied as well if VCC is supplied.

Table 5-2. Pin Descriptions of LPC Bus Interface

Pin(s) No.	Signal	Attribute	Description
LPC Bus Interface (3.3V CMOS I/F)			
23	**LPCRST#**	IK	***LPC Hardware Reset*** LPC hardware reset will reset LPC interface and host side modules. The source is determined by EC side register bit LPCRSTEN. This pin can be omitted if external LPC reset is not required.
46	**CLKRUN#**	IO16	***LPC CLKRUN# Signal***
6	**GA20**	IO2	***Gate A20 Signal*** This is GA20 signal driven by SWUC module.
9	**KBRST#**	IO2	***KB Reset Signal*** This is KBRST# signal driven by SWUC module.
19	**WRST#**	IK	***Warm Reset*** For EC domain function, reset after power up.

Table 5-3. Pin Descriptions of 3.3V/1.8V External Serial Flash Interface (FSPI)

Pin(s) No.	Signal	Attribute	Description
External Serial Flash Interface (3.3V/1.8V CMOS I/F)			
54	**FSCK**	O4	***Serial Flash Clock*** Clock (frequency = FreqPLL) to external serial flash.
50	**FSCE#**	O4	***Serial Flash Chip Enable*** Connected to CE# of serial flash.
51	**FMOSI**	IOK4	***Serial Flash In*** Connected to SI of serial flash.
52	**FMISO**	IOK4	***Serial Flash Out*** Connected to SO of serial flash.

NOTE: Please do not place any pull-up resistor on these FSPI pins to reduce power consumption.

Table 5-4. Pin Descriptions of Keyboard Matrix Scan Interface

Pin(s) No.	Signal	Attribute	Description
KB Matrix Interface (3.3V CMOS I/F)			
33, 32	**KSO12, KSO11**	O8	***Keyboard Scan Output*** Keyboard matrix scan output.
34	**KSI0**	IK	***Keyboard*** Scan Input Keyboard matrix scan input for switch based keyboard.

Table 5-5. Pin Descriptions of SMBus Interface

Pin(s) No.	Signal	Attribute	Description
SMBus Interface (3.3V CMOS I/F)			
1, 63, 59, 47	**SMCLK[2:0], SMCLK3**	IOK4, IOK16	***SMBus CLK*** 4 SMBus interface provided.
2, 64, 60, 48	**SMDAT[2:0], SMDAT3**	IOK4, IOK16	***SMBus Data*** 4 SMBus interface provided.

Table 5-6. Pin Descriptions of PS/2 Interface

Pin(s) No.	Signal	Attribute	Description
PS/2 Interface (3.3V CMOS I/F)			
42	**PS2CLK1**	IOK8	***PS/2 CLK*** 1 sets of PS/2 interface, alternate function of GPIO. PS2CLK1 correspond to channel 2 respectively.
43	**PS2DAT1**	IOK8	***PS/2 Data*** 1 sets of PS/2 interface, alternate function of GPIO. PS2DAT1 correspond to channel 2 respectively.

Table 5-7. Pin Descriptions of PWM Interface

Signal	Pin(s) No.	Attribute	Description
PWM Interface (3.3V CMOS I/F)			
25, 24	**PWM[1:0]**	O8	***Pulse Width Modulation Output*** These are general-purpose PWM signals. PWM0-1 correspond to channel 0-1 respectively.
41, 29	**TACH1B** **TACH0A**	IK	***Tachometer Input*** These are tachometer inputs from external fans. They are used for measuring the external fan speed.

Table 5-8. Pin Descriptions of Serial Port Interface

Pin(s) No.	Signal	Attribute	Description
Serial Port Interface (3.3V CMOS I/F)			
57	**SIN0**	IOK16	***Serial Data Input*** This input receives serial data from the communications link.
58	**SOUT0**	IOK16	***Serial Data Output*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.

Table 5-9. Pin Descriptions of UART Interface

Pin(s) No.	Signal	Attribute	Description
UART Interface (3.3V CMOS I/F)			
58	**TXD**	O	***UART TX Output*** UART TX Output from 8032
57	**RXD**	IK	***UART RX Input*** UART RX Input from 8032

Table 5-10. Pin Descriptions of CIR Interface

Pin(s) No.	Signal	Attribute	Description
CIR Interface (3.3V CMOS I/F)			
48	**CTX1**	IOK16	***CIR TX Output*** Transmission data for CIR interface.
47	**CRX1**	IOK16	***CIR RX Input*** Receive data for CIR interface.

Table 5-11. Pin Descriptions of Platform Environment Control Interface (PECI)

Pin(s) No.	Signal	Attribute	Description
Platform Environment Control Interface Interface (3.3V CMOS I/F)			
1	**PECI**	PECI	***PECI*** This bi-directional pin provides data communication between the PECI host and devices.
2	**PECIRQT#**	O4	***PECI Request*** The PECI request is output to PECI devices. When this pin goes low, it requests the system to make the PECI bus available.

Table 5-12. Pin Descriptions of GPIO Interface

Pin(s) No.	Signal	Attribute	Description
GPIO Interface (3.3V CMOS I/F)			
Refer to Pins List	**GPA[1,0], GPB[6:0], GPC[2:0], GPD[6,5,2,0], GPE[7,4,0], GPF[7,6,3,2], GPG[7:1], GPH[2:0], GPI[3:0], GPJ[3], GPM[6:0]**	IOK	***GPIO Signals*** The GPIO pins are divided into groups. Some GPIO pins have alternative function. **PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG[7:2] (Reserved for hardware strapping)**. GPG2 must be pulled down with an external resistor.

Table 5-13. Pin Descriptions of Hardware Strap

Pin(s) No.	Signal	Attribute	Description
Hardware Strap (3.3V CMOS I/F)			
54, 3, 52, 51, 50, 49, 5	**GPG[7:1]**	IK	These pins are the entry of the test mode.

Table 5-14. Pin Descriptions of ADC Input Interface

Pin(s) No.	Signal	Attribute	Description
ADC Interface (3.3V CMOS I/F)			
38-35	**ADC[3:0]**	AI	***ADC Input/Alternate GPIO*** These 4 ADC inputs can be used as GPIO ports depending on the ADC channels required.

Table 5-15. Pin Descriptions of DAC Output Interface

Pin(s) No.	Signal	Attribute	Description
DAC Interface (3.3V CMOS I/F)			
41	**DAC3**	AO	***DAC Output***

Table 5-16. Pin Descriptions of Power/Ground Signals

Pin(s) No.	Signal	Attribute	Description
Power Ground Signals			
8, 27, 30, 44, 53	**VSS**	I	***Ground*** Digital ground.
16	**VCC**	I	***System Power Supply of 3.3V/1.8V*** The power supply of LPC and related functions, which is main power of system.
4, 7, 26, 31, 45, 62	**VSTBY**	I	***Standby Power Supply of 3.3V*** The power supply of EC domain functions, which is standby power of system.

Pin(s) No.	Signal	Attribute	Description
55	**VFSPI**	I	***Standby Power Supply of 3.3V/1.8V*** This pin supplies the I/O power of FSCK/FSCE#/FMOSI/FMISO/SERIRQ. If the external SPI flash is used, the power level of the flash must be the same as that of the VFSPI pin. The power pin must be supplied as well if VCC is supplied. It's allowed to let {VSTBY,VFSPI}={on,off} and the FSPI I/F must be disabled by the setting in 16B-signature if the EC power-on configuration is {VSTBY,VFSPI}={on,off}.
17	**VCORE**	I/O	***Core Power Bypass*** Internal core power output. External capacitor is required to be connected between this pin and VSS and physically close to this pin. The capacitor type must be low-ESR and MLCC is required.
40	**AVSS**	I	***Analog Ground for Analog Component***
39	**AVCC**	I	***Analog VCC for Analog Component***

Notes: I/O cell types are described below:

I: Input PAD.
AI: Analog Input PAD.
IK: Schmitt Trigger Input PAD.
IKD: Schmitt Trigger Input PAD (integrated one pull-down resistor).
PI: PCI Bus Specified Input PAD.
PIO: PCI Bus Specified Input/Output PAD.
OSCI: Oscillator Input PAD.
AO: Analog Output PAD.
O2: 2 mA Output PAD.
O4: 4 mA Output PAD.
O6: 6 mA Output PAD.
O8: 8 mA Output PAD.
OP: Programmable Driving Strength Output PAD.
UIO: USB 1.1 Bidirectional PAD.
PIO: PCI Bus Specified Bidirectional PAD.
OSCIO: Oscillator Bidirectional PAD.
AIO: Bidirectional Analog PAD.
AIO2: Bidirectional PAD with 2 mA Output and Analog Input PAD.
IOK2: Bidirectional PAD with 2 mA Output and Schmitt Trigger Input PAD.
IOK4: Bidirectional PAD with 4 mA Output and Schmitt Trigger Input PAD.
IOK6: Bidirectional PAD with 6 mA Output and Schmitt Trigger Input PAD.
IOK8: Bidirectional PAD with 8 mA Output and Schmitt Trigger Input PAD.
IOK16: Bidirectional PAD with 16 mA Output and Schmitt Trigger Input PAD.
IOKP: Bidirectional PAD with Programmable Driving Strength Output and Schmitt Trigger Input PAD.

6. DC Characteristics

Operating Conditions

VSTBY ……..... 3.3V±0.15V
VFSPI (3.3V) …….. ..... 3.3V±0.15V
VFSPI (1.8V) …….. ..... 1.8V±0.09V
VCC (3.3V)……..... 3.3V±0.15V
VCC (1.8V)……..... 1.8V±0.09V
AVCC…….. ..... 3.3V±0.05V
Operating Temperature (Ta) .....-25°C to +85°C

Absolute Maximum Ratings

Applied Voltage of VFSPI(1.8V), VCC(1.8V) ……..
..... -0.3V to +2.1V
Applied Voltage of VSTBY, VFSPI(3.3V), VCC(3.3V),
AVCC …….. ..... -0.3V to +3.6V
Input Voltage of 1.8V Interface.... -0.3V to VSUP+0.3V
Input Voltage of 3.3V Interface.... -0.3V to VSUP+0.3V
Input Voltage of 5.0V Interface..... -0.3V to +5.8V
Input Voltage of 1.8V/3.3V .....
Optional Interface .....-0.3V to +3.6V
Storage Temperature .....-40°C to +125°C

Note: VSUP is VCC, VSTBY, VFSPI or AVCC.

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
V_{IL}	Input Low Voltage	—	—	0.8	
V_{IH}	Input High Voltage	2.0	—	—	
V_{IH}	Input High Voltage (5V tolerant pad)	2.0	—	—	
V_{OL}	Output Low Voltage	—	—	0.4	I_{OL}= -2 - -16mA
V_{OH}	Output High Voltage	2.4	—	—	I_{OH}= 2 - 16mA
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	0.8		—	
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage	—		2.0	
I_{IL}	Input leakage Current	-10μA	±1μA	10μA	no pull-up or pull-down
I_{OZ}	Tri-state Leakage Current	-10μA	±1μA	10μA	no pull-up or pull-down
R_{pu}	Input Pull-Up Resistance	40KΩ	75KΩ	190KΩ	V_I= 0V
R_{pd}	Input Pull-Down resistance	40KΩ	75KΩ	190KΩ	V_I= VSUP
Cin	Input Capacitance	—	2.8pF	—	
C_L	Load Capacitance	—	—	10pF	Only for FSPI signals.
Cout	Output Capacitance	2.7pF	—	4.9pF	
Cbld	Bi-directional Buffer	2.7pF	—	4.9pF	

Note : VSUP is VCC (3.3V), VSTBY, VFSPI (3.3V) or AVCC.

1.8V CMOS Interface					
V_{IL}	Input Low Voltage	—	—	0.25*VSUP	
V_{IH}	Input High Voltage	0.75*VSUP	—	—	
V_{IH}	Input High Voltage (3.3V tolerant pad)	0.75*VSUP	—	—	
V_{OL}	Output Low Voltage	—	—	0.4	I_{OL}= -2 - -16mA
V_{OH}	Output High Voltage	0.75*VSUP	—	—	I_{OH}= 2 - 16mA
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	0.25*VSUP		—	
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage	—		0.75*VSUP	
I_{IL}	Input leakage Current	-10μA	±1μA	10μA	no pull-up or pull-down
I_{OZ}	Tri-state Leakage Current	-10μA	±1μA	10μA	no pull-up or pull-down
R_{pu}	Input Pull-Up Resistance	80KΩ	200KΩ	510KΩ	V_I= 0V
R_{pd}	Input Pull-Down resistance	80KΩ	200KΩ	510KΩ	V_I= VSUP
Cin	Input Capacitance	—	2.8pF	—	
C_L	Load Capacitance	—	—	10pF	Only for FSPI signals.
Cout	Output Capacitance	2.7pF	—	4.9pF	
Cbld	Bi-directional Buffer	2.7pF	—	4.9pF	

Note : VSUP is VCC (1.8V), VFSPI (1.8V).

Table 6-1. Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Conditions
3.3V CMOS Interface					
I_{SLEEP}	VSTBY supply current if Crystal-Free	—	45 μA	—	Internal pull is disabled VIL = GND VIH = VSTBY No load

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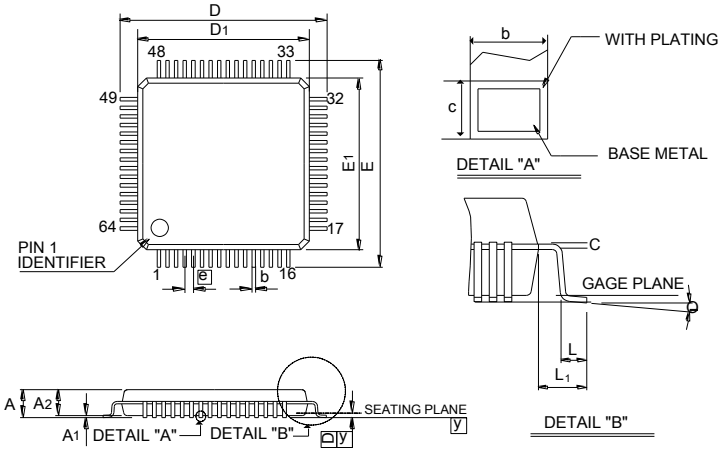
7. Package Information

LQFP 64 Outline Dimensions unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.063	-	-	1.60
A1	0.002	-	0.006	0.05	-	0.15
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.005	0.007	0.009	0.13	0.18	0.23
c	0.004	-	0.008	0.09	-	0.20
D	0.354 BSC			9.00 BSC		
D1	0.276 BSC			7.00 BSC		
E	0.354 BSC			9.00 BSC		
E1	0.276 BSC			7.00 BSC		
e	0.016 BSC			0.40 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	0.039 REF			1.00 REF		
y	-	-	0.004	-	-	0.10
θ	0°	3.5°	7°	0°	3.5°	7°

Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion. But mold mismatch is included.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimension: millimeter
4. Reference Document : JEDEC MS-026

DI-LQFP64(7.0*7.0)v0

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8. Ordering Information

Part No.	Package
IT8110E/CX	LQFP 64

All components provided are RoHS-compliant (100% Green Available).

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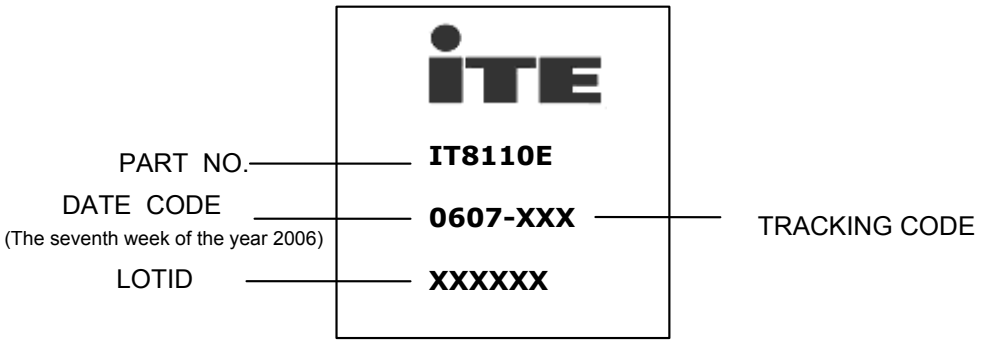
9. Top Marking Information

IT8110E



ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2013)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc.

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Otherwise specified in the order agreed by Seller, delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and by its conditions Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.