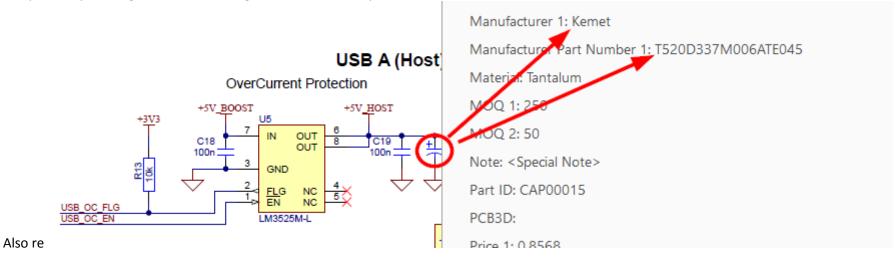
In regard to queries by Chris regarding our ripple problem: I want to restate the problem as succinctly as possible, but still give enough overview for TI engineers to make a proper judgment.

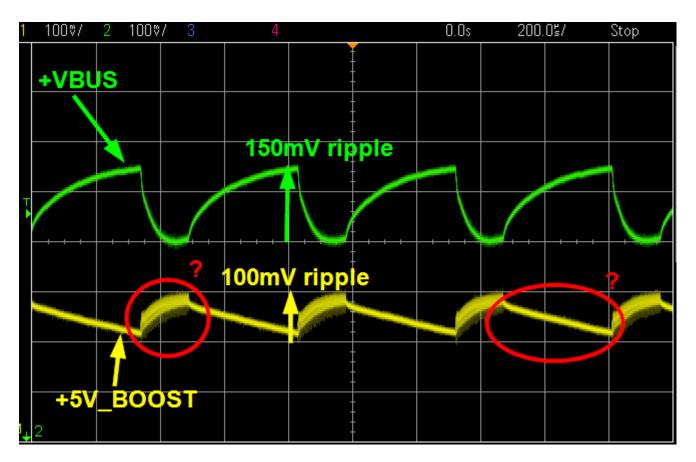
Attached is a schematic overview of our whole TI-based power **system** used to power a Raspberry Pi Compute Module 3 and LCD. If you hover and click on a component, you will get detailed info, e.g. manufacturer and part number:



As one can see, the power sources are +5V USB and/or +4V2 Li-Po battery, which goes to a battery and power-path management system (U1). The output (+VBUS) goes to a +1V8 buck converter (U7), +3V3 buck converter (U4) and +5V boost converter (U2).

The output of the boost converter (+5V_BOOST) goes to a USB power switch (U3: LM3525M-L) with a large 330 uF, low 45mOhm ESR, Tantalum capacitor C3 on the output.

We have found large ripple on the input (+VBUS) and output (+5V_BOOST) of the +5V boost converter if we connect C3 directly (bypassing U1). No load is connected. Unfortunately, the ripple varies from board to board. Here is the worst case:



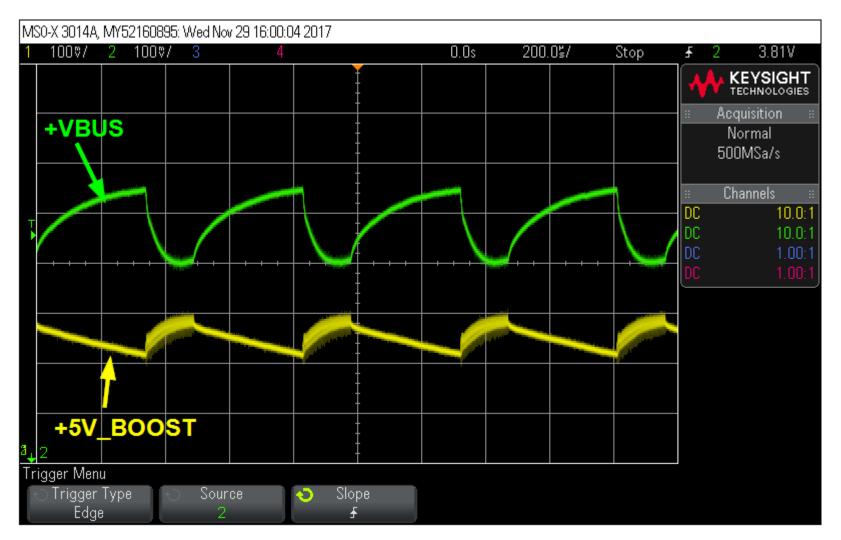
See below four screenshots showing the startup and ripple waveforms for board A and board B.

We have found the following two pieces of info in the boost converter's datasheet regarding the input and output capacitance:

Board_A Startup



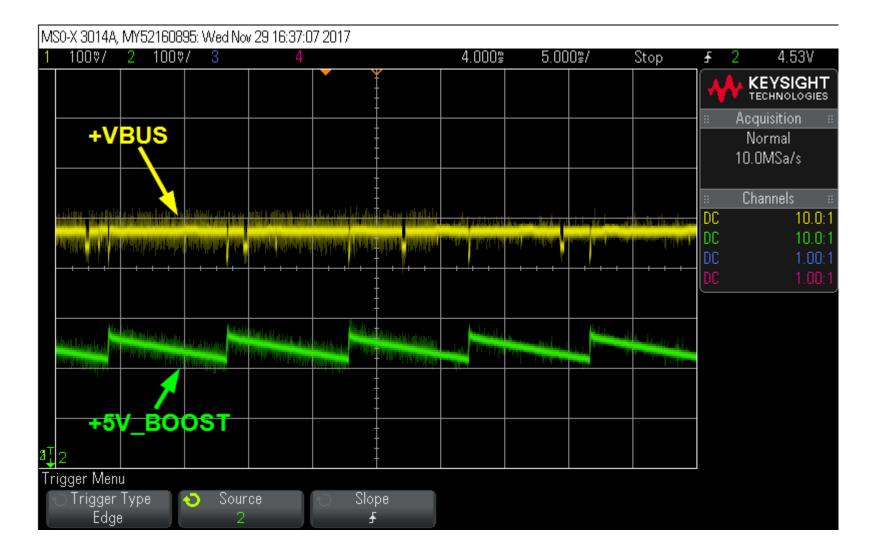
Board_A Ripple

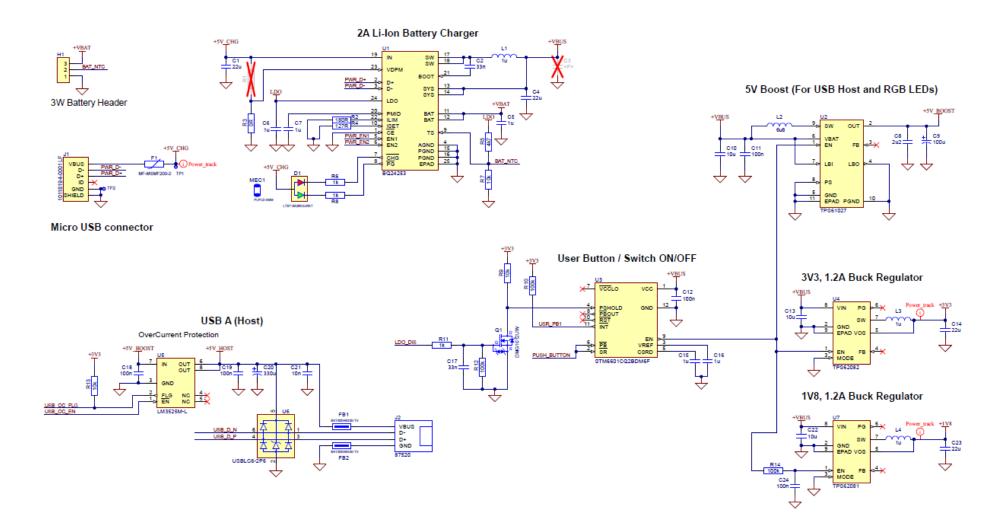


Board_B Startup



Board_B Ripple







TPS61020, TPS61024, TPS61025, TPS61026, TPS61027, TPS61028, TPS61029

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An additional ripple of 16 mV is the result of using a tantalum capacitor with a low ESR of 80 m Ω . The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 26 mV. Additional ripple is caused by load transients. This means that the output capacitor has to completely supply the load during the charging phase of the inductor. A reasonable value of the output capacitance depends on the speed of the load transients and the load current during the load change. With the calculated minimum value of 24 μ F and load transient considerations the recommended output capacitance value is in a 47 to 100 μ F range. For economical reasons, this is usually a tantalum capacitor. Therefore, the control loop has been optimized for using output capacitors with an ESR of above 30 m Ω . Additionally, a ceramic output capacitor of 2.2 μ F must be added in parallel with the tantalum output capacitor.

The device is not designed to operate with ceramic capacitors only, unless a discrete resistor is added in series with them to replicate the required ESR. Large amounts of low ESR capacitance on the output causes instability.

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12 Power Supply Recommendations

This input supply should be well regulated with the rating of TPS6102x. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

We have experimented by making the input capacitance larger, but only at about 220 uF do we start to see a significant difference.

And now for the big questions:

- 1. Can the C-shaped rise and saw-tooth fall waveform of the +5V boost converter output be explained? (no load is connected)
- 2. if we take the voltage drop of the power path management system (U1) into account, is the TPS61027 the right choice for a +5V boost converter, considering it's input requirements and output capacitance ESR requirements?
- 3. Can we fix it by adding low ESR input capacitance? How much?

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