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DEVELOPMENT ASSOCIATION STANDARD

Digital Interface Standards for Monitor
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Table of Contents

1. Overview

1.1 Objective

The objective of this standard is to provide a digital video interface for a display device attached to a video port of a personal computer (PC), work station (WS) and other electronic devices

1.2 Name

This standard is called "Digital Interface Standards for Monitor" (abbreviation : DISM).

1.3 History

In general, a display device with a digital video interface such as a liquid crystal display (LCD) has a fixed pixel format. It is effective to transmit digital data to such devices as it precludes the conversion of digital data to analog data which results in the degradation of display quality. The adoption of a digital format also lowers the system cost as well as simplifies the monitor architecture. At this juncture, the industry does not have any effective standard to achieve the above points. Thus, all the members of DISM are motivated to make a new industry standard, which is widely accepted.

2. Scope of Application

This standard defines signal standards, electrical characteristics, connectors, pin assignments and a digital video interface software specifications for PCs, WSs, display devices and other electronic devices.

3. DISM Overview

3.1 Features

Key features of this standard are as follows.

- High quality video output.
- Plug & Play enabled.
- Capable of using existing technologies.
- Capable of working over cables 10 meters long.
- Low EMI.
- Reduced pin count relative to a parallel interface.

From above point of view, DISM specifies the following three standards.

3.2 Support Signal Form

Digital data	Transition Minimized Differential Signaling (TMDS), Low Voltage Differential Signaling (LVDS), Giga-bit Video Interface (GVIF), Must Support one of the above Transmission Methods
Display Data Channel (DDC)	Mandatory
Signal for VESA “Hot Plugging” (SENS)	Mandatory
Universal Serial Bus (USB)	Optional

Relative to the above transmission methods and the other supported signals, three standards are defined in table 3.1.

Table 3.1 DISM Standards List

	Data Format	Support Signals	Interface Connector	
			Host Side	Monitor Side
Standard 1	TMDS	Digital data DDC, USB	MDR type 26 or 20 pin Connector	MDR type 26 pin Connector
Standard 2a	LVDS	Digital data DDC, USB	MDR type 26 pin Connector	MDR type 26 pin Connector
Standard 2b	LDI	Digital data DDC, USB	MDR type 36 pin Connector	MDR type 36 pin Connector
Standard 3	GVIF	Digital data DDC, USB	MDR type 14 pin Connector	MDR type 14 pin Connector

3.3 Maximum Specifications

3.3.1 Maximum Transmission Specifications

The maximum performance capabilities of the3 standards are as follows.

	Current Status	Future Target
Max. Clock	112MHz	158.4MHz
Max. Resolution	1280x1024	1600x1200
Max. Frame Rate	60Hz	60Hz
Max. Data Bit	24bpp	24bpp

3.3.2 Maximum Transmission Line

Maximum transmission cable length for digital video data is set to 10m. If they are equipped with USB, maximum transmission cable length is set to 5m.

3.4 Referenced Standards

Several standards (see list below) are referenced by DISM.

Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, TIA/EIA-644-1995

VESA Display Data Channel (DDC) Standard, Version 3

VESA Extended Display Identification Data (EDID) Standard, Version 3

Universal Serial Bus Specification, Version 1.0

3.5 Revision History

Digital Interface Standards for Monitor Proposal	Version 0.1p	1998 April 1st
	Version 0.2p	1998 April 23rd
	Version 0.3p	1998 May 7th
	Version E0.3p	1998 June 18th
	Version E0.4p	1998 July 30th
	Version E0.7p	1998 October 5th
	Version E0.9p	1998 October 5th

Version E0.7p : Chapter 6,7,8,9 equal Version E0.4

4. Definition of Terms

Host : Devices which have DISPLAY SIGNAL OUTPUT

Monitor : Image display devices which are connected to HOST devices

Video port : External interface to out put the display data and display control signal

5. Data Transmission Standard 1 : TMDS

5.1 Introduction

Data Transmission Standard 1 specifies an Interface between a Host PC and a Digital monitor. In this standard, TMDS (Transition Minimized Differential Signaling) Standard developed by Silicon Image Inc., is adopted as the digital video data transmission method, and as for the connectors, the MDR (Mini-D Ribbon) connector by 3M Ltd., or it's compatible products are applied.

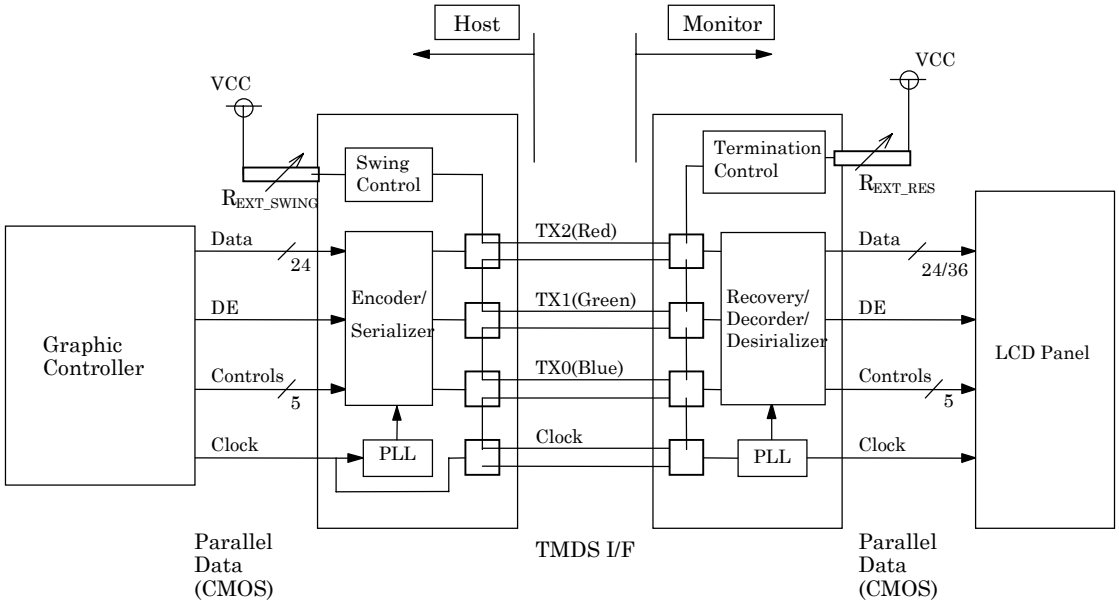
5.2 TMDS Overview

5.2.1 Architecture

TMDS technology using four channel transmission lines is composed of three channel video data transmission lines (Red, Green and Blue) and one channel clock transmission line. High speed video data transmission lines can transmit the data at a speed of f_{ck}x10[bps] (f_{ck} is display clock frequency) per channel. For example, if f_{ck} is 65[MHz], the transmission capability is 650[Mbps]. 8 bit color video data and synchronization signals (or 2 bit control signals) are serialized and transmitted through these high speed transmission lines.

Transmitter encodes the data to transition controlled and DC balanced data. Receiver over-samples the data three times in each transmission line individually, and re-synchronizes them with the display clock.

Figure 5.1 Block Diagram of TMDS



5.2.2 Transmission Line

Serial signal of each transmission line is a single-ended differential signal, and is composed of two data lines and one return ground line.

Termination resistance of receiver can be controlled by external resistor R_{EXT_RES}.

Output current of transmitter can be controlled by external resistor R_{EXT_SWING}, and input voltage amplitude of receiver can be controlled by controlling this output current.

Figure 5.2 Transmission Line

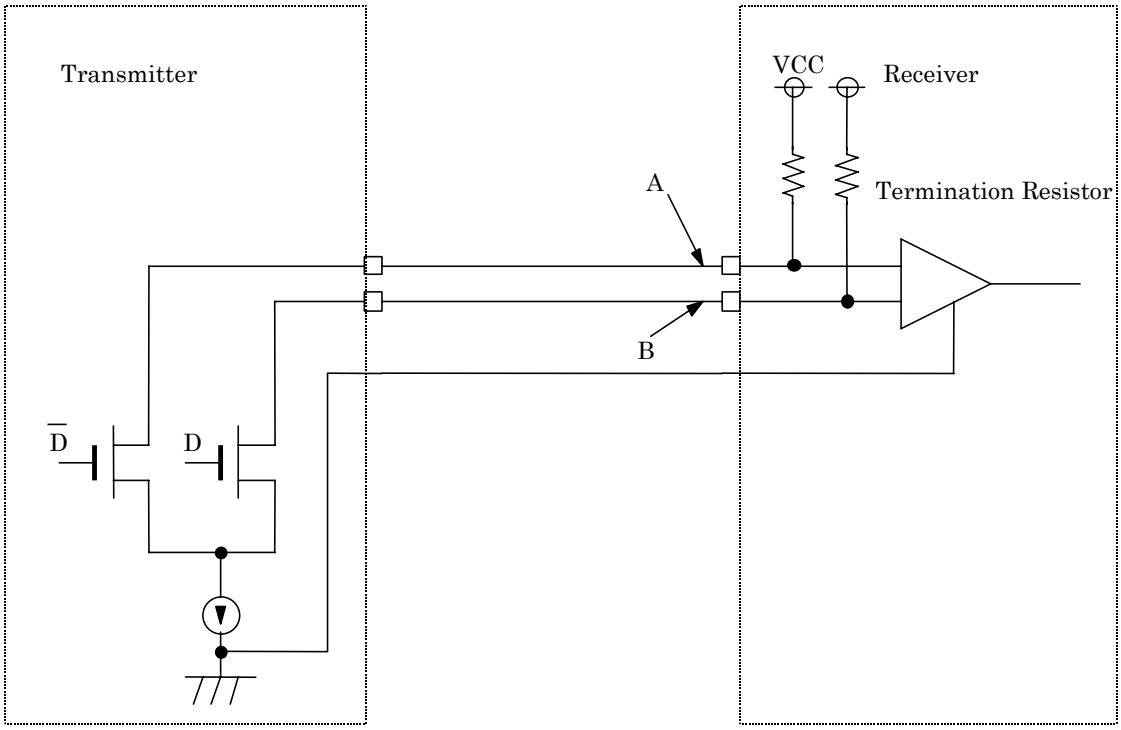
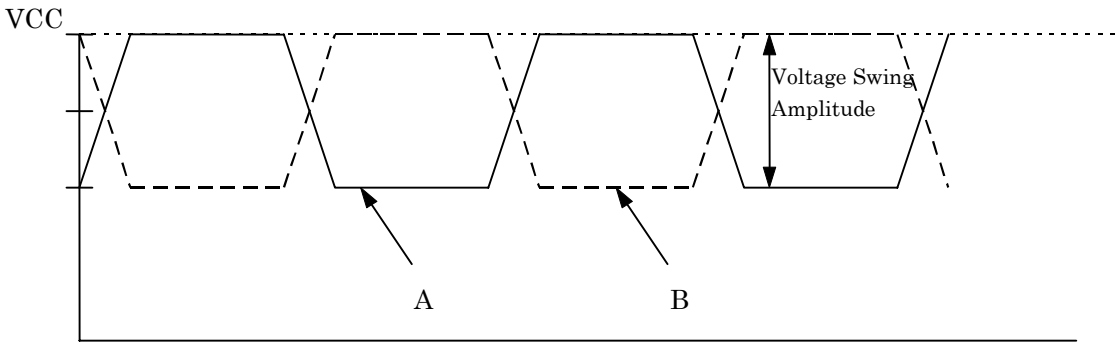


Figure 5.3 Differential Voltage Amplitude



5.2.3 Variation

Standard 1 defines the following two standards depending on the connector type.

(1) 26 pins

This standard adopts 26 pin MDR type connector, and supports video data, USB signal and DDC signal.

(2) 20 pins

This standard adopts 20 pin MDR type connector, and supports video data and DDC signal, but not a USB signal.

5.3 Electrical Characteristics

5.3.1 DC Electrical Specifications

(1) Transmitter

Table 5.1 TMDS Transmitter DC Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Differential Output Voltage Amplitude	V_{OD}	R_{LOAD}=50Ω,	450	500	550	mV
High-level Output Voltage	V_{DOH}			VCC		V
Output Short Circuit Current	I_{OS}	V_{OUT}=0V			5	uA

(2) Receiver

Table 5.2 TMDS Receiver DC Specification

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Differential Input Voltage Amplitude	V_{ID}		200	500	800	mV

5.3.2 AC Electrical Specifications

Figure 5.4 AC Timing

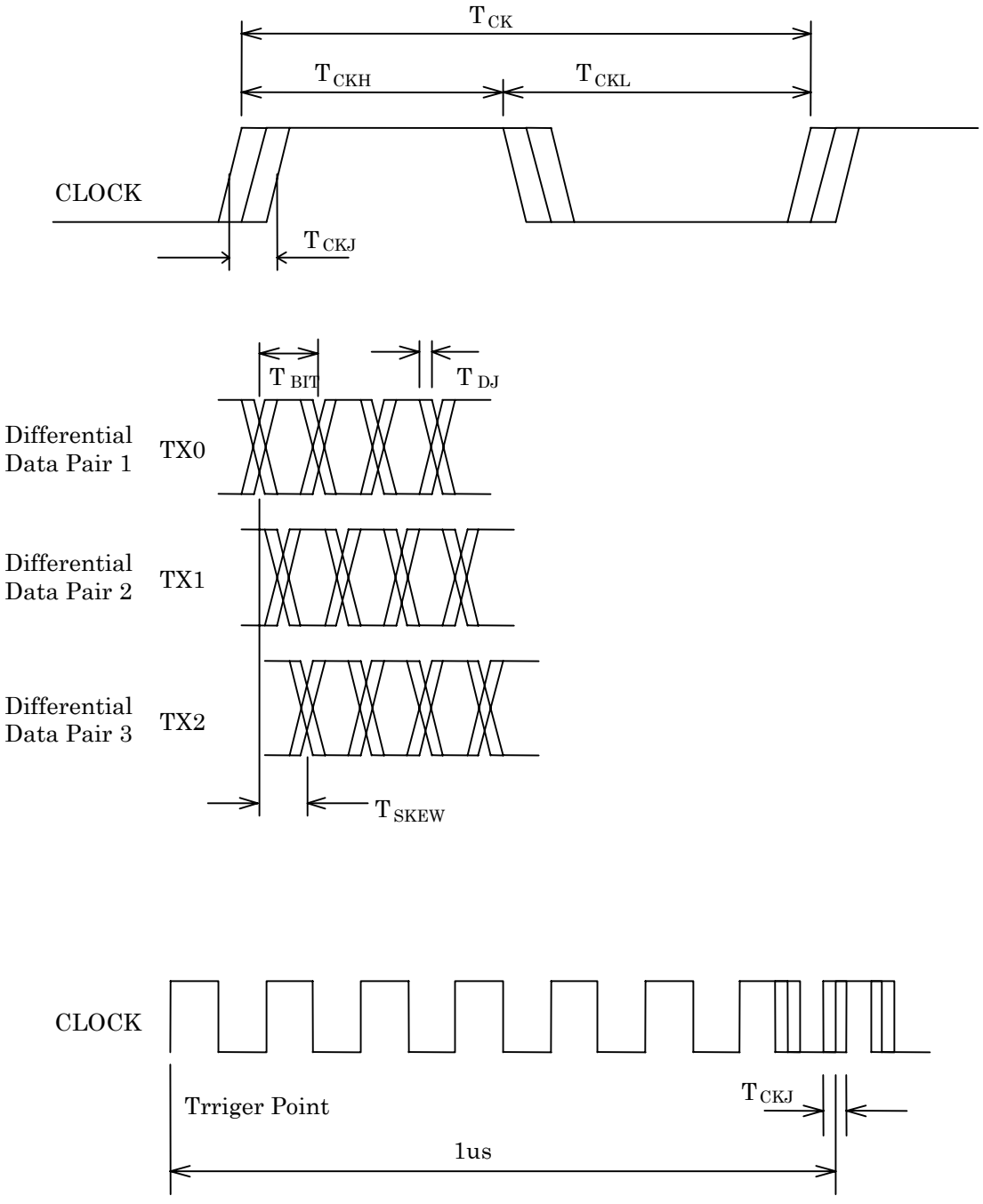


Table 5.3 TMDS Transmitter AC Specifications

Parameter	Symbol	Specification	Frequency of Pixel Clock				
			25MHz	40MHz	65MHz	112MHz	160MHz
Clock "High" Time	T_{CKH}	4ns min.					
Clock "Low" Time	T_{CKL}	4ns min.					
Clock Jitter	T_{CKJ}	2ns max.	-	-	-	-	-

Table 5.4 TMDS Receiver AC Specifications

Parameter	Symbol	Specification	Frequency of Pixel Clock				
			25MHz	40MHz	65MHz	112MHz	160MHz
Clock Jitter	T_{CKJ}	2ns max.	-	-	-	-	-
Bit Time	T_{BIT}	T_{CK} x 0.10 typ.	4 ns	2.5 ns	1.5 ns	892 ps	625 ps
Data Jitter	T_{DJ}	T_{BIT} x 0.20 typ.	800 ps	500 ps	307 ps	178 ps	125 ps
Data Skew	T_{SKEW}	T_{BIT}	20 ns	12.5 ns	7.69 ns	4.46 ns	3.125 ns

5.3.3 Termination Resistor

Termination resistor shall be the following value.

$50\Omega \pm 10\%$ (single end)

It is necessary for the value of the termination resistor to agree to the specific impedance (single end) of the cable.

5.3.4 DDC/USB Power Supply

Current of 1A maximum shall be supplied for DDC and 500mA maximum shall be supplied for USB.

5.4 Overview of Encoding and Decoding

An encoder of transmitter in TMDS converts 8 bit data into 10 bit coded data within an active display time (DE=High). 10 bit data is converted into the transition minimized data and the encoding guarantees DC-balanced. In the blank time (DE=Low), 2 bit control signals are embedded into 10bit synchronization control data, and it enables the receiver to synchronize during every blank time.

Refer to the table 5.5, 5.6 and 5.7 shown encoding data of each channel (TX0 to TX2)

Table 5.5 Encoding date at channel TX0

Data [7:0]	DE	VSYNC	VSYNC	10bit code
1 to 256	High	—	—	C_1 –C_{256}
—	Low	L	L	C_{257}
—	Low	L	H	C_{258}
—	Low	H	L	C_{259}
—	Low	H	H	C_{260}

Table 5.6 Encoding date at channel TX1

Data [7:0]	DE	PLL_SYNC	CLT1	10bit code
1 to 256	High	—	—	C_1 –C_{256}
—	Low	L	L	C_{257}
—	Low	L	H	C_{258}
—	Low	H	L	C_{259}
—	Low	H	H	C_{260}

Table 5.7 Encoding date at channel TX2

Data [7:0]	DE	CLT2	CLT3	10bit code
1 to 256	High	—	—	C_1 –C_{256}
—	Low	L	L	C_{257}
—	Low	L	H	C_{258}
—	Low	H	L	C_{259}
—	Low	H	H	C_{260}

TMDS receiver detects the synchronization codes sent from the transmitter and forms synchronization signals. The decoding block decodes 10 bit data codes and synchronization signals into 8 bit image data, 2 bit control signals and DE (Data Enable).

5.5 Connector Pin Assignment

5.5.1 MDR type Connector 26 pin

Table 5.8 26 pin Connector Pin Assignment

Pin # Host	Pin # Monitor	Signal	Description
26	1	GND (DDC)	Ground for DDC
13	14	TXC -	TMDS Differential Clock (-)
25	2	TXC SHIELD	TMDS Shield
12	15	TXC +	TMDS Differential Clock (+)
24	3	+5VDC (DDC)	+5V Power Supply for DDC
11	16	+5VDC (USB)	+5V Power Supply for USB
23	4	TX0 -	TMDS Differential Data (-)
10	17	TX0 SHIELD	TMDS Shield
22	5	TX0 +	TMDS Differential Data (+)
9	18	DDC/SCL	DDC Clock
21	6	USB-	USB Differential Signal (-)
8	19	USB SHIELD	USB Shield
20	7	USB+	USB Differential Signal (+)
7	20	Reserved	Reserved
19	8	Reserved	Reserved
6	21	Reserved	Reserved
18	9	DDC/SDA	DDC Data
5	22	TX1 -	TMDS Differential Data (-)
17	10	TX1 SHIELD	TMDS Shield
4	23	TX1 +	TMDS Differential Data (+)
16	11	GND (USB)	Ground for USB
3	24	SENS	Signal for “Hot Plugging”
15	12	TX2 -	TMDS Differential Data (-)
2	25	TX2 SHIELD	TMDS Shield
14	13	TX2 +	TMDS Differential Data (+)
1	26	GND (USB)	Ground for USB

5.5.2 MDR type Connector 20 pin

Table 5.9 20 pin Connector Pin Assignment

Pin # Host	Signal	Description
1	TX1 +	TMDS Differential Data (+)
2	TX1 -	TMDS Differential Data (-)
3	TX1 SHIELD	TMDS Shield
4	TXC SHIELD	TMDS Shield
5	TXC +	TMDS Differential Clock (+)
6	TXC -	TMDS Differential Clock (-)
7	GND	Ground for DDC
8	+5VDC	+5V Power Supply for DDC
9	Reserved	Reserved
10	Reserved	Reserved
11	TX2 +	TMDS Differential Data (+)
12	TX2 -	TMDS Differential Data (-)
13	TX2 SHIELD	TMDS Shield
14	TX0 SHIELD	TMDS Shield
15	TX0 +	TMDS Differential Data (+)
16	TX0 -	TMDS Differential Data (-)
17	Reserved	Reserved
18	SENS	Signal for “Hot Plugging”
19	DDC/SDA	DDC Data
20	DDC/SCL	DDC Clock

5.6 Data Mapping

Table 5.10 TMDS Transmitter Data Mapping

Differential Data	Input Data	18bpp	24bpp
TX0	D0	Not Used	B0
	D1	Not Used	B1
	D2	B0	B2
	D3	B1	B3
	D4	B2	B4
	D5	B3	B5
	D6	B4	B6
	D7	B5	B7
	HSYNC	HSYNC	HSYNC
	VSYNC	VSYNC	VSYNC
TX1	D8	Not Used	G0
	D9	Not Used	G1
	D10	G0	G2
	D11	G1	G3
	D12	G2	G4
	D13	G3	G5
	D14	G4	G6
	D15	G5	G7
	PLL_SYNC	PLL_SYNC	PLL_SYNC
	CTL1	Reserved	Reserved
TX2	D16	Not Used	R0
	D17	Not Used	R1
	D18	R0	R2
	D19	R1	R3
	D20	R2	R4
	D21	R3	R5
	D22	R4	R6
	D23	R5	R7
	CTL2	Reserved	Reserved
	CTL3	Reserved	Reserved

Note : R0-R7, G0-G7, B0-B7 are the gradation data of red, green and blue.
R0, G0 and B0 are LSB.

5.7 Supplement

5.7.1 Applicable IC's to TMDS

Applicable IC's to TMDS are shown at the table 5.11 and 5.12 as of September, 1998.

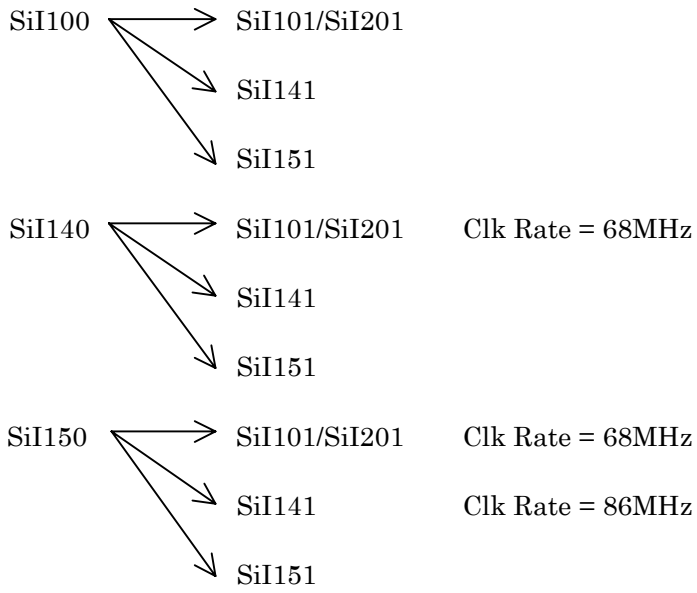
Table 5.11 Applicable Transmitters to TMDS

Model	Rev.	Manufacturer	Clk Rate	Remarks
SiI100CT64	3.51	Silicon Image, Inc.	25MHz-68MHz	
SiI140CT64	-	Silicon Image, Inc.	25MHz-86MHz	
SiI150	-	Silicon Image, Inc.	25MHz-112MHz	

Table 5.12 Applicable Receivers to TMDS

Model	Rev.	Manufacturer	Clk Rate	Remarks
SiI101CT80	3.6	Silicon Image, Inc.	25MHz-68MHz	
SiI141CT80	-	Silicon Image, Inc.	25MHz-86MHz	
SiI151	-	Silicon Image, Inc.	25MHz-112MHz	
SiI201	-	Silicon Image, Inc.	40MHz-65MHz	with LCD Controller

5.7.2 Compatibility between Transmitter and Receiver



5.7.3 Transmission Capabilities

This section shows the maximum speed display mode under VESA standard, at the Table 5.13.

Table 5.13 Maximum speed Display Mode

	When using SiI100/101	When using SiI140/141	When using SiI150/151
Clock Rate	65MHz	75MHz	108MHz
Mode	XGA	XGA	SXGA
Frame Rate	60Hz	75Hz	60Hz
Colors	16,700,000 colors	16,700,000 colors	16,700,000 colors

5.7.4 Voltage Swing Control Resistor (R_{EXT_SWING}) and Termination Control Resistor (R_{EXT_RES})

SiI100, SiI140 and SiI150 in the section of "5.7.1 Applicable IC to TMDS" causes Voltage Swing Amplitude of differential signals from the transmitter to control with a series resistor for Voltage Swing Control (R_{EXT_SWING}) .

Voltage swing amplitude shall be approximately given by expressions below.

V_{SWING} = 0.5V x (500Ω/R_{EXT_SWING})

Voltage Swing Control Resistor (R_{EXT_SWING}) shall be recommended as follows.

In case of that V_{OD} is form 450mV to 550mV.

R_{EXT_SWING} = 510Ω ± 5%

As for the Termination Control Resistor (R_{EXT_RES}), it applies value of 10 times of termination resistor at the single end. So, if termination resistor is 50Ω, R_{EXT_RES} shall become about 500Ω.

6. Data transmission standard 2a : LVDS

6.1 Introduction

Standard 2a adapts Low Voltage Differential Signaling (LVDS) as the video data transmission method and MDR type connector developed by Sumitomo 3M, Ltd., or it's compatible products, as host and monitor connector.

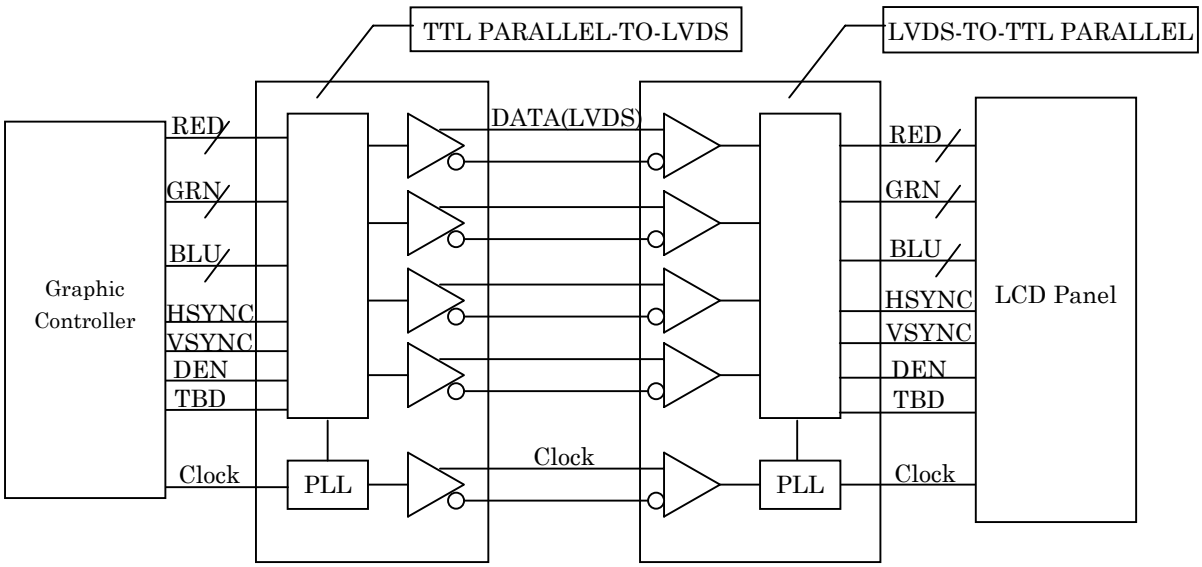
6.2 Overview

6.2.1 Architecture

The signal standard of LVDS is composed of 4 channels of video data transmission lines (R, G, B, and display control signal) and 1 channel of clock transmission line, totaling 5 channels of data transmission lines transmitted by the host system. LVDS is based on the physical layer definition of the IEEE1596.3 standard and ANSI/TIA/EIA-644. The video data transmission IC's based on LVDS are released by the following companies with their respective products: National Semiconductor Corp. with FPD Link; Texas Instruments, Inc. with FLATLINK; THine Microsystems, Inc. with the THC63LVDXXX series, etc.

The above transmission lines have a capability of 7 x f_{ck}bps as a transmitter serializes the video data (8bit each), horizontal and vertical clock signals, data enable signal, and control signal totaling 28 signals into 4 channels.

Figure 6.1 Block Diagram of FPD Link, FLAT Link, THine



6.3 Electrical Characteristics

6.3.1 DC Electrical Specifications

Refer to ANSI/TIA/EIA-644 for each item.

(1) Transmitter

Table 6.1 LVDS Transmitter DC Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Differential Output Voltage	V_{OD}	RL=100Ω	250	345	450	mV
Transmitter Offset	V_{OS}		1.125	1.25	1.375	V

(2) Receiver

Table 6.2 LVDS Receiver DC Electrical Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Differential Input High Threshold	V_{TH}	V_{CM}=1.2V			100	|mV|
Input Voltage	V_{IN}		0		2.4	V

6.3.2 AC Electrical Specifications

Refer to the data sheet published by each manufacturer (National Semiconductor, Corp., Texas Instruments, Inc., THine Microsystems, Inc.).

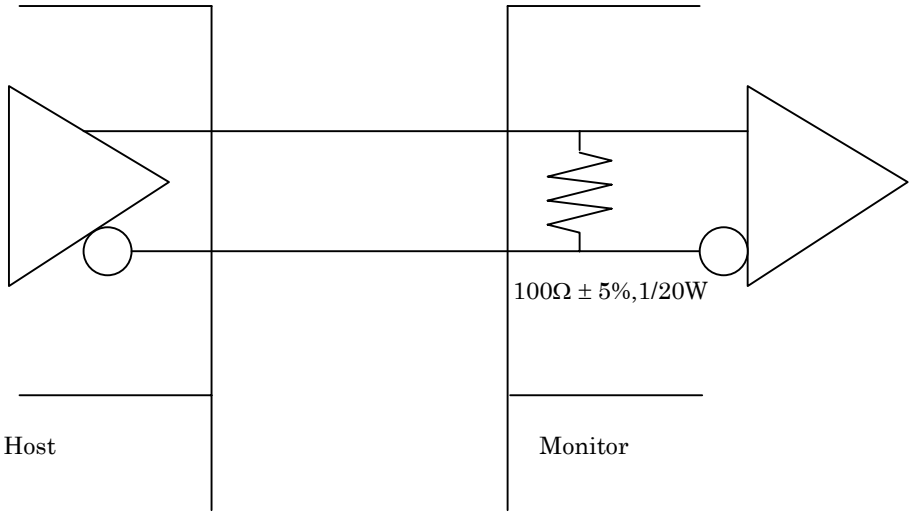
Table 6.3 AC Characteristics Reference Data Sheet List

Manufacture	Transmitter	Receiver
National Semiconductor	DS100100(March 1998)	DS012887(July 1997)
Texas Instruments	SLLS271(March 1997)	SLLS259B(May 1997)
THine Microsystems	Version 2.02	Version 2.02

6.3.3 Termination resistance

Each LVDS pair should be terminated within 5% of 100Ω ± on the monitor side.

Figure 6.2 Termination resistance



6.3.4 DDC/USB Power Supply

Current of 1A maximum shall be supplied for DDC and 500mA maximum shall be supplied for USB.

6.4 Connector Pin Assignment

This section defines the Connector Pin Assignments.

Table 6.4 26 pin Connector Pin Assignment

Pin # Host	Pin # Monitor	Signal	Description
26	1	GND (DDC)	Ground for DDC
13	14	TxOUT3+/ RxIN3+	LVDS Differential Data (+)
25	2	TxOUT3 SHIELD	LVDS Shield
12	15	TxOUT3-/ RxIN3-	LVDS Differential Data (-)
24	3	+5VDC (DDC)	+5V Power Supply for DDC
11	16	+5VDC (USB)	+5V Power Supply for USB
23	4	TxCLKOUT+/ RxCLKIN+	LVDS Differential Clock (+)
10	17	TxCLK SHIELD	LVDS Shield
22	5	TxCLKOUT-/ RxCLKIN-	LVDS Differential Clock (-)
9	18	DDC/SCL	DDC Clock
21	6	USB-	USB Differential Signal (-)
8	19	USB SHIELD	USB Shield
20	7	USB+	USB Differential Signal (+)
7	20	TxOUT2+/ RxIN2+	LVDS Differential Data (+)
19	8	TxOUT2 SHIELD	LVDS Shield
6	21	TxOUT2-/ RxIN2-	LVDS Differential Data (-)
18	9	DDC/SDA	DDC Data
5	22	TxOUT1+/ RxIN1+	LVDS Differential Data (+)
17	10	TxOUT1 SHIELD	LVDS Shield
4	23	TxOUT1-/ RxIN1-	LVDS Differential Data (-)
16	11	GND (USB)	Ground for USB
3	24	SENS	Signal for “Hot Plugging”
15	12	TxOUT0+/ RxIN0+	LVDS Differential Data (+)
2	25	TxOUT0 SHIELD	LVDS Shield
14	13	TxOUT0-/ RxIN0-	LVDS Differential Data (-)
1	26	GND (USB)	Ground for USB

6.5 Data Mapping

This section defines data mapping for TFT signal format only.

Table 6.5 Data Mapping

Differential Data(*)	Input Data	TFT 18bpp	TFT 24 bpp
TxOUT0	TxIN/RxOUT0	R0	R2
RxIN0	TxIN/RxOUT1	R1	R3
	TxIN/RxOUT2	R2	R4
	TxIN/RxOUT3	R3	R5
	TxIN/RxOUT4	R4	R6
	TxIN/RxOUT6	R5	R7
	TxIN/RxOUT7	G0	G2
TxOUT1	TxIN/RxOUT8	G1	G3
RxIN1	TxIN/RxOUT9	G2	G4
	TxIN/RxOUT12	G3	G5
	TxIN/RxOUT13	G4	G6
	TxIN/RxOUT14	G5	G7
	TxIN/RxOUT15	B0	B2
	TxIN/RxOUT18	B1	B3
TxOUT2	TxIN/RxOUT19	B2	B4
RxIN2	TxIN/RxOUT20	B3	B5
	TxIN/RxOUT21	B4	B6
	TxIN/RxOUT22	B5	B7
	TxIN/RxOUT24	HSYNC	HSYNC
	TxIN/RxOUT25	VSYNC	VSYNC
	TxIN/RxOUT26	DEN	DEN
TxOUT3	TxIN/RxOUT27	Not Used	R0
RxIN3	TxIN/RxOUT5	Not Used	R1
	TxIN/RxOUT10	Not Used	G0
	TxIN/RxOUT11	Not Used	G1
	TxIN/RxOUT16	Not Used	B0
	TxIN/RxOUT17	Not Used	B1
	TxIN/RxOUT23	Not Used	Not Used

(*) : A signal name description of a data mapping for Texas Instruments, Inc. and THine Microsystems, Inc. is stated in Table 6.6.

Table 6.6 LVDS Data Line Name Conversion

	Texas Instruments, Inc.	THine Microsystems, Inc.
TxOUT0/RxIN0	Y0/A0	TA/RA
TxOUT1/RxIN1	Y1/A1	TB/RB
TxOUT2/RxIN2	Y2/A2	TC/RC
TxOUT3/RxIN3	Y3/A3	TD/RD

6.6 Supplement

6.6.1 Applicable IC's to LVDS

This section shows applicable LVDS IC's which have a 28 bit TTL input.

(1) The National Semiconductor, Corp.

Applicable IC's as of May, 1998 are shown in the table.

Table 6.7 Applicable IC's by National Semiconductor

Model	Function	Supply Voltage (V)	Data Strobe Edge	Clock Frequency(MHz)	
				MIN	MAX
DS90CF383A	Transmitter	3.3	Falling	18	68
DS90C383A	Transmitter	3.3	Programmable	18	68
DS90CF384/A	Receiver	3.3	Falling	20	65

(2) Texas Instruments, Inc.

Applicable IC's as of March, 1998 are shown in the table.

Table 6.8 Applicable IC's by Texas Instrument

Model	Function	Supply Voltage (V)	Data Strobe Edge	Clock Frequency(MHz)	
				MIN	MAX
SN75LVDS81	Transmitter	3.3	Falling	31	68
SN75LVDS83	Transmitter	3.3	Programmable	31	68
SN75LVDS82	Receiver	3.3	Falling	31	68

(3) THine Microsystems, Inc.

Applicable IC's as of March, 1998 are shown in the table.

Table 6.9 Applicable IC's by THine Microsystems

Model	Function	Supply Voltage (V)	Data Strobe Edge	Clock Frequency(MHz)	
				MIN	MAX
THC63LVDF83A	Transmitter	3.3	Falling	20	70
THC63LVDM83A	Transmitter	3.3	Programmable	20	70
THC63LVDR84A	Receiver	3.3	Rising	20	70
THC63LVDF84A	Receiver	3.3	Falling	20	70

6.6.2 Transmission Capability

This section shows the maximum video signal in VESA standard display mode.

Table 6.10 Maximum display mode

	When using Applicable IC(*)
Clock Rate	65MHz
Mode	XGA
Frame Rate	60Hz
Colors	16,700,000 colors

(*) : When using a different IC manufactureres' transmitter/reciver combination, evaluate the combination before applying to your system.

6.6.3 Connector Pin Assignment and Data Mapping for 21-bit LVDS

(1) Connector Pin Assignment when using 21-bit LVDS IC

Table 6.11 Connector Pin Assignment for 21-bit LVDS

Pin # Host	Pin # Monitor	Signal	Description
26	1	GND(DDC)	Ground for DDC
13	14	N.C	Non Connect
25	2	N.C	Non Connect
12	15	N.C	Non Connect
24	3	+5VDC(DDC)	+5V Power Supply for DDC
11	16	+5VDC(USB)	+5V Power Supply for USB
23	4	TxCLKOUT+/ RxCLKIN+	LVDS Differential Clock (+)
10	17	TxCLK SHIELD	LVDS Shield
22	5	TxCLKOUT-/ RxCLKIN-	LVDS Differential Clock (-)
9	18	DDC/SCL	DDC Clock
21	6	USB-	USB Differential Signal (-)
8	19	USB SHIELD	USB Shield
20	7	USB+	USB Differential Signal (+)
7	20	TxOUT2+/ RxIN2+	LVDS Differential Data (+)
19	8	TxOUT2 SHIELD	LVDS Shield
6	21	TxOUT2-/ RxIN2-	LVDS Differential Data (-)
18	9	DDC/SDA	DDC Data
5	22	TxOUT1+/ RxIN1+	LVDS Differential Data (+)
17	10	TxOUT1 SHIELD	LVDS Shield
4	23	TxOUT1-/ RxIN1-	LVDS Differential Data (-)
16	11	GND(USB)	Ground for USB
3	24	SENS	Signal for “Hot Plugging”
15	12	TxOUT0+/ RxIN0+	LVDS Differential Data (+)
2	25	TxOUT0 SHIELD	LVDS Shield
14	13	TxOUT0-/ RxIN0-	LVDS Differential Data (-)
1	26	GND (USB)	Ground for USB

(2) Data Mapping when using 21-bit LVDS IC

Table 6.12 Data Mapping for 21 bit LVDS

Differential Data	Input Data	TFT 18 bpp
TxOUT0	TxIN/RxOUT0	R0
RxIN0	TxIN/RxOUT1	R1
	TxIN/RxOUT2	R2
	TxIN/RxOUT3	R3
	TxIN/RxOUT4	R4
	TxIN/RxOUT5	R5
	TxIN/RxOUT6	G0
TxOUT1	TxIN/RxOUT7	G1
RxIN1	TxIN/RxOUT8	G2
	TxIN/RxOUT9	G3
	TxIN/RxOUT10	G4
	TxIN/RxOUT11	G5
	TxIN/RxOUT12	B0
	TxIN/RxOUT13	B1
TxOUT2	TxIN/RxOUT14	B2
RxIN2	TxIN/RxOUT15	B3
	TxIN/RxOUT16	B4
	TxIN/RxOUT17	B5
	TxIN/RxOUT18	HSYNC
	TxIN/RxOUT19	VSYNC
	TxIN/RxOUT20	DEN

7. Data Transmission Standard 2b: LDI

7.1 Introduction

Standard 2b adapts LDI (LVDS Display Interface) being developed by National Semiconductor, Corp. and Texas Instruments, Inc. as the digital video transmission method, and MDR type connector developed by Sumitomo 3M, Ltd., or it's compatible products, as host and monitor connector.

7.2 Overview

7.2.1 Architecture

The signal standard of LDI is composed of 8 channels of video data transmission lines (R, G, B, and display control signal) and 1 channel of clock transmission line, totaling 10 channels of data transmission lines transmitted by the host system. LVDS is based on the physical layer definition of the IEEE1596.3 standard and ANSI/TIA/EIA-644.

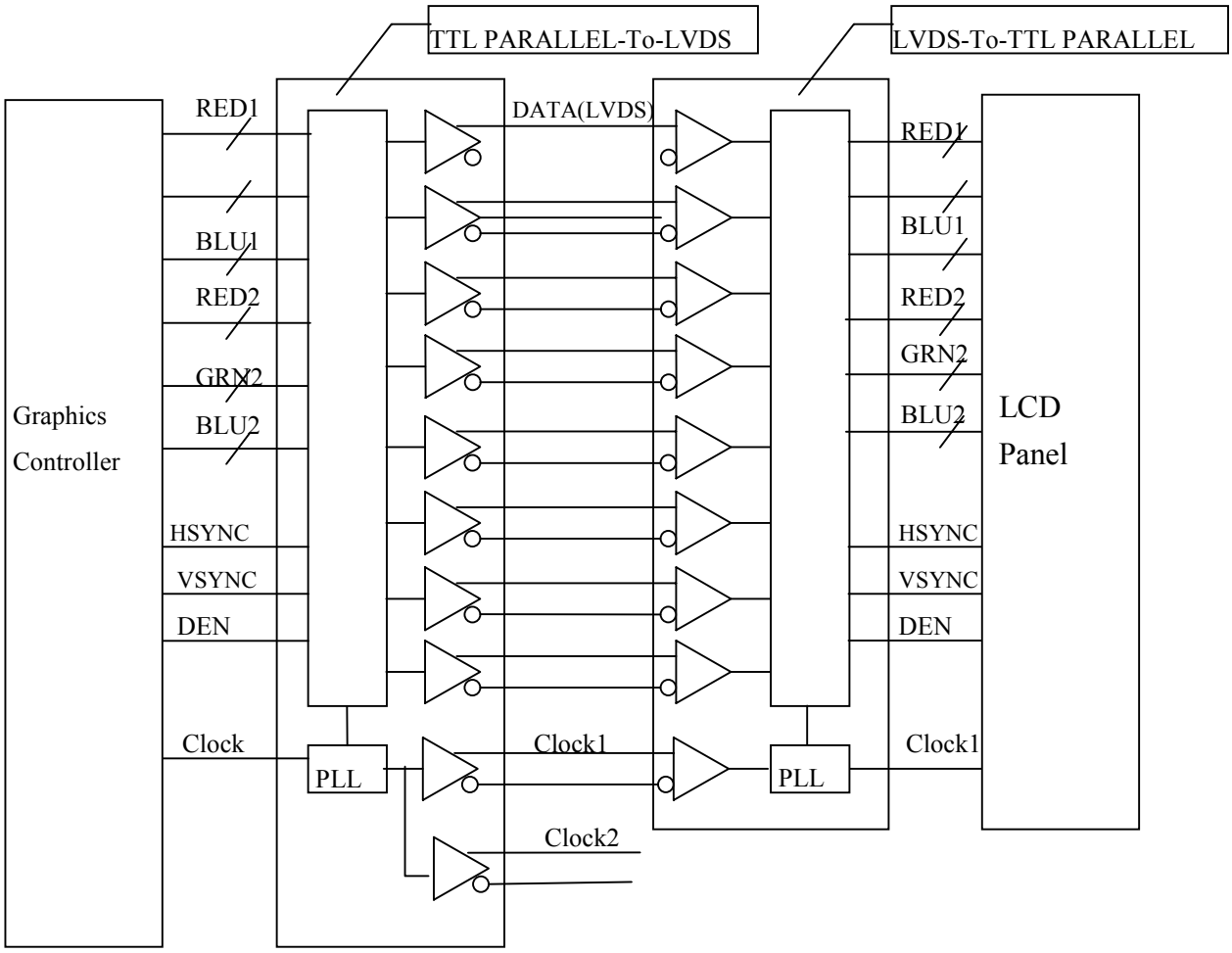
The above transmission lines have a capability of 7 x f_{ck}bps as a transmitter serializes two channels of video data (8bit each), horizontal and vertical clock signal, and data enable signal, totaling 51 signals into 8 channels.

LDI has the following two additional functions as compared to FPD Link; FLATLINK; THine Microsystems' THC63LVDXXX series (the traditional LVDS method); a DC balance function to control interference of cable transmission and a new function to transmit the display control signal during the blanking time.

(1) Complete Dual Pixel Interface

The transmitter serializes 2 channels of video data (8bits each for R, G, B for each channel, totaling 48bits), horizontal and vertical clock signals, and data enable signal to 8 channels of LVDS signals and transmits them. The receiver converts 8 channels of LVDS signals into parallel signals and outputs 2 channels of video data (8bits each for R, G, B for each channel, totaling 48bits), horizontal and vertical clock signals, and data enable signal.

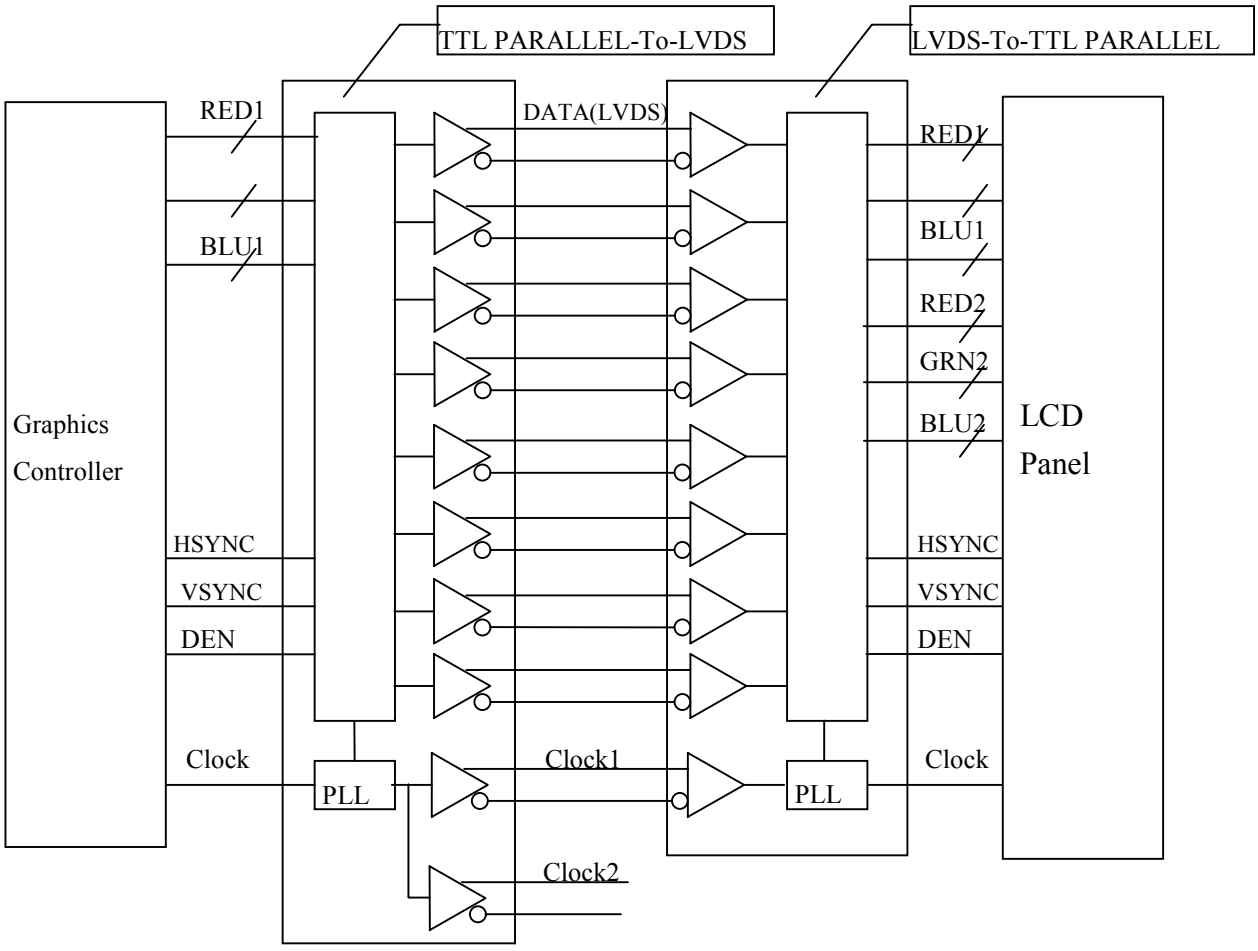
Figure 7.1 Block Diagram of LDI (Complete Dual Pixel Interface)



(2) Single Input and Dual Output at Dual LVDS Interface

A transmitter serializes 1 channel of video data (8bits each for R, G, B, totaling 24bits), horizontal and vertical clock signals, and data enable signal to 8 channels of LVDS signals and transmits them. A receiver converts 8 channels of LVDS signals into parallel signals and outputs 2 channels of video data (8bits each for R, G, B for each channel, totaling 48bits), horizontal and vertical clock signals, and data enable signal.

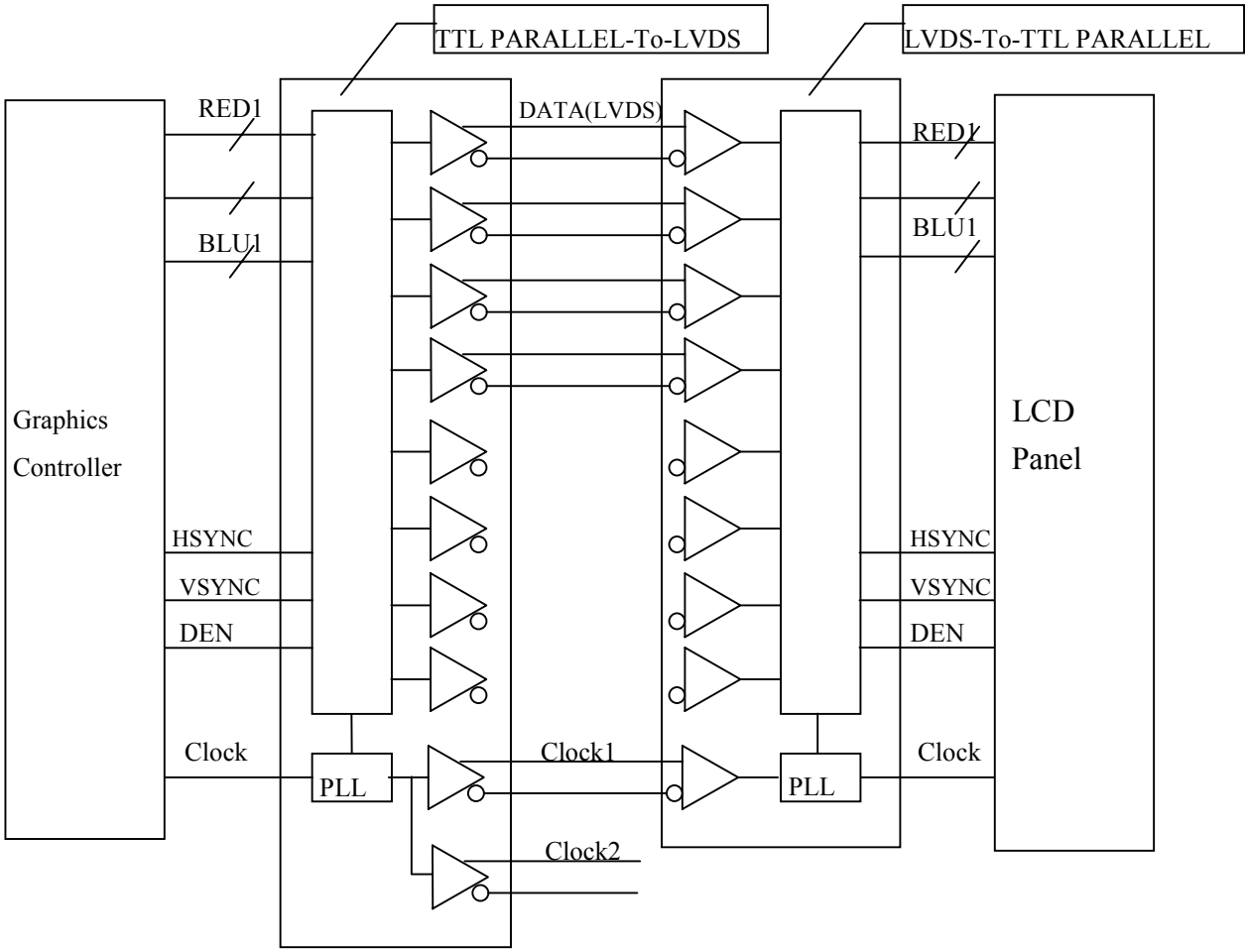
Figure 7.2 Block Diagram of LDI
(Single Input and Dual Output at Dual LVDS Interface)



(3) Single Input and Output at Single LVDS Interface

The transmitter serializes 1 channel of video data (8bits each for R, G, B, totaling 24bits), horizontal and vertical clock signals, and data enable signal to 4 channels of LVDS signals and transmits them. The receiver converts 4 channels of LVDS signals into parallel signals and outputs 1 channel of video data (8bits each for R, G, B for each channel, totaling 24bits), horizontal and vertical clock signals, and data enable signal.

Figure 7.3 Block Diagram of LD
(Single Input and Output at Single LVDS Interface)



7.3 Electrical Characteristics

7.3.1 DC Electrical Specifications

Refer to ANSI/TIA/EIA-644 for each item.

(1) Transmitter

Table 7.1 LVDS Transmitter DC Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Differential Output Voltage Amplitude	V_{OD}	R_L=100Ω	250	345	450	MV
Offset	V_{OS}		1.125	1.25	1.375	V

(2) Receiver

Table 7.2 LVDS Receiver DC Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Threshold	V_{TH}	VCM=1.2V			100	|mV|
Input Range	V_{IN}		0		2.4	V

7.3.2 AC Electrical Specifications

Refer to the data sheet published by each manufacturer (National Semiconductor, Corp., Texas Instruments, Inc., THine Microsystems, Inc.).

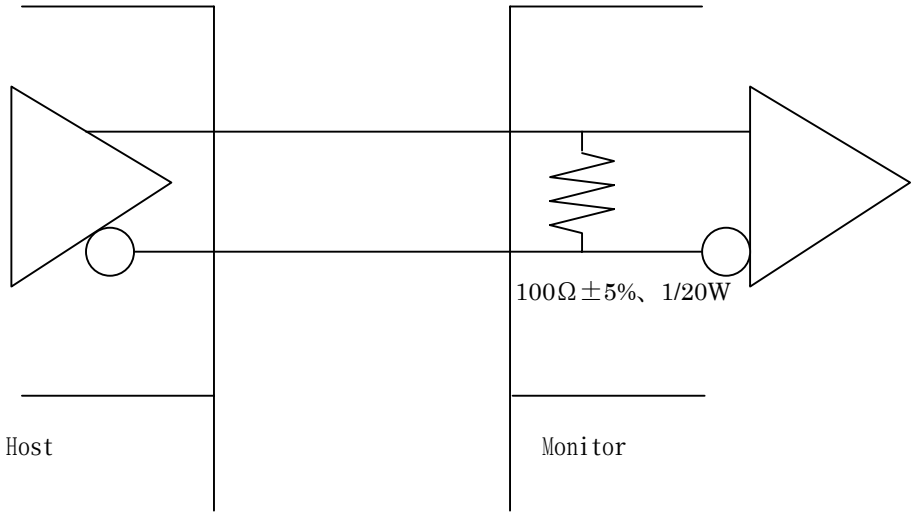
Table 7.3 Datasheets for AC Specifications

Manufacturer	Transmitter	Receiver
National Semiconductor	DS100100(March 1998)	DS012887(July 1997)
Texas Instruments	SLLS271(March 1997)	SLLS259B(May 1997)
THine Microsystems	Version 2.02	Version 2.02

7.3.3 Termination Resistor

Each LVDS pair should be terminated within 5% of 100Ω ± on the monitor side.

Figure 7.4 Termination Resistor



7.3.4 DDC/USB Power Supply

Current of 1A maximum shall be supplied for DDC and 500mA maximum shall be supplied for USB.

7.4 Connector Pin Assignment

(1) Transmitting 2 channel LVDS

The connector pin assignment is shown in Table 7.4.

Table 7.4 Connector Pin Assignment

Pin # Host	Pin # Monitor	Signal	Description
1	1	A0M	LDI Differential Signal(-)
19	19	A0P	LDI Differential Signal (+)
2	2	A1M	LDI Differential Signal (-)
20	20	A1P	LDI Differential Signal (+)
3	3	A2M	LDI Differential Signal (-)
21	21	A2P	LDI Differential Signal (+)
4	4	CLK1M	CLK1M
22	22	CLK1P	CLK2P
5	5	A3M	LDI Differential Signal (-)
23	23	A3P	LDI Differential Signal (+)
6	6	AXGND	LDI/USB Shield
24	24	AXGND	LDI/USB Shield
7	7	DUAL (*1)	Dual/Single Mode Switch
25	25	BAL (*2)	DC Balance Mode (When High)
8	8	GND (USB)	USB GND
26	26	GND (DDC)	DDC GND
9	9	SENS	Signal for “Hot Plugging”
27	27	NC	
10	10	DDC/SCL	DDC Clock
28	28	DDC/SDA	DDC Data
11	11	+5V DC (DDC)	+5V Power Supply for DDC
29	29	+5V DC (USB)	+5V Power Supply for USB
12	12	USB+	USB Differential Signal (+)
30	30	USB-	USB Differential Signal (-)

13	13	AXGND	LDI/USB Shield
31	31	AXGND	LDI/USB Shield
14	14	A4M	LDI Differential Signal (-)
32	32	A4P	LDI Differential Signal (+)
15	15	A5M	LDI Differential Signal (-)
33	33	A5P	LDI Differential Signal (+)
16	16	A6M	LDI Differential Signal (-)
34	34	A6P	LDI Differential Signal (+)
17	17	A7M	LDI Differential Signal (-)
35	35	A7P	LDI Differential Signal (+)
18	18	CLK2M	CLK2M
36	36	CLK2P	CLK2P

(*1)DUAL: Switch DUAL/Single transmission, High = DUAL Transmission

(*2)BAL : Set Balance Mode, High = DC Balance Mode

(2) Transmitting 1 channel LVDS

The connector pin assignment is shown in Table 7.5.

Table 7.5 Connector Pin Assignment

Pin # Host	Pin # Monitor	Signal	Description
1	1	A0M	LDI Differential Signal (-)
19	19	A0P	LDI Differential Signal (+)
2	2	A1M	LDI Differential Signal (-)
20	20	A1P	LDI Differential Signal (+)
3	3	A2M	LDI Differential Signal (-)
21	21	A2P	LDI Differential Signal (+)
4	4	CLK1M	CLK1M
22	22	CLK1P	CLK2P
5	5	A3M	LDI Differential Signal (-)
23	23	A3P	LDI Differential Signal (+)
6	6	AXGND	LDI/USB Shield
24	24	AXGND	LDI/USB Shield
7	7	DUAL (*1)	Set Low (GND)
25	25	BAL (*2)	Set Low (GND)
8	8	GND (USB)	USB GND
26	26	GND (DDC)	DDC GND
9	9	SENS	Signal for “Hot Plugging”
27	27	NC	
10	10	DDC/SCL	LDI Differential Signal (+)
28	28	DDC/SDA	LDI Differential Signal (-)
11	11	+5V DC (DDC)	+5V Power Supply for DDC
29	29	+5V DC (USB)	+5V Power Supply for USB
12	12	USB+	USB Differential Signal (+)
30	30	USB-	USB Differential Signal (-)
13	13	AXGND	LDI/USB Shield

31	31	AXGND	LDI/USB Shield
14	14	Not Used	Not Used
32	32	Not Used	Not Used
15	15	Not Used	Not Used
33	33	Not Used	Not Used
16	16	Not Used	Not Used
34	34	Not Used	Not Used
17	17	Not Used	Not Used
35	35	Not Used	Not Used
18	18	Not Used	Not Used
36	36	Not Used	Not Used

(*1)DUAL: Switch DUAL/Single transmission, High = DUAL Transmission

(*2)BAL : Set Balance Mode, High = DC Balance Mode

7.5 Data Mapping

(1) DC Balance Mode

The data mapping for DC balanced mode is shown in Table 7.6.

Table 7.6 Data Mapping (DC Balance Mode)

Signal	Data	Signal	Data
TxOUT0/	R10	TxOUT4/	R20
RxIN0	R11	RxIN4	R21
	R12		R22
	R13		R23
	R14		R24
	R15		R25
	DCBAL		DCBAL
TxOUT1/	G10	TxOUT5/	G20
RxIN1	G11	RxIN5	G21
	G12		G22
	G13		G23
	G14		G24
	G15		G25
	DCBAL		DCBAL
TxOUT2/	B10	TxOUT6/	B20
RxIN2	B11	RxIN6	B21
	B12		B22
	B13		B23
	B14		B24
	B15		B25
	DCBAL		DCBAL
TxOUT3/	R16	TxOUT7/	R26
RxIN3	R17	RxIN7	R27
	G16		G26
	G17		G27
	B16		B26
	B17		B27
	DCBAL		DCBAL

(2) Non DC Balance Mode

The data mapping for Non DC balanced mode is shown in Table 7.7.

Table 7.7 Data Mapping (Non DC Balance Mode)

Signal	Data	Signal	Data
TxOUT0/	G10	TxOUT4/	G20
RxIN0	R15	RxIN4	R25
	R14		R24
	R13		R23
	R12		R22
	R11		R21
	R10		R20
TxOUT1/	B11	TxOUT1/	G21
RxIN1	B10	RxIN1	B20
	G15		G25
	G14		G24
	G13		G23
	G12		G22
	G11L		G21
TxOUT2/	EN	TxOUT2/	EN
RxIN2	VSYNC	RxIN2	TESTA
	HSYNC		TESTB
	B15		B25
	B14		B24
	B13		B23
	B12		B22
TxOUT3/		TxOUT7/	
RxIN3	B17	RxIN7	B27
	B16		B26
	G17		G27
	G16		G26
	R17		R27
	R16		R26

7.6 Supplement

7.6.1 Applicable IC's to LVDS

(1) National Semiconductor Corp.

This section shows applicable LVDS IC's which have a 28 bit TTL input. The following information is as of May, 1998.

(a) Complete Dual Pixel Interface

Table 7.8 Applicable IC's to LDI (Dual Interface) by National Semiconductor Corp.

Model	Function	Supply Voltage (V)	Data Strobe Edge	Clock Frequency(MHz)	
				MIN	MAX
DS90CF387	Transmitter	3.3	Falling	32.5	112
DS90CF388	Receiver	3.3	Falling	32.5	112

(b) Single Input and Dual Output at Dual LVDS Interface

Table 7.9 Applicable IC's to LDI (Single Input Dual Output) by National Semiconductor Corp.

Model	Function	Supply Voltage (V)	Data Strobe Edge	Clock Frequency(MHz)	
				MIN	MAX
DS90CF387	Transmitter	3.3	Falling	65	170
DS90CF388	Receiver	3.3	Falling	32.5	85

(c) Single Input and Output at Single LVDS Interface

Table 7.10 Applicable IC's to LDI (Single Interface) by National Semiconductor Corp.

Model	Function	Supply Voltage (V)	Data Strobe Edge	Clock Frequency(MHz)	
				MIN	MAX
DS90CF387	Transmitter	3.3	Falling	32.5	112
DS90CF388	Receiver	3.3	Falling	32.5	112

7.6.2 Transmission Capabilities

This section shows the maximum transmission capabilities of DS90C387, 388 developed by National Semiconductor Corp..

(1) Dual LVDS Transmission

Maximum Display Data Dot Clock: 224MHz

(2) Single LVDS Transmission

Maximum Display Data Dot Clock: 112MHz

(3) Single Video Data Input

When using a single input mode as a data input of a transmitter, maximum transmission speed is 85MHz for Dual LVDS transmission mode and 112MHz for single LVDS transmission mode as its maximum input is 170MHz.

The following shows the minimum transmission capabilities of DS90C387, 388 developed by National Semiconductor Corp..

(1) Dual LVDS Transmission

Minimum Display Data Dot Clock: 65MHz

(2) Single LVDS Transmission

Minimum Display Data Dot Clock: 32.5MHz

(3) Single Video Data Input

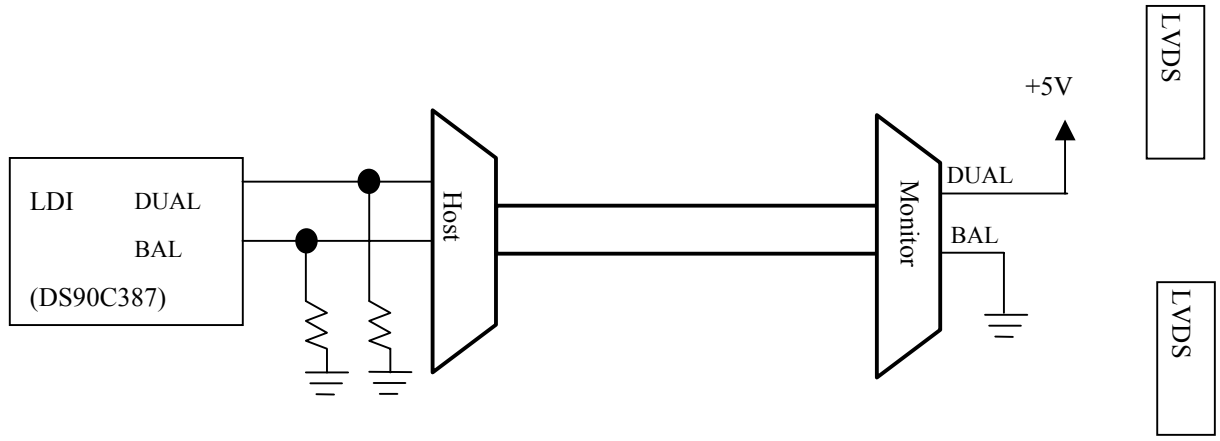
When using a single input mode as a data input of a transmitter, minimum transmission speed is 65MHz for Dual LVDS transmission mode and 32.5MHz for single LVDS transmission mode.

7.6.3 Dual/BAL Mode Application Example

This section shows the examples of DUAL/BAL pin usage. Those examples are NOT a mandatory requirement of DISM.

(1) Host (LDI), Monitor (LVDS 2ch)

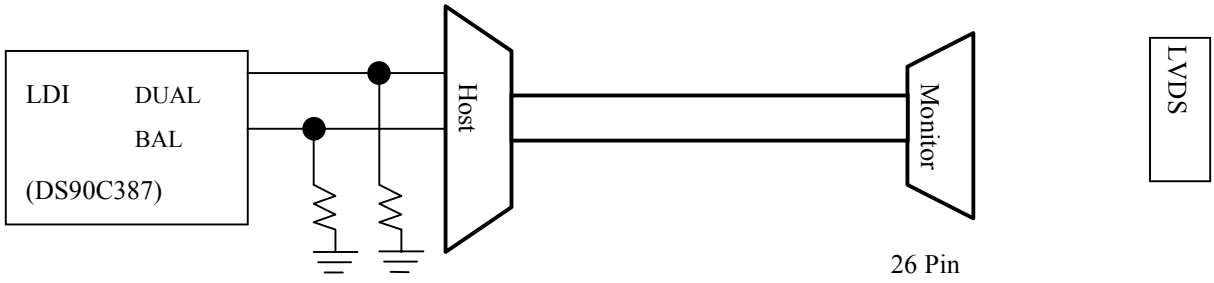
Figure 7.4 Example of LDI Host and LVDS 2ch Monitor



For host side, connect pulled down signals between LDI and a connector.
For monitor side, connect DUAL to +5V, and BAL to ground.
The above configuration sets a DUAL transmission mode and non-DC balance mode. Thus signals can be transmitted to 2 channels of LVDS at monitor side.

(2) Host (LDI), Monitor (LVDS 1ch)

Figure 7.5 Example of LDI Host and LVDS 1ch Monitor

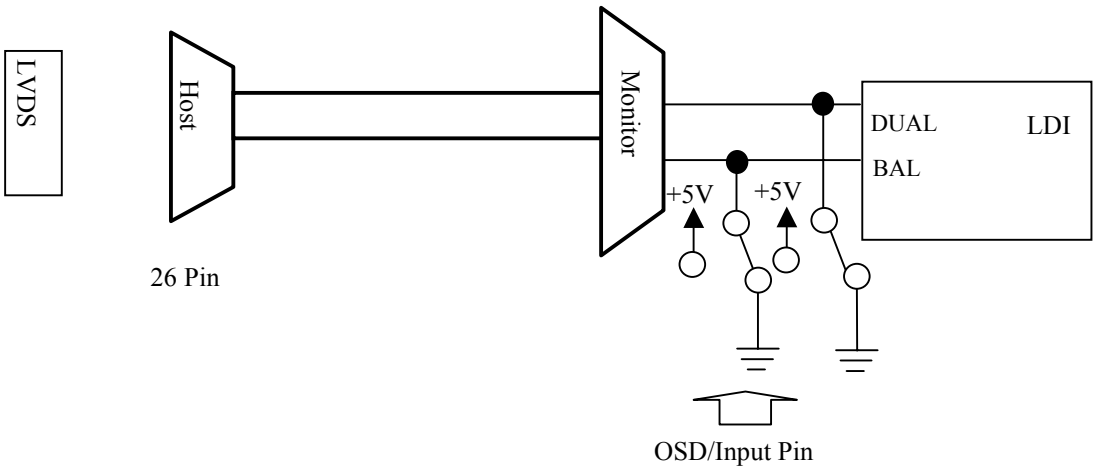


When assembling a 36pin to 26pin cable, disconnect DUAL/BAL signal line of 36pin. This sets Low level of pulled down signal to LDI, a single transmission mode and non-DC balance mode is configured. Thus signals can be transmitted to LVDS of monitor side

The current LDI transmitter (DS90C387) does not support single LVDS output at Dual input of display data. Thus a graphics chip has to be configured to output single display data in order to support single LVDS output.

(3) Host (LVDS 1ch), Monitor (LDI)

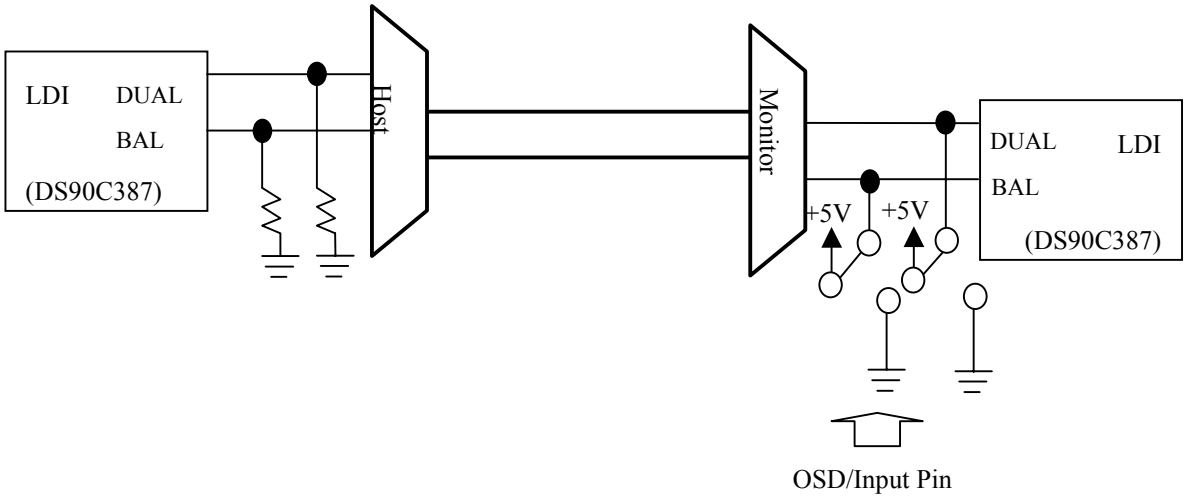
Figure 7.6 Example of LVDS 1ch Host and LDI Monitor



When assembling a 36pin to 26pin cable, disconnect DUAL/BAL signal line of 36pin. Also set both DUAL and BAL to ground level at monitor side by OSD. This sets Low level of pulled down signal to LDI, a single transmission mode and non-DC balance mode is configured. Thus signals can be transmitted to LVDS of monitor side

(4) Host (LDI), Monitor (LDI)

Figure 7.7 Example of LDI Host and LDI Monitor



Set Dual/Single transmission and balance mode by OSD.
Use Dual mode if over 112MHz (when using DS90C387/DS90CF388) of transmission speed is required.

8. Data Transmission Standard 3 : GVIF

8.1 Introduction

Standard 3 adapts GVIF by SONY, Corp. as a digital video data transmission method and MDR type connector by Sumitomo 3M, Ltd. or it's compatible products as host and monitor connector.

8.2 GVIF Overview

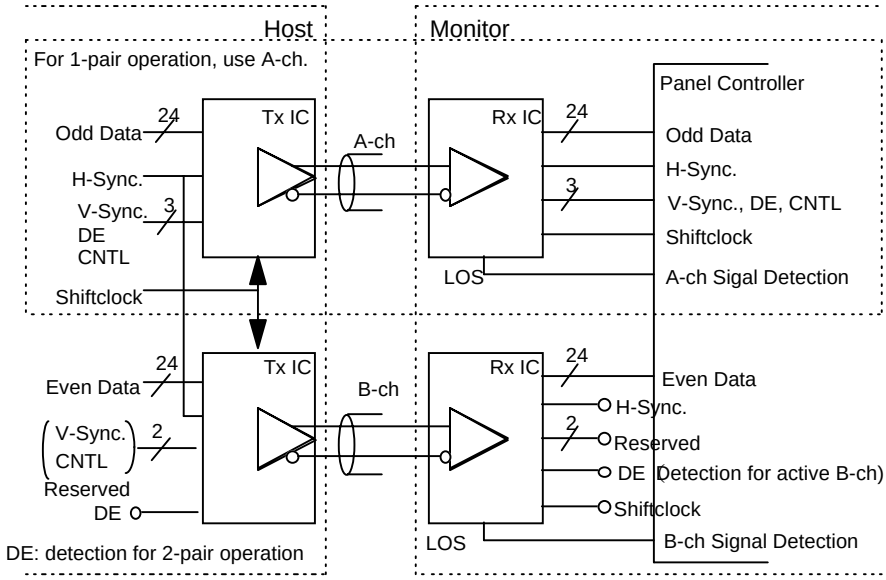
GVIF (Gigabit Video Interface) is base-band digital video interface using advanced serial data transmission technology. It is possible to transmit 24 bit color VGA/SVGA/XGA/SXGA/UXGA video data, and features are as follows.

- GVIF allows to use small connector and long cable.
  Because of is required just one pair of differential cable.
  In case of over SXGA resolutions, GVIF supports them using two pairs.
- Excellent EMI performance by small differential signal (400mVp-p) with good DC balancing.
  No external controller or reference clock.
  GVIF has all of the functions which are required for serial data transmission, such as high speed clock generator, clock and data recover circuit, data coding, synchronizing controller and so on,
- GVIF allows to use over 5[m] cable and to change without adjustment.
  Because of the receiver has built-in automatic cable equalizer.

8.2.1 Block Diagram

The block diagram of transmitter/receiver is shown in figure 8.2.1.

Figure 8.2.1 Block Diagram of GVIF



For switching one pair operation and two pair operation, host should have the decision circuit.

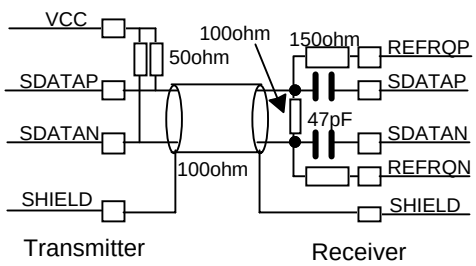
When two pair operation, DE at B-ch should have the signal for DE.

When one pair operation, DE at B-ch should be fixed level.

8.2.2 Transmission Line

Transmission impedance 100-ohm shielded twisted pair line

Figure 8.2.2 Transmission line



8.2.3 Variation

Standard 3 defines the following two variation depending on the required transmission capability.

(1) 1-pair

For dot clock is 65MHz or lower, one pair should be used.

(2) 2-pairs

For dot clock is over 65MHz, two pair should be used.

Data mapping should be as chapter 8.6.

Table 8.2.3 Variation for transmission capacity

	VGA	SVGA	XGA (*)	SXGA	UXGA
1-pair	Yes	Yes	Yes	No	No
2-pair	No	No	Yes	Yes	Yes

(*) For over 65MHz dot clock, 2-pair should be used.

8.3 Electrical Characteristics

8.3.1 DC Electrical Specifications

Table 8.3.1a DC Electrical Specifications of Transmitter

Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
IOH_SD	Output HIGH Current (SDATA)		0		mA	
IOL_SD	Output LOW Current (SDATA)		16		mA	(*1)
VIH_SD	Input HIGH Voltage (SDATA)		Vcc1-0.4		V	Common Mode
VIL_SD	Input LOW Voltage (SDATA)		Vcc1-0.8		V	Voltage (*2)

(*1) : Differential output using 16mA driven NPN Transistor (Open collector).

400mV(p-p) voltage swing at transmission port when 25-ohm load as Fig.8.2.2.

(*2) : Vcc1 is power supply voltage of transmitter IC.

Table 8.3.1b DC Electrical Specifications of Receiver

Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
IOH_RQ	Output HIGH Current (REFREQ)		0		mA	
IOL_RQ	Output LOW Current (REFREQ)		8.0		mA	

8.3.2 AC Electrical Specifications

Table 8.3.2a AC Electrical Specifications of Transmitter

Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
Fsftclk	Minimum SFTCLK Frequency			25.0	MHz	
	Maximum SFTCLK Frequency	65.0			MHz	
Dsftclk	SFTCLK Duty Factor	40		60	%	Vth = 1.4V

Table 8.3.2b AC Electrical Specifications of Receiver

Symbol	Description	Min.	Typ.	Max.	Unit	Conditions
Fsftclk	Minimum SFTCLK Frequency			25.0	MHz	
	Maximum SFTCLK Freqency	65.0			MHz	

8.3.3 Termination

Transmitter: Pull up both + and – to Vcc using 50-ohm(within +/-5%) resisters.

Receiver: Terminate differential port using 100-ohm(within +/-5%) resisters.

Refer Fig.8.2.2.

8.3.4 DDC/USB Power Supply

Maximum 1 A_{DC}.

8.4 Encode Decode

Enc. codes captured 28-bit data which are RGB, H/VSYNC, DE and CNTL to 30-bit word. If the coding was not available, in case of very simple picture such as all black, receiver had trouble due to missing word termination. The Encoder generates the pattern which allow receiver to recover the data, and to keep good DC balancing and word synchronizing pattern when falling edge of HSYNC.

8.5 Connector Pin Assignment

Table 8.5 14 pin Connector Pin Assignment

Pin		Signal	Description
Host	Monitor		
1	1	SDATAN-A	GVIF Data A -
8	8	SDATA SHIELD-A	GVIF Shield A
2	2	SDATAP-A	GVIF Data A +
9	9	VCC (+5V)	USB/DDC Power +5V
3	3	GND	USB/DDC GND
10	10	SDATAN-B	GVIF Data B -
4	4	SDATA SHIELD-B	GVIF Shield B
11	11	SDATAP-B	GVIF Data B +
5	5	DDC/SCL	DDC Clock
12	12	DDC/SDA	DDC Data
6	6	USB+	USB Data +
13	13	USB SHIELD	USB Shield
7	7	USB-	USB Data -
14	14	SENS	For “Hot Plugging”

8.6 Data Mapping

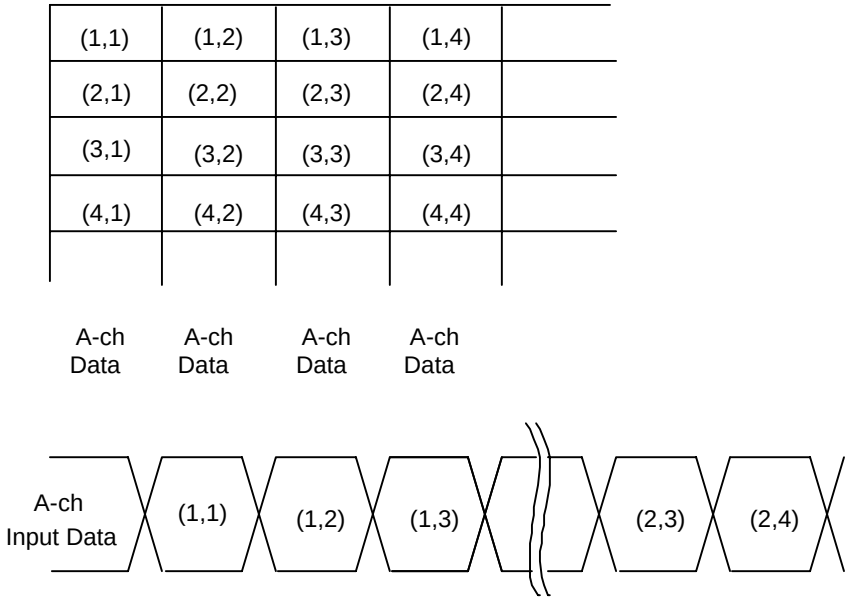
8.6.1 Data Mapping when using 1-pair

A-ch should be used in Chapter 8.5.

Table 8.6.1 GVIF Data Mapping (When using 1-pair)

Description	24-bit Color		18-bit Color	
	Sig. Name	Comment	Sig. Name	Comment
R0	R0	R data (LSB)	Not used	
R1	R1	R Data	Not used	
R2	R2	R Data	R0	R data (LSB)
R3	R3	R Data	R1	R Data
R4	R4	R Data	R2	R Data
R5	R5	R Data	R3	R Data
R6	R6	R Data	R4	R Data
R7	R7	R Data (MSB)	R5	R Data (MSB)
G0	G0	G Data(LSB)	Not used	
G1	G1	G Data	Not used	
G2	G2	G Data	G0	G Data(LSB)
G3	G3	G Data	G1	G Data
G4	G4	G Data	G2	G Data
G5	G5	G Data	G3	G Data
G6	G6	G Data	G4	G Data
G7	G7	G Data((MSB)	G5	G Data (MSB)
B0	B0	B Data(LSB)	Not used	
B1	B1	B Data	Not used	
B2	B2	B Data	B0	B Data (LSB)
B3	B3	B Data	B1	B Data
B4	B4	B Data	B2	B Data
B5	B5	B Data	B3	B Data
B6	B6	B Data	B4	B Data
B7	B7	B Data (MSB)	B5	B Data (MSB)
HSYNC	HSYNC	H-Sync	HSYNC	H-Sync
VSYNC	VSYNC	V-Sync	VSYNC	V-Sync
CNTL	-	(Reserved)	-	(Reserved)
DE	DE	Data Enable	DE	Data Enable

Figure 8.6.1 Pixel Configuration when using 1-pair



8.6.2 Data Mapping when using 2-pair

Odd Data should be assigned to A-ch, even data should be assigned to B-ch.

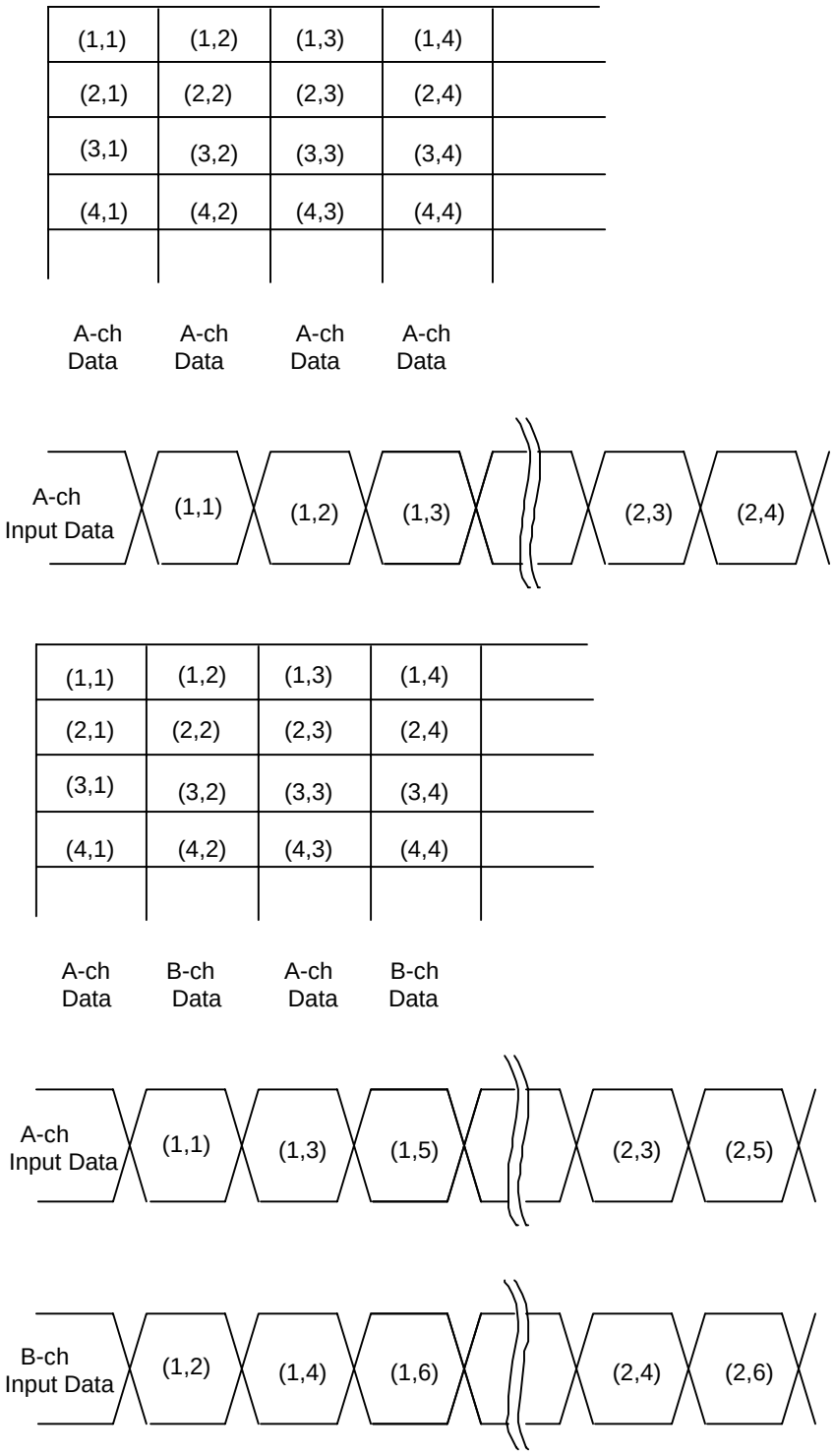
Table 8.6.2a Data for A-ch Mapping (When using 2-pair)

Description	24-bit Color		18-bit Color	
	Sig. Name	Comment	Sig. Name	Comment
R0	R0	R data (LSB)	Not used	
R1	R1	R Data	Not used	
R2	R2	R Data	R0	R data (LSB)
R3	R3	R Data	R1	R Data
R4	R4	R Data	R2	R Data
R5	R5	R Data	R3	R Data
R6	R6	R Data	R4	R Data
R7	R7	R Data (MSB)	R5	R Data (MSB)
G0	G0	G Data(LSB)	Not used	
G1	G1	G Data	Not used	
G2	G2	G Data	G0	G Data(LSB)
G3	G3	G Data	G1	G Data
G4	G4	G Data	G2	G Data
G5	G5	G Data	G3	G Data
G6	G6	G Data	G4	G Data
G7	G7	G Data (MSB)	G5	G Data (MSB)
B0	B0	B Data (LSB)	Not used	
B1	B1	B Data	Not used	
B2	B2	B Data	B0	B Data (LSB)
B3	B3	B Data	B1	B Data
B4	B4	B Data	B2	B Data
B5	B5	B Data	B3	B Data
B6	B6	B Data	B4	B Data
B7	B7	B Data (MSB)	B5	B Data (MSB)
HSYNC	HSYNC	H-Sync	HSYNC	H-Sync
VSYNC	VSYNC	V-Sync	VSYNC	(Reserved)
CNTL	-	(Reserved)	-	（Reserved）
DE	DE	Data Enable	DE	Data Enable

Table 8.6.2b Data for B-ch Mapping (When using 2-pair)

Description	24-bit Color		18-bit Color	
	Sig. Name	Comment	Sig. Name	Comment
R0	R0	R data (LSB)	Not used	
R1	R1	R Data	Not used	
R2	R2	R Data	R0	R data (LSB)
R3	R3	R Data	R1	R Data
R4	R4	R Data	R2	R Data
R5	R5	R Data	R3	R Data
R6	R6	R Data	R4	R Data
R7	R7	R Data (MSB)	R5	R Data (MSB)
G0	G0	G Data (LSB)	Not used	
G1	G1	G Data	Not used	
G2	G2	G Data	G0	G Data (LSB)
G3	G3	G Data	G1	G Data
G4	G4	G Data	G2	G Data
G5	G5	G Data	G3	G Data
G6	G6	G Data	G4	G Data
G7	G7	G Data (MSB)	G5	G Data (MSB)
B0	B0	B Data (LSB)	Not used	
B1	B1	B Data	Not used	
B2	B2	B Data	B0	B Data (LSB)
B3	B3	B Data	B1	B Data
B4	B4	B Data	B2	B Data
B5	B5	B Data	B3	B Data
B6	B6	B Data	B4	B Data
B7	B7	B Data (MSB)	B5	B Data (MSB)
HSYNC	HSYNC	H-Sync	HSYNC	H-Sync
VSYNC	VSYNC	(Reserved)	VSYNC	(Reserved)
CNTL	-	(Reserved)	-	（Reserved）
DE	DE	Data Enable	DE	Data Enable

Figure 8.6.2 Pixel Configuration when using 2-pair



8.7 Supplement

8.7.1 GVIF IC

Table 8.7.1 Applicable IC's to GVIF

Transmitter	Receiver
Sony CXB1455R	Sony CXB1454R (with Cable Equalizer)
	Sony CXB1456R (Low Power Consumption)

Note : October, 1998

CXB1456R works at 1-pair operation ONLY

8.7.2 Transmission Capabilities for GVIF IC Sony CXB1455R

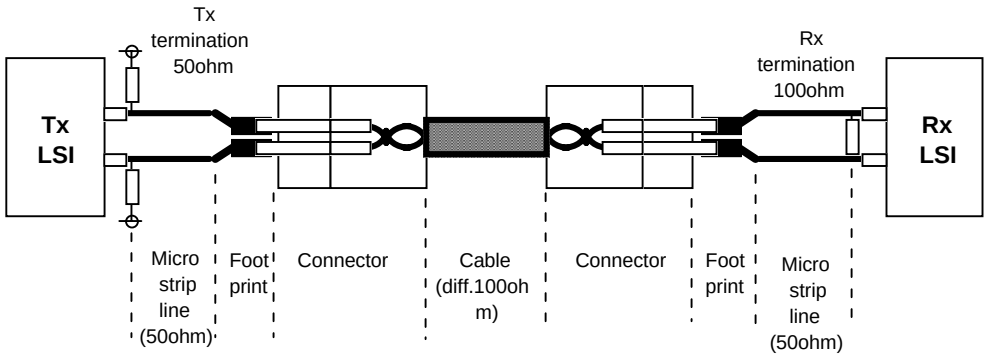
Table 8.7.2 Maximum Transmission Capabilities for Sony CXB1455R

	1-pair	2-pair
Clock Frequency	65MHz	130MHz
Resolution	XGA	SXGA
Color Resolution	24bit	24bit

8.7.3 Recommended Transfer System

Recommendation for cable and connector characteristics

GVIF system uses terminators at both end (transmitter and receiver), cable equalizer and small amplitude differential signal, in order to solve the troubles of high speed data transmission, such as signal reflection, reducing signal level and EMI.
In order to achieve best solution, you should pay attentions as follows,



The followings are important issues for good data transmission system.

1) Good Impedance matching
   Differential impedance should be fit to recommended template in the next page.
2) Cable loss should be small and loss curve should be smooth.
   For CXB1454R which has built-in cable equalizer.
      Maximum Loss should be less than 15 dB at 1GHz,
      and the attenuation curve is like square root of frequency.
   For CXB1456R which has no equalizer in it.
      Maximum Loss should be less than 3 dB at 1GHz,
3) Skew of POS/NEG (differential signal) should be small.
   Less than 12% of 1 bit time
      That is, 160pS @VGA, 100pS@SGVA, 60pS@XGA
4) Good EMI performance cable and connectors

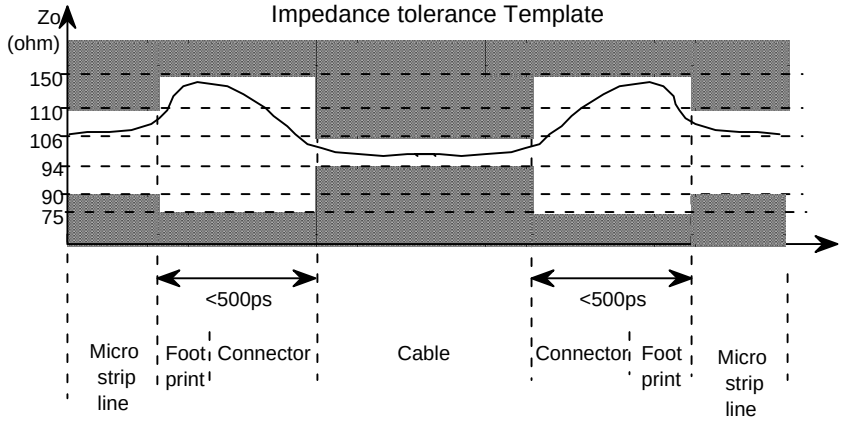
In order to satisfy the above issues, the recommendations are as follows,

1) Use the differential cable which is good controlled impedance, low loss and good skew matching. Shielded twisted pair(STP) cable is recommended.
2) Use the connector which is low reflectance.
3) Pay attention for assignment of signals at connector pins. Minimize interference from other signals and pair of high speed signals length should be identical.
4) Use double shielded cable.

8.7.4 Recommended Transfer Line

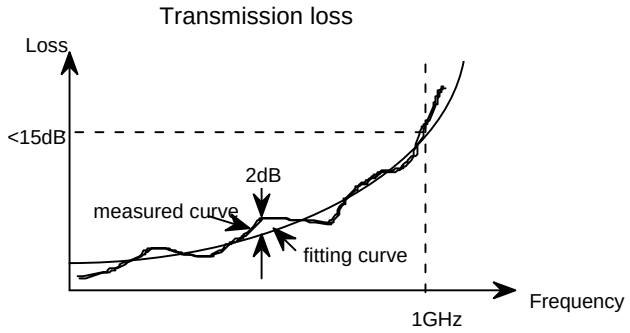
1) Impedance

GVIF transmission system use 100ohm in differential transmission line. Impedance mismatch causes bit error and increase EMI by signal reflection.
Tolerance of impedance for GVIF transmission is shown in Figure 2.



2) Loss

GVIF employs Automatic cable equalizer to compensate "sqrt(f)dB loss" by skin effect.
The loss of transmission system should be well fit to the sqrt(f)dB curve and less than 15dB@1GHz as shown in Figure 3.



9. Other Supported Signals

9.1 DDC

The DDC standard used with the Data Transmission Standard 1, 2a, 2b, 3 is referred to VESA Display Data Channel Standard Version 3.0 (Date: May, 1998) defined by VESA.

9.2 SENS Signal

9.2.1 Definition

The SENS signal used with the Data Transmission Standard 1, 2a, 2b, 3 is used to support the "hot plugging" function defined by VESA. However, it is not used for "Charge Power" but only detecting display.

9.2.2 Electrical Characteristics

Table 9.1 Characteristics of SENS Signal for Display

		Min.	Typ.	Max.	Unit	Remarks
Output Voltage	V_{SO}	2.4		20	V	
Output Current	I_{SO}			10	mA	

Table 9.2 Characteristics of SENS signal for Host

		Min.	Typ.	Max.	Units	Remarks
Input Voltage	V_{SI}	2.0		20	V	
Input Current	I_{SI}			10	mA	

9.3 USB

The USB standard used with the Data Transmission Standard 1, 2a, 2b, 3 is referred to Universal Serial Bus Specification Version 1.0 (Date: May, 1998) defined by VESA.

10. Display Signal Timing Specifications

10.1 Introduction

This chapter defines timing specifications such as horizontal and vertical frequency, blanking time and so on.

10.2 Definition

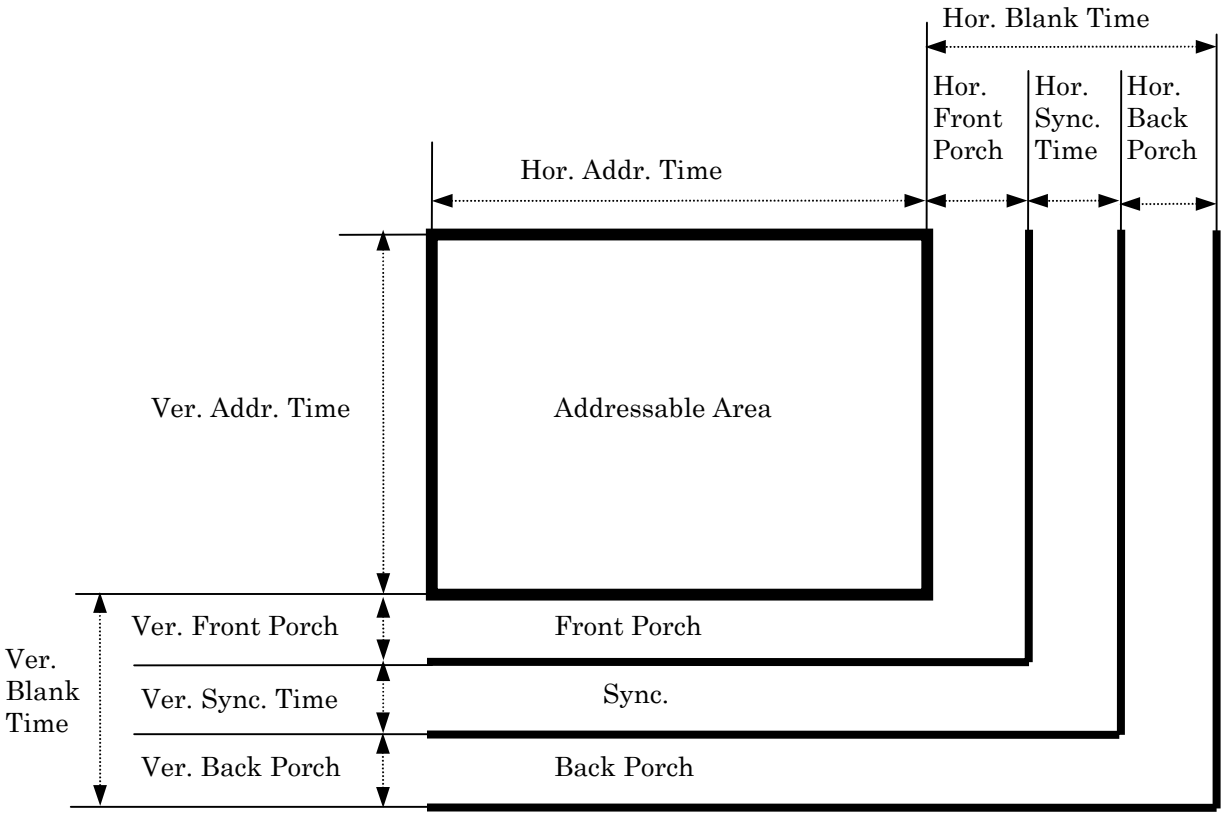
DISM standard supports the following display resolutions:

- VGA (640 x 480)
- SVGA (800 x 600)
- XGA (1024 x 768)
- SXGA (1280 x 1024)
- UXGA (1600 x 1200)

Timing specifications for respective resolutions are shown in this section. 60MHz mode of the VESA timing specification is adapted for VGA, SVGA and XGA. As for SXGA and UXGA, DISM original specifications are defined. (The specifications for SXGA and UXGA have not been defined yet.)

The parameters for timing specifications are defined in Figure 10.1.

Figure 10.1 Timing Specification Parameters



11. Software Specification

11.1 Overview

This chapter explains the specification required for DISM compatible system that the host system reads monitor information in order to set optimal configuration.

In order to achieve this specification, the method of data comminication is based on VESA DDC standard and its data format is based on VESA EDID 1.1 or 1.2.

11.2 Hardware Requirements

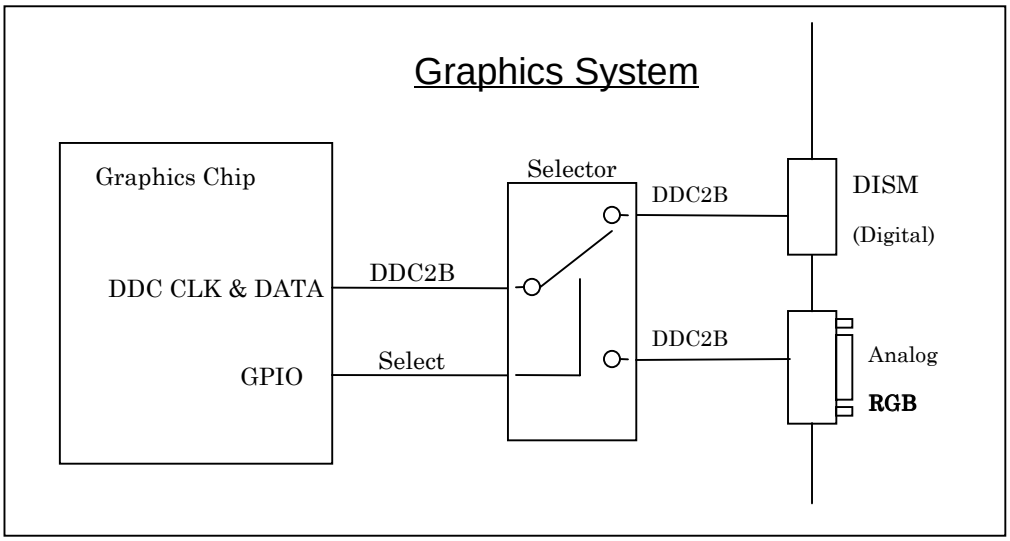
The host system may have one or more DISM compatible digital interfaces and an analog RGB connector on its system.

In the case where the host system is equipped with one DISM compatible connector, the DDC2B terminal of the graphics system can be connected directly to the DDC2B pin of a DISM connector.

In the case where the host system is equipped with more than one DISM compatible connector or a RGB connector, a selector must be used in order to avoid a conflict with the DDC data. (Refer to Figure 11.1). A selector must be designed to be controlled by the graphics system or host system. However, if the graphics system has more than one DDC2B terminals, a selector does not have to be used, and a DDC2B terminal may be connected to a DISM compatible connector.

Remark : USB usage is not specified here.

Figure 11.1 Example of DISM Compatible Host System



11.3 Detection of Display

This section defines the host system and the detection mechanism of the display system in order to avoid dangerous conditions (the un-suitable refresh rate, timing, data format, and so on) causing damage or destruction of the display.

11.3.1 Detection Mechanism - Host

When booting up the host system, the host reads EDID through DDC and then initializes graphics controller based on EDID information. The output from transmitter (LVDS, TMDS, GVIF) is disabled until the graphics controller is initialized.

If it fails to read EDID, it should report a malfunction by the beeping sound or other means.

Please refer to VESA standard for EDID and DDC.

Note: EDID and DDC are a trademark of VESA.

Remark : A host system should try re-detecting display for at least 30 seconds.

11.3.2 EDID

11.3.2.1 Overview

This chapter describes LCD Monitor timing definitions.

11.3.3.2 Host – Monitor Interface Requirements

DISM supports EDID 1.1 and 1.2. VESA standard 60Hz mode is recommended for the timing setting (Horizontal/Vertical addressable area, Vertical Front/Back porch, Vertical sync time, Horizontal Front/Back porch, Horizontal sync time) that monitor supports.

Please refer to the VESA standards for EDID specification and usage.

If a specific display mode in EDID is not supported, the graphics controller should convert this display mode to the supportable mode. The conversion is either scaling or centering.

11.4 Hot Plugging

The DISM compatible host system and display must protect themselves from physical and electronic damages and must be able to display normal images as hot plugging, if the display cable is disconnected and connected at or after system starting.

Also SENS signal can be used to detect disconnection and connection status, the host system is interrupted by using SENS signal if host system needs to detect disconnection and connection status of a display cable.

12. Mechanical Physical Specifications

12.1 Introduction

This Chapter defines five connector types, which support the three interface standards.

Table 12.1 shows the section and figure number for each connector's physical specifications.

MDR or equivalent connectors can be used for these standards.

Table 12.1 Connector Specifications Reference

	Plug	Receptacle	Bracket	Mating
Standard 1 (26 pin Connector)	12.2.1(1)	12.2.2(1)		12.6
Standard 1 (20 pin Connector)	12.2.1(2)	12.2.2(2)		12.6
Standard 2a	12.3.1	12.3.2	12.3.3	12.6
Standard 2b	12.4.1	12.4.2		12.6
Standard 3	12.5.1	12.5.2		12.6

12.2 Standard 1 Connector

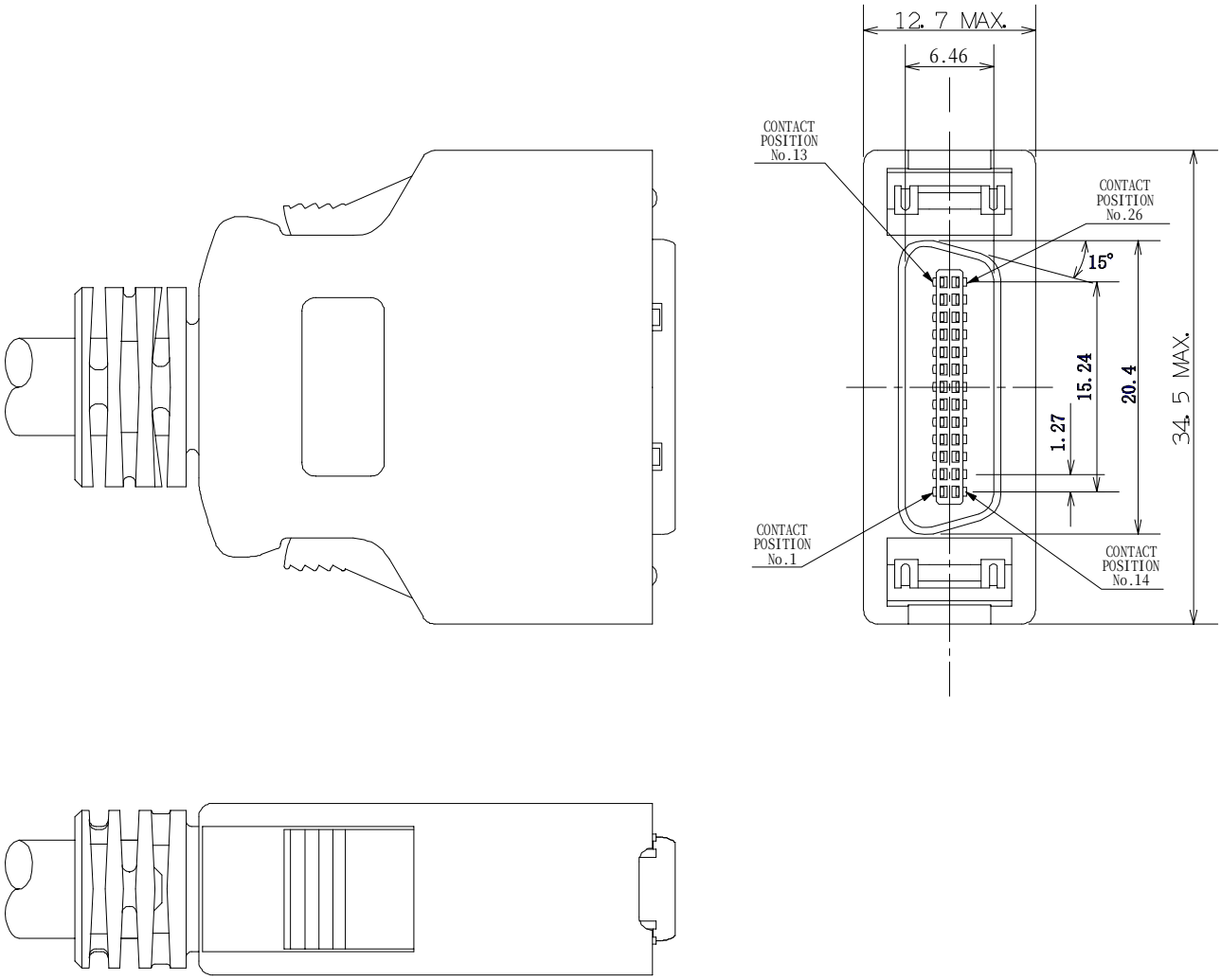
This section defines a connector specification, which supports standard 1. It includes 20 and 26-position connector.

12.2.1 Plug Connector

(1) 26 position Plug Connector

Refer to table 12.1 for compatible receptacle connectors

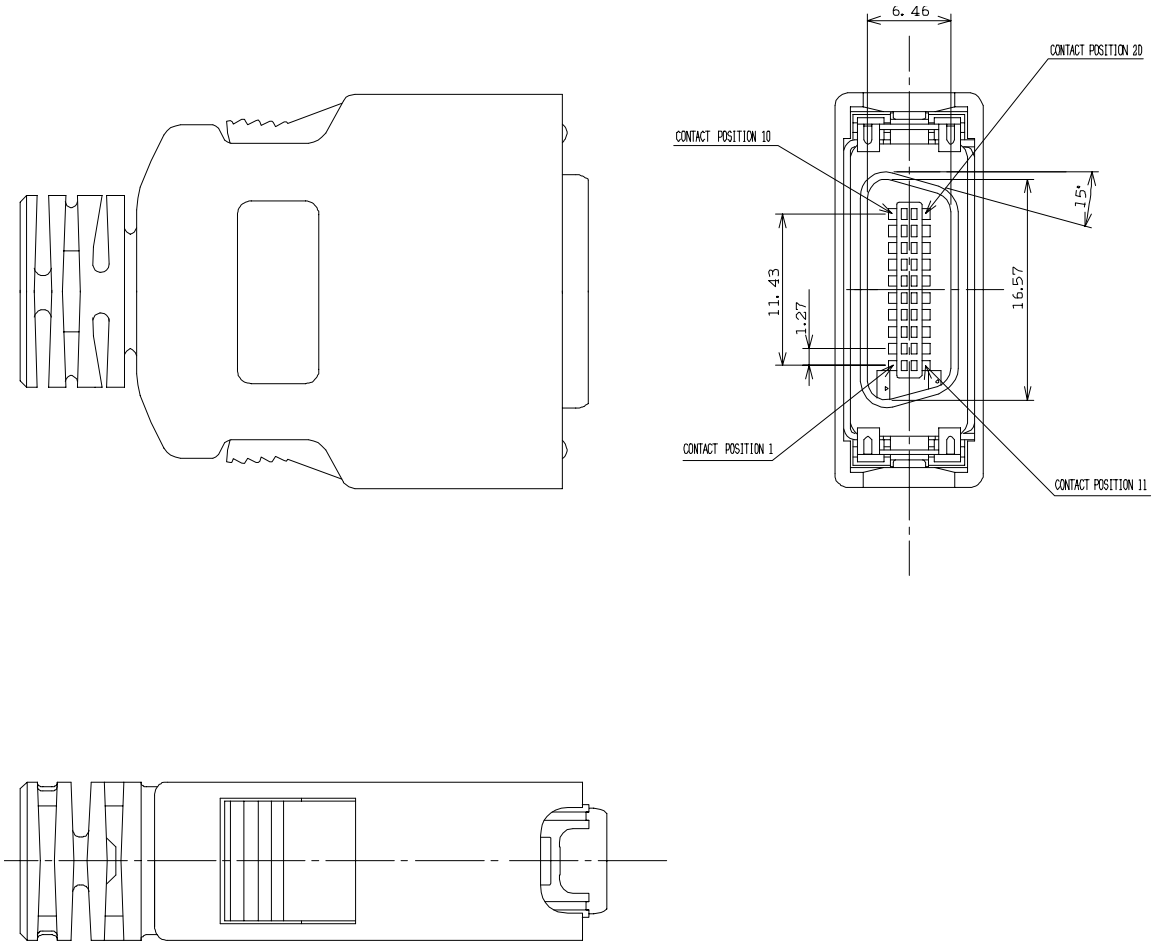
Figure 12.1 26 position Plug Connector which supports standard 1



(2) 20 position Plug Connector

Refer to the table 12.1 for compatible receptacle.

Figure 12.2 20 position Plug Connector which supports standard 1

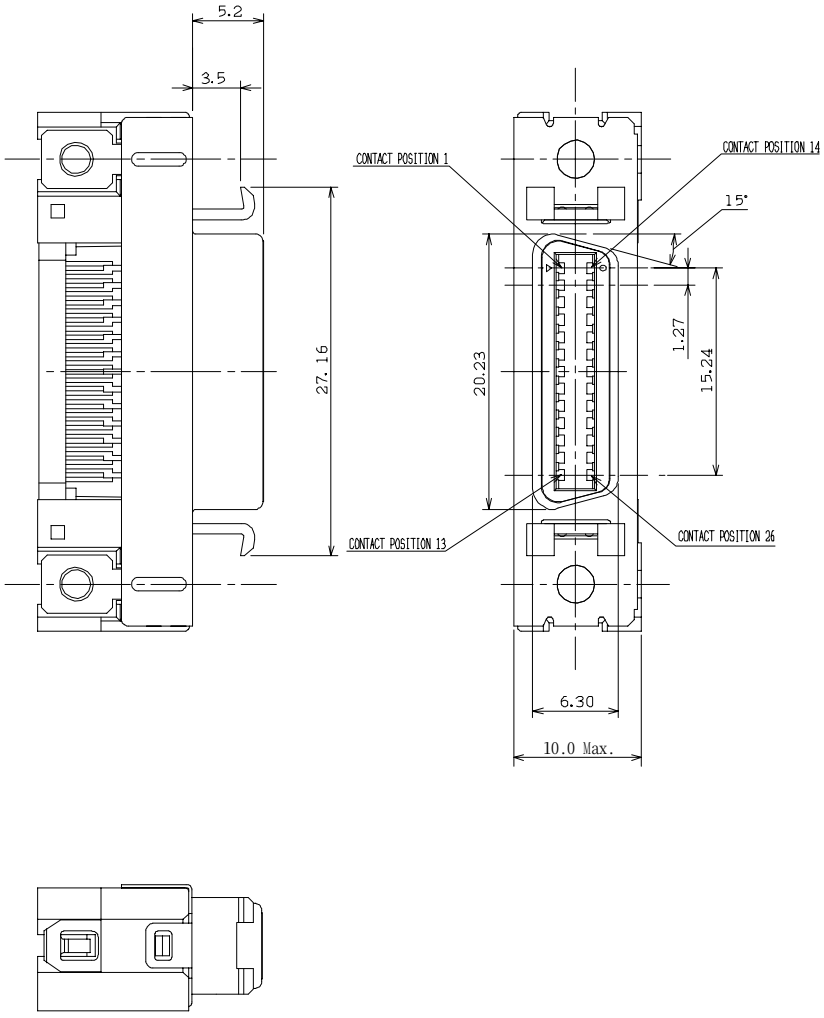


12.2.2 Receptacle Connector

(1) 26 position Receptacle Connector

Refer to table 12.1 for compatible plug connector.

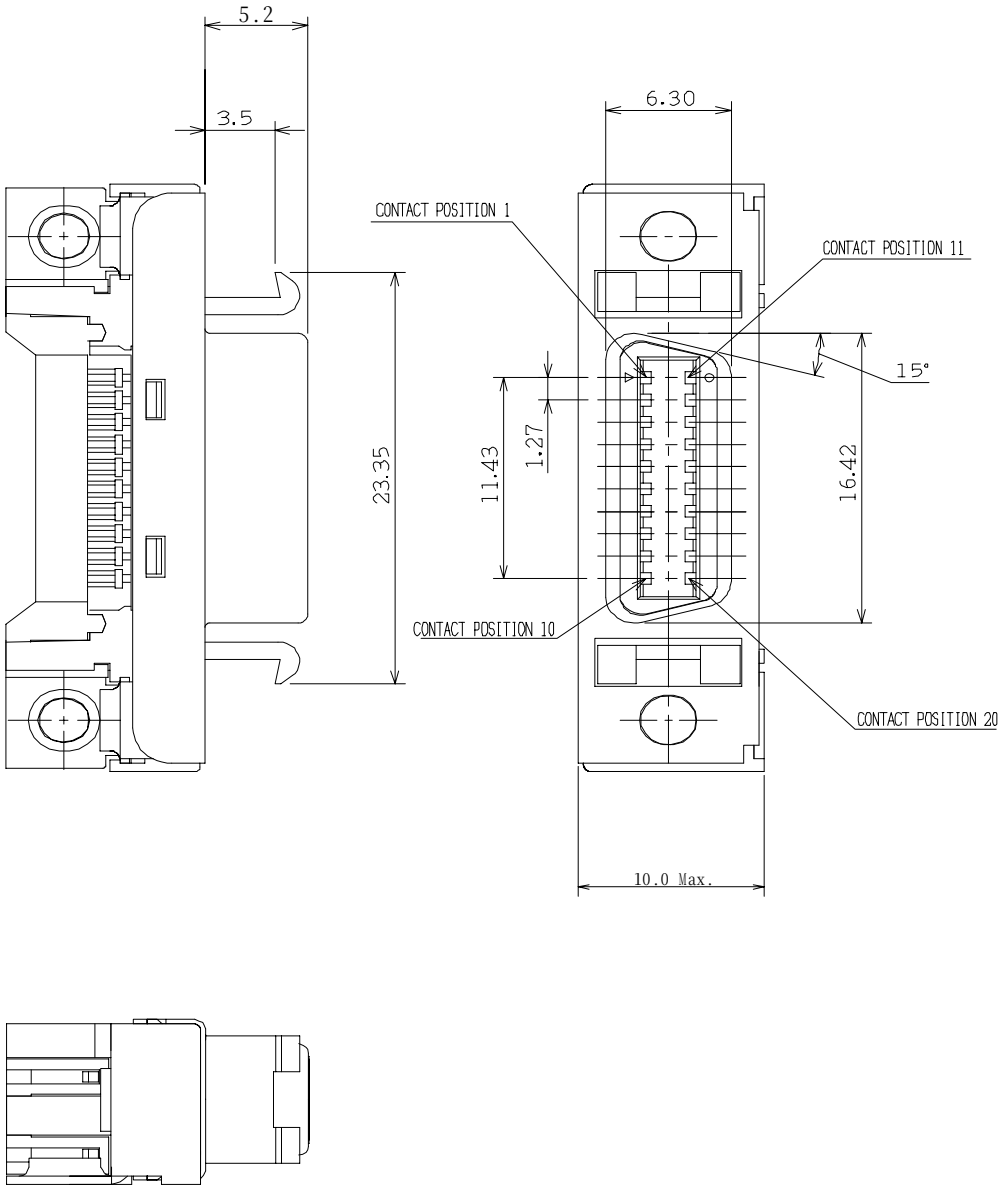
Figure 12.3 26 position Receptacle Connector which supports standard 1



(2) 20 position Receptacle Connector

Refer to the table 12.1 for compatible plug.

Figure 12.4 20 position Receptacle Connector which supports standard 1



12.3 Connector for Standard 2a

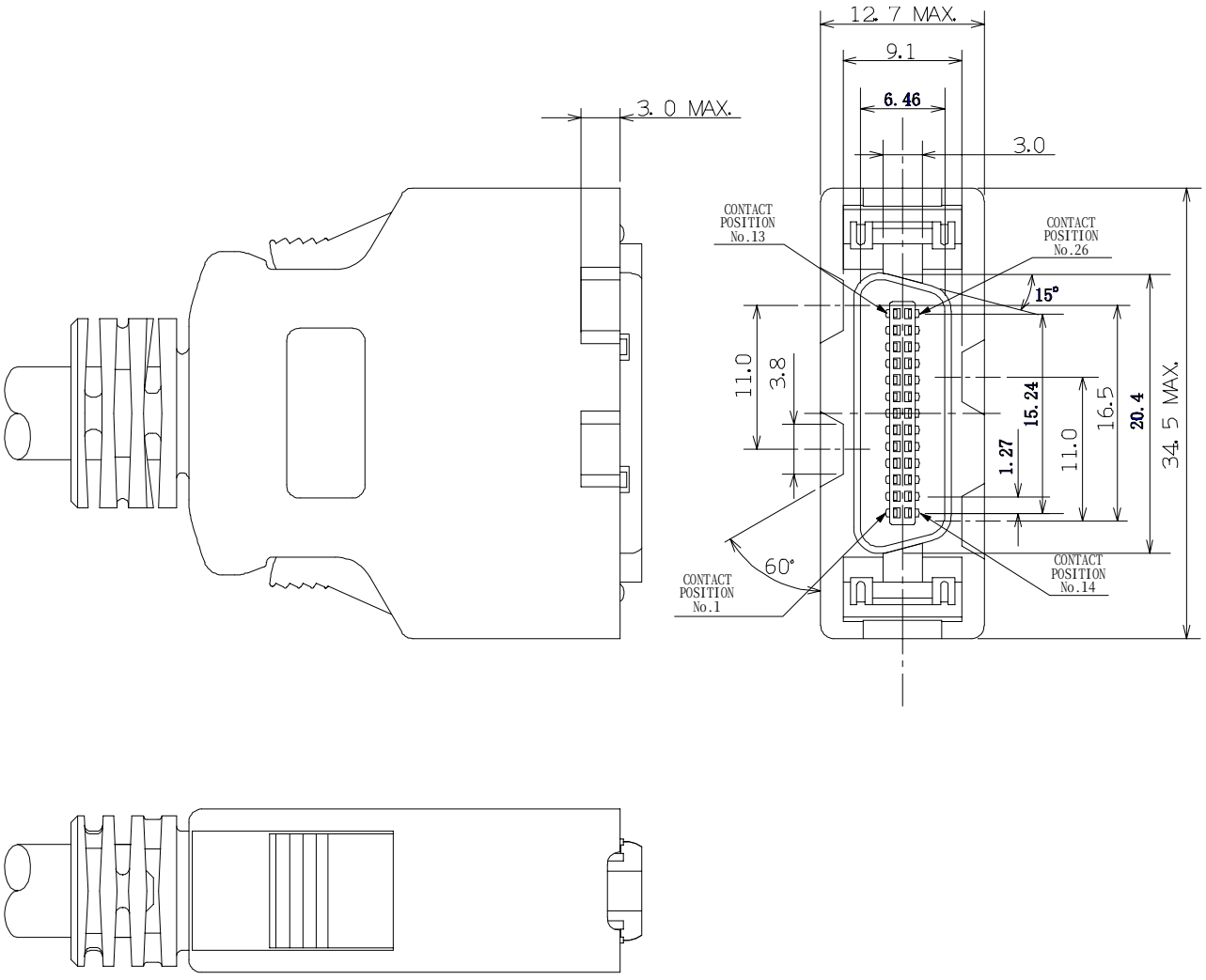
This section defines a connector specification to support standard 2a.

12.3.1 Plug Connector

26 position Plug Connector with Polarization Key

Refer to table 12.1 for compatible receptacle connector and polarization key bracket. Figure of insertion polarization key system is shown in section 12.7.

Figure 12.5 26 position Plug Connector with Polarization for standard 2a



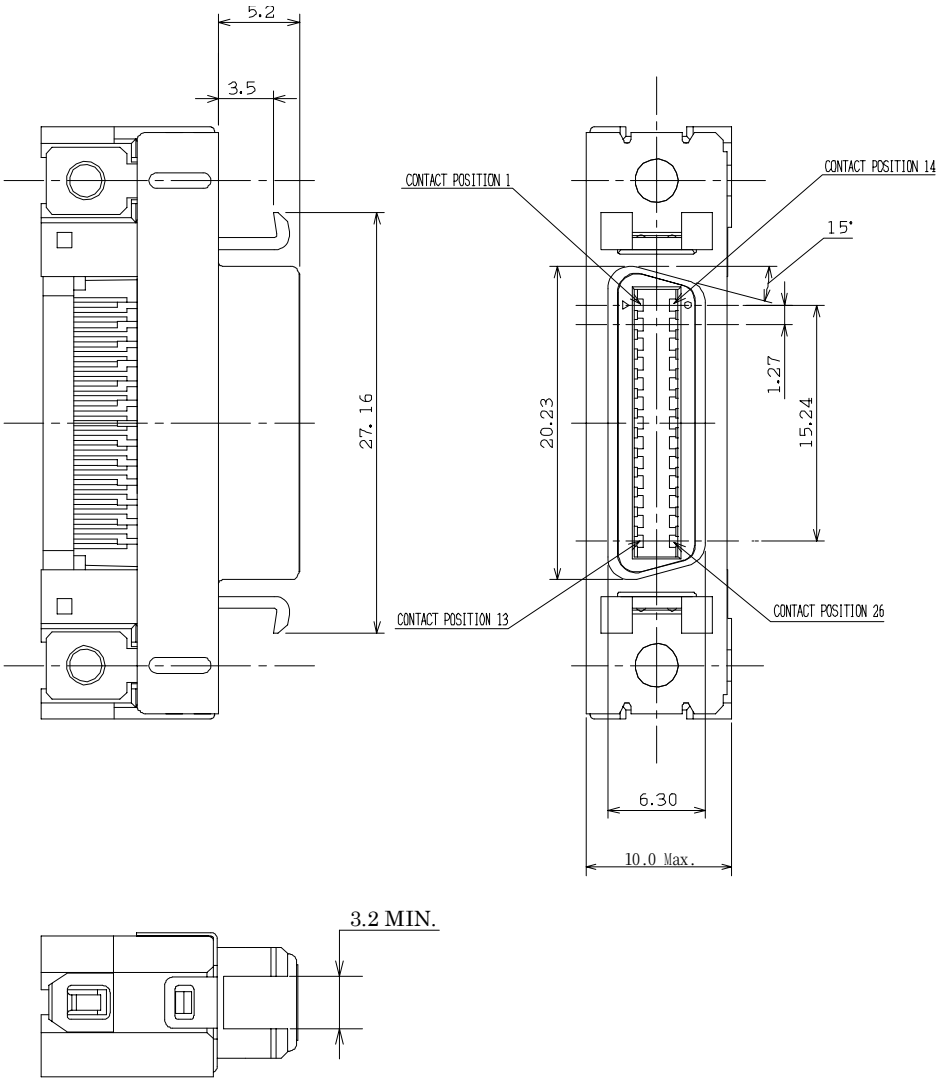
12.3.2 Receptacle Connector

26 position Receptacle Connector with Polarization Key

Please refer to table 12.1 for compatible plug connector and polarization key bracket.

Figure of Polarization key mechanism is shown in section 12.7.

Figure 12.7 26 position Receptacle Connector which supports standard 2a

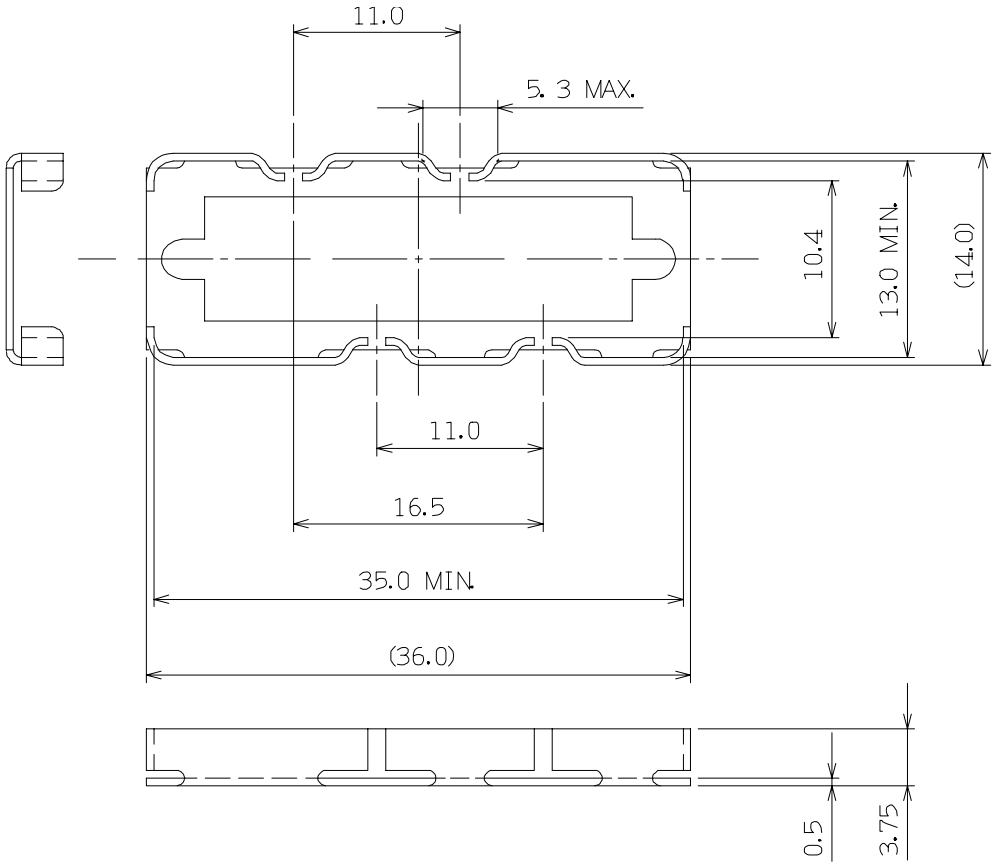


12.3.3 Bracket

Polarization bracket

The figure of the polarization key mechanism is shown in section 12.7. Refer to chart 12.1 for applicable plug and receptacle connector.

Figure 12.7 Bracket for Polarization Key System which supports standard 2a



12.4 Connector for Standard 2b

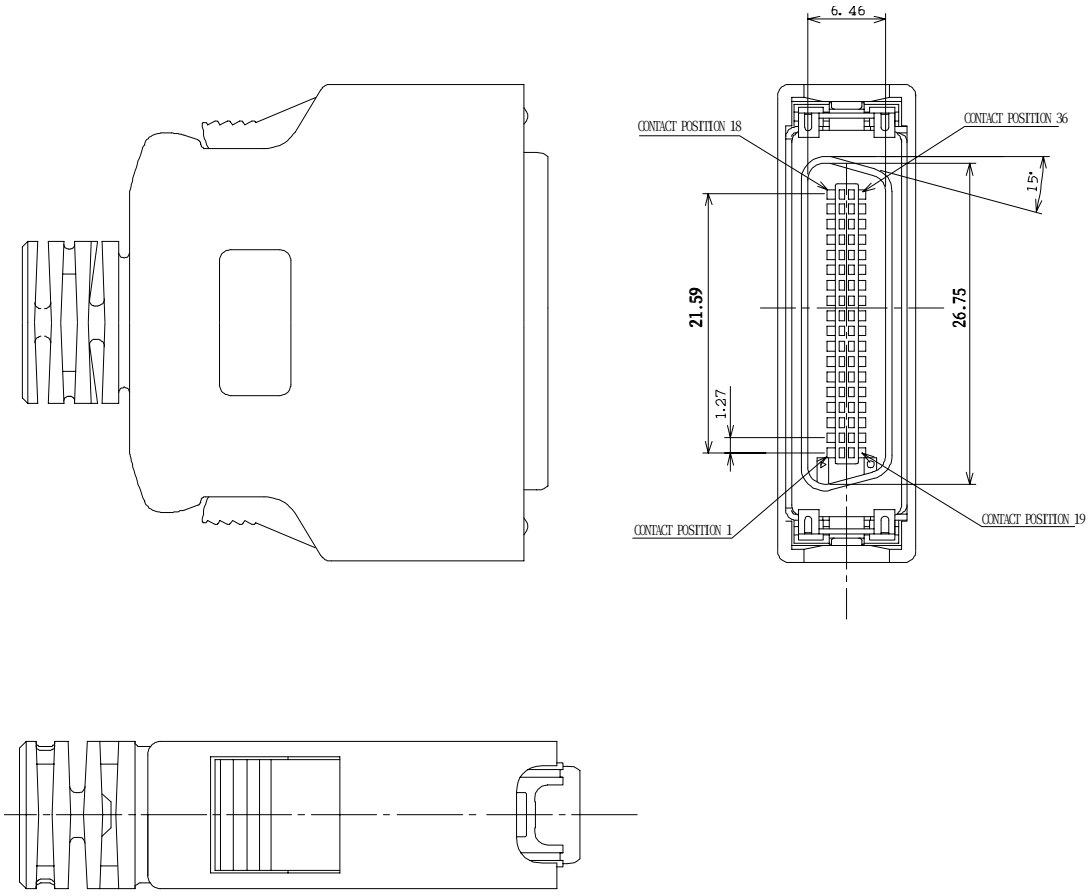
This section defines a connector specification to support standard 2b.

12.4.1 Plug Connector

36 position Plug Connector

Please refer to table 12.1 for compatible receptacle connector.

Figure 12.8 36 position Plug Connector which supports standard 2b

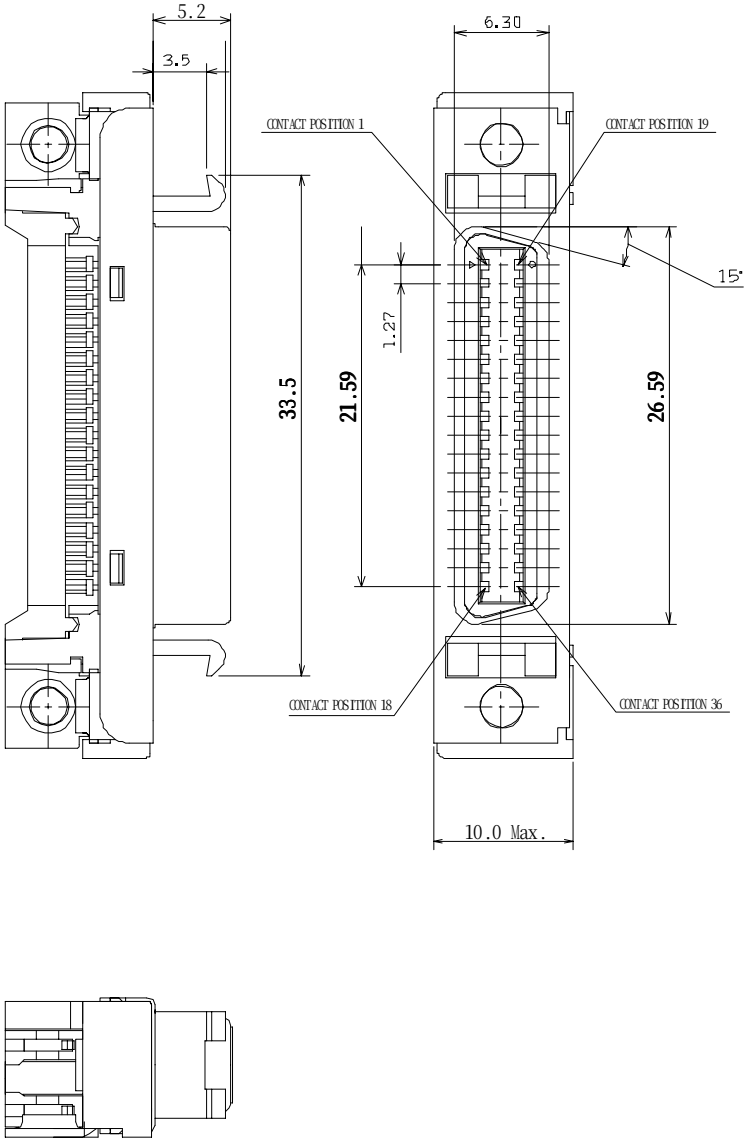


12.4.2 Receptacle connector

36 position Receptacle Connector.

Please refer to table 12.1 for compatible plug connector.

Figure 12.9 36 position Receptacle Connector which supports standard 2b



12.5 Connector for Standard 3

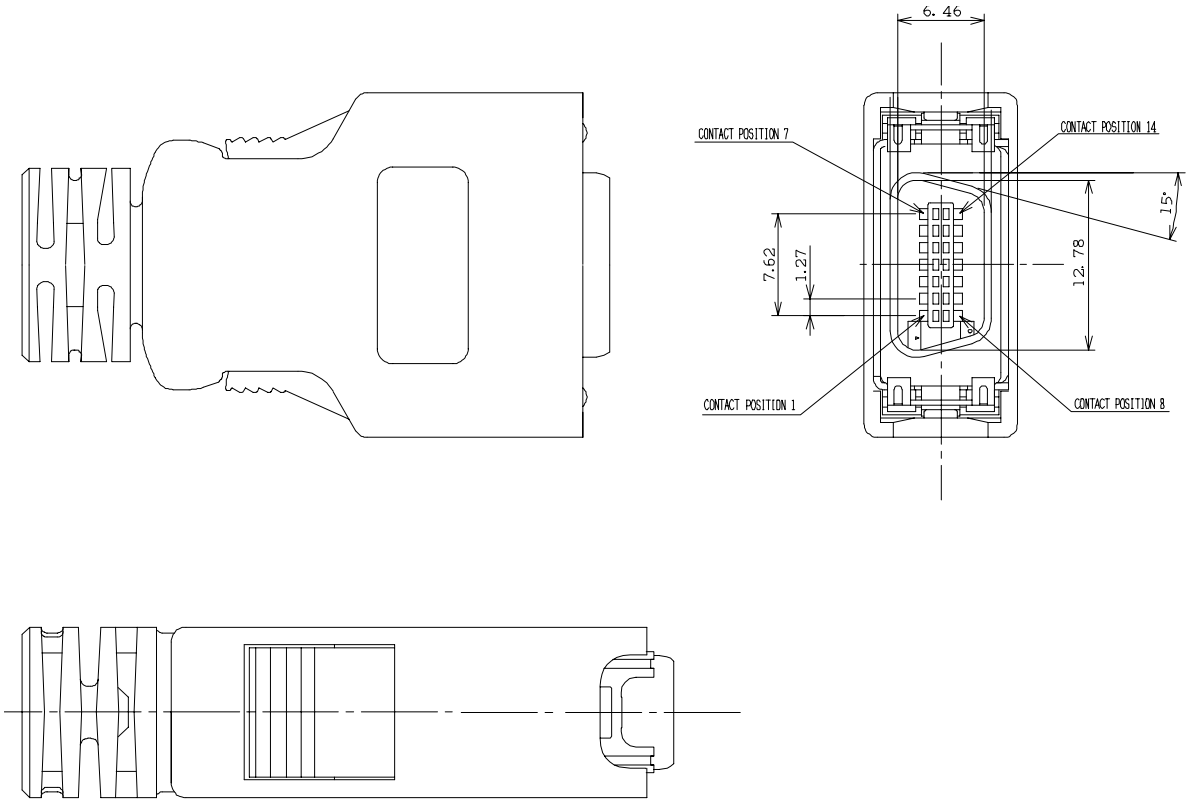
This section defines a connector specification to support standard 3.

12.5.1 Plug Connector

14 position Plug Connector

Please refer to table 12.1 for compatible receptacle connector.

Figure 12.10 14 position plug connector, which supports standard 3

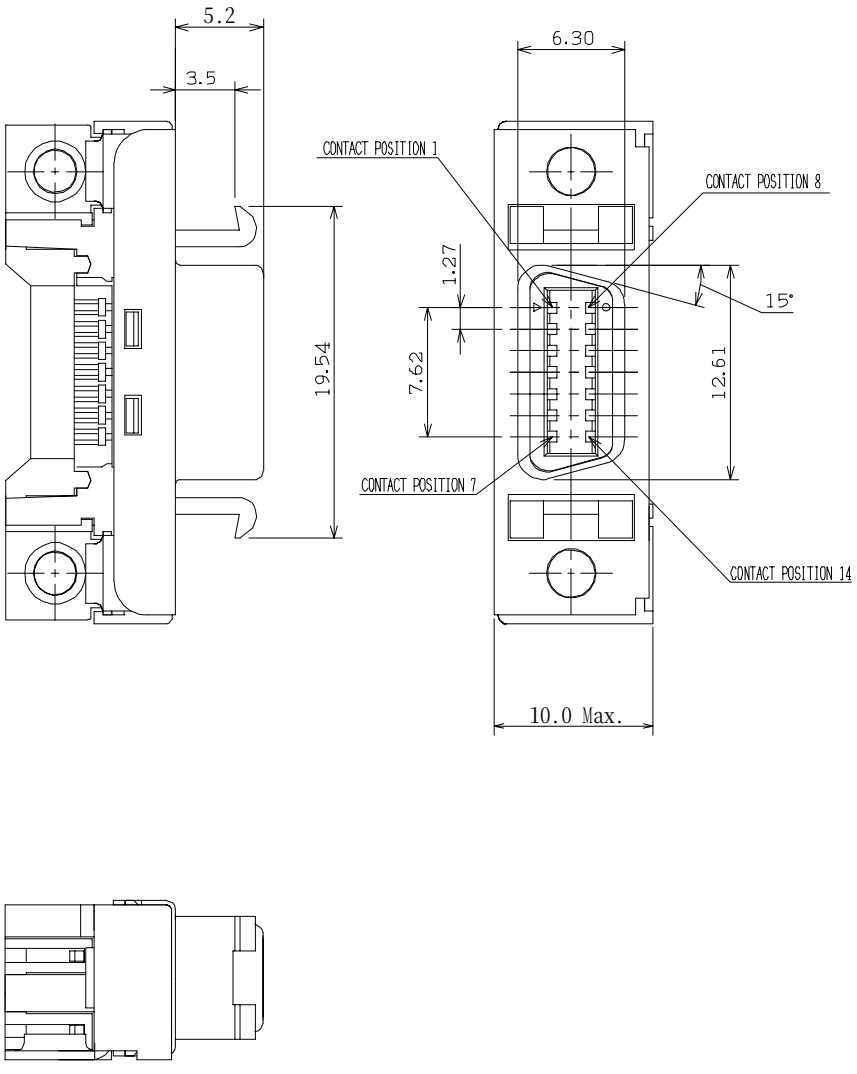


12.5.2 Receptacle connector

14 position Receptacle Connector

Please refer to table 12.1 for compatible plug connector.

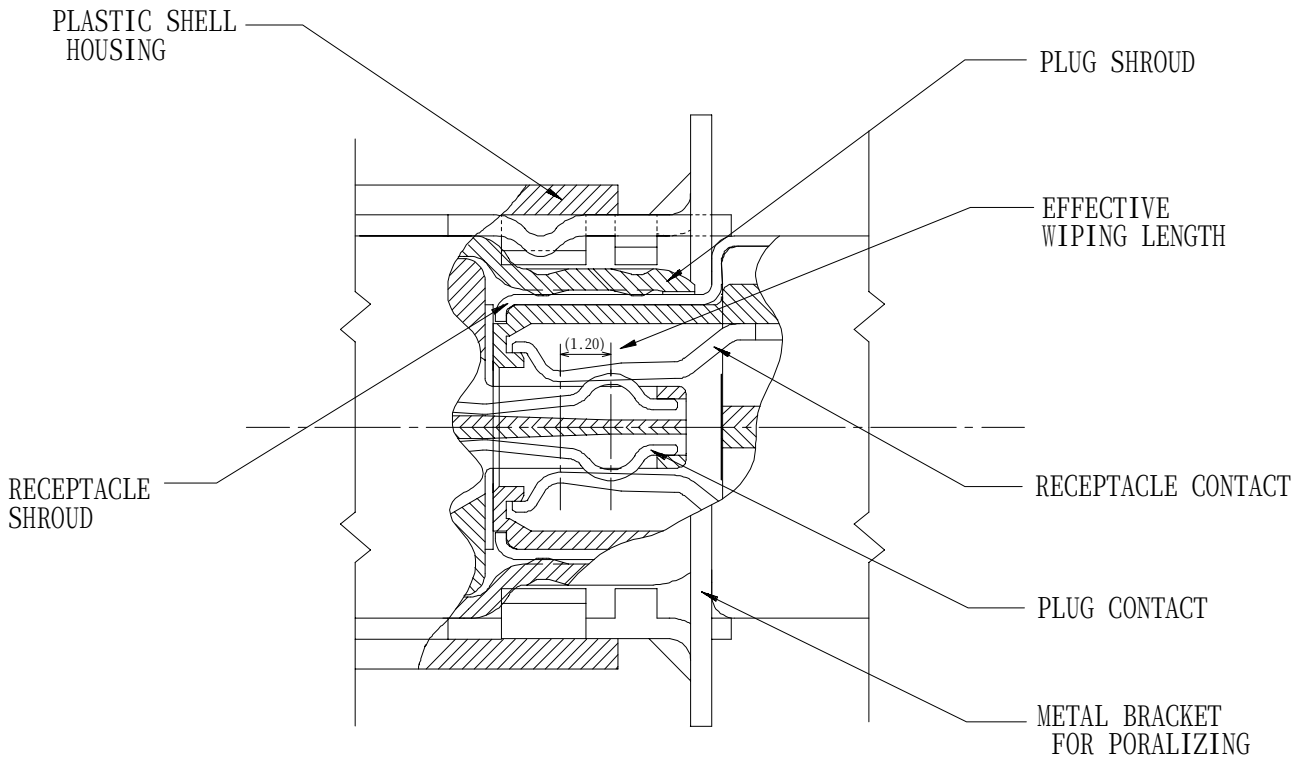
Figure 12.12 14 position Receptacle Connector which supports standard 3



12.6 Connector Mating Features

This section shows a cross section of the connector mating for 12.2, 12.3, 12.4, and 12.5.

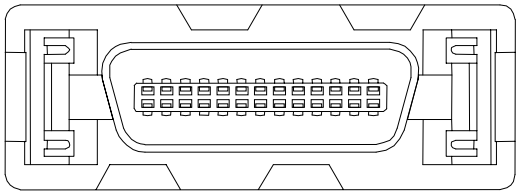
Figure 12.12 Connector Mating Cross Section (Reference)



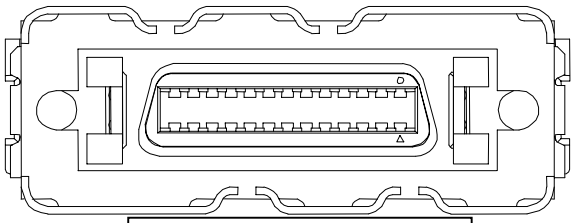
CONNECTOR MATING FEATURES

12.7 Polarization Key System

Figure 12.13 Polarization Key system structure



Plug Connector



Receptacle connector
and
Bracket

13. Display

The logo/icon marks are defined for DISM standard. They can be displayed in the devices compatible with this standard, and the logo mark must be displayed in the device that is described as compatible with this standard. To display the logo/icon mark, an approval is required which is stated in the "Guideline for Logo/Icon mark Usage" set forth other.

13.1 Logo mark

See the "Guideline for Logo/Icon mark Usage" for detail.

13.2 Icon mark

See the Guideline for Logo/Icon mark Usage" for detail.