On SPECIFICATION

NVIDIA Jetson TX1/TX2 Developer Kit Carrier Board

Abstract

This document contains recommendations and guidelines for Engineers to follow to create modules for the expansion connectors on the Jetson™ carrier board as well as understand the capabilities of the other dedicated interface connectors and associated power solutions on the platform.

Note: Jetson TX2 utilizes Tegra X2 which is a Parker series SoC.

CAUTION:

1. ALWAYS CONNECT JETSON MODULE & ALL EXTERNAL PERIPHERAL DEVICES BEFORE CONNECTING THE POWER SUPPLY TO THE AC POWER JACK. Connecting a device while powered on may damage the Developer Kit carrier board, Jetson module or peripheral device. In addition, the carrier board should be powered down and the power removed before plugging or unplugging devices or add-on modules into the headers. Wait for the red power VDD_IN LED (See Figure 1) to turn off, or wait for 5 minutes if your system does not have a power LED. This includes the Jetson module, the camera & display headers, the M.2 connector, the PCIe® x4 connector, SATA & the other expansion headers. For the PCIex4 & SATA connector, also wait for the PCIe/SATA 12V LED to turn off (See Figure 1)

2. The NVIDIA® Jetson Developer Kit carrier board contains ESD-sensitive parts. Always use appropriate anti-static and grounding techniques when working with the system. Failure to do so can result in ESD discharge to sensitive pins, and irreparably damage your Jetson carrier board. NVIDIA will not replace units that have been damaged due to ESD discharge.

Document Change History

Date	Description
MAY, 2017	Initial Release
JUN, 2017	**M.2, Key E Expansion Slot** - Updated figure, Pin Descriptions table & notes to show I2C on pins 58/60 at 1.8V level by default. **Display** - Changed headings to to make DSI & DP/eDP sections more clear - Corrected lane order in eDP Connection example figure in eDP Connector block.
JUN, 2017	**Expansion Header & GPIO Expansion Header** - Updated main tables o Removed column for device connected and put the information in the notes instead. o Added column for signal voltage level at header & updated note 3 to mention voltage selector jumper J24. - Added tables for Jetson TX1 & TX2 to provide signal details (Name, Tegra Ball, Tegra GPIO, POR, etc.)
OCT, 2017	**Introduction** - Updated introduction paragraph(s)

NVIDIA.

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1.0 INTRODUCTION

The NVIDIA® Jetson Developer Kit carrier board is ideal for software development within the Linux environment. Standard connectors are used to access Jetson module features and interfaces, enabling a highly flexible and extensible development platform. (Jetson Developer Kits are not intended for production purposes.)

Go to https://developer.nvidia.com/embedded-computing for access to JetPack SDK. Use the JetPack installer to flash your Jetson Developer Kit with the latest OS image, to install developer tools for both host PC and Developer Kit, and to install the libraries and APIs, samples, and documentation needed to jumpstart your development environment.

1.1 Jetson Module Feature List

Applications Processor
- Tegra X1 or Tegra X2

Memory
- LPDDR4 DRAM & eMMC 5.1
- Memory sizes for DDR & eMMC vary depending on module – Check relevant Data Sheet

Network
- 10/100/1000 BASE-T Ethernet

Connectivity
- Dual U.FL RF connectors: Connects to 802.11a/b/g/n/ac WLAN/Bluetooth enabled devices.

Advanced power management
- Dynamic voltage and frequency scaling
- Multiple clock and power domains
- Thermal Transfer Plate & optional Fan/Heatsink

1.2 Carrier Board Feature List

Connection to Jetson Module
- 400-pin (8x50) Board-Board Connector

Storage
- Full Size SD Card Slot
- SATA Connector (Power & TX/RX)

USB
- USB 2.0 Micro AB (Host & Device)
- USB 3.0 Type A (Host only)

Wired Network
- Gigabit Ethernet (RJ45 Connector w/LEDs)

PCIe
- Standard PCIe® x4 connector

Display Expansion Header
- 120-pin (2x60) Board-Board
- DSI (2x4 lanes)
- eDP/DP/HDMI
- Backlight: PWM/Control
- Touch: SPI/I2C

HDMI Type A

Camera Expansion Header
- 120-pin (2x60) Board-Board
- CSI: 6, x2 – 3, x4
- Camera CLK, I2C & Control
- I2S, UART, SPI, Digital Mic (Jetson TX2 only)

M.2 Key E Connector
- PCIe x1 Lane, SDIO (Jetson TX1 only), USB 2.0
- I2S, UART, I2C, Control

Expansion Header
- 40-pin (2x20) header
- I2C, SPI, UART, I2S, Audio Clock/Control
- D-MIC (Jetson TX2 only)

GPIO Expansion Header
- 30-pin (2x15) header
- I2S, GPIOs, Digital Speaker (Jetson TX2 only)

UI & Indicators
- Power, Reset & Force Recovery Buttons
- LEDs: Main DC input, Main 3.3V (Power)/SOC Enables, M.2 Activity, PCIe/SATA 12V rail

Debug/Serial
- JTAG Connector (Standard 20-pin header)
- Debug Connector
  - 60-pin (2x30) Board-Board
  - JTAG, UART, I2C, Power, Reset & Recovery
- Serial Port Signals (1x6 header)

Miscellaneous
- Fan Connector: 5V, PWM & Tach

Power
- DC Jack: 5.5V-19.6V
- Main 3.3V/5V Buck Supplies: 2xTPS53015
- Main 1.8V Buck Supply: APW8805
- USB VBUS Load Switches: RT9715 & APL3511
- 12V Boost (PCIe & SATA): LM3481
- Load Switches/LDOs (SD/HDMI/Display/Camera)
- Charge Control Header: 10-pin Flex Receptacle

Developer Kit Operating Temperature Range
- 0ºC to 50ºC

1.3 Jetson Carrier Board Block Diagram

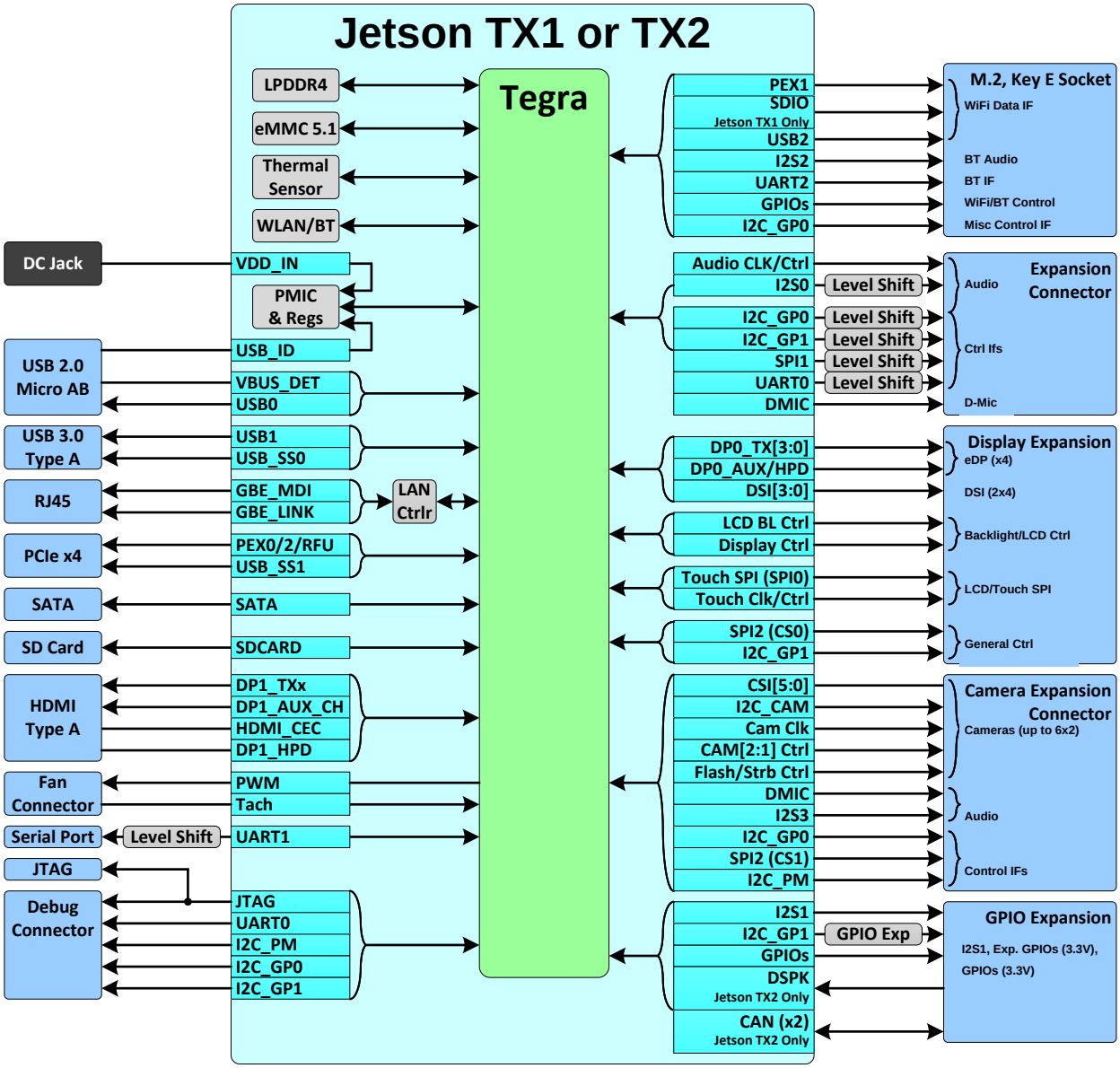
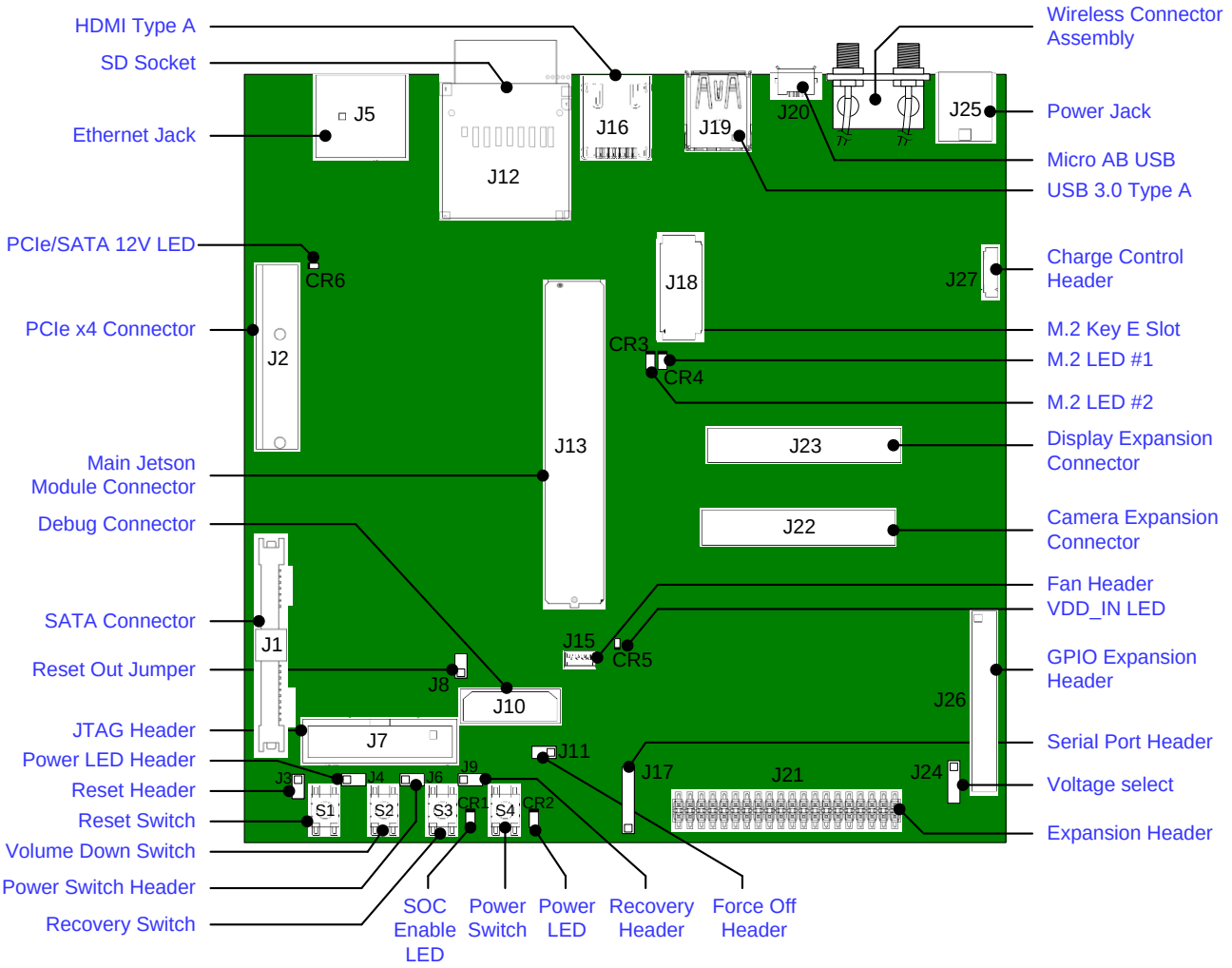
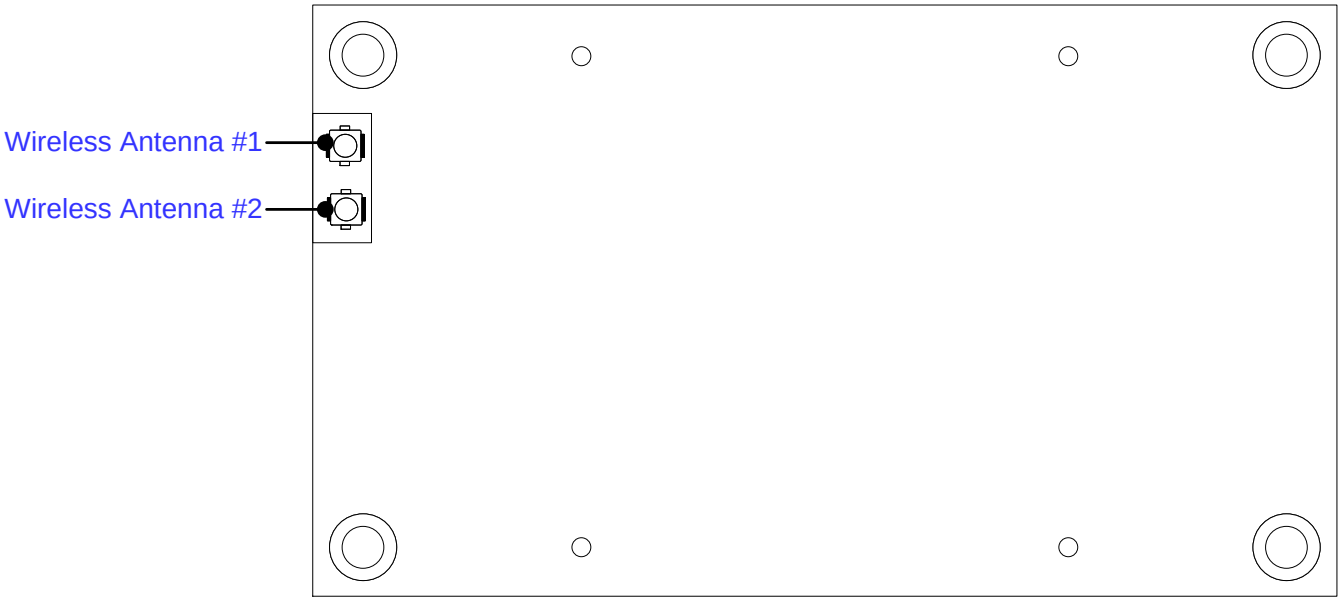


Figure 1. Jetson Carrier Board Placement (Top View)



J1	SATA Connector (22-pin Inc. Power)
J2	PCIe x4 Connector
J3	Reset Switch Header (1x2, 2.54mm pitch)
J4	Power LED Header (1x2, 2.54mm pitch)
J5	RJ45 Ethernet Jack
J6	Power Switch Header (1x2, 2.54mm pitch)
J7	JTAG Header (2x10, 2.54mm pitch)
J8	Reset Out Header (1x2, 2.54mm pitch)
J9	Force Recovery Header (1x2, 2.54mm pitch)
J10	Debug Connector (2x30, 0.5mm pitch)
J11	Force Off Header (1x2, 2.54mm pitch)
J12	SD Socket (Full Size)
J13	Main Module Connector (8x50, 1.27mm pitch)
J14	Reserved
J15	Fan Header (4-pin, 1.25mm pitch)
J16	HDMI Type A
J17	Serial Port Header (1x6, 2.54mm pitch)
J18	M.2 Key E Connectivity Socket (75-pin)
J19	USB 3.0 Type A
J20	Micro AB USB
J21	Expansion Header (2x20, 2.54mm pitch)
J22	Camera Expansion Connector (2x60, 0.5mm pitch)
J23	Display Expansion Connector (2x60, 0.5mm pitch)
J24	Voltage select for SPI/I2C Level Shifter (1x3, 2.54mm pitch)
J25	Power Jack
J26	GPIO Expansion Header (2x15, 2.54mm pitch)
J27	Charge Control Header (10-pin Flex Recep., 0.8mm pitch)
S1	Reset Switch
S2	Volume Down (Sleep) Switch
S3	Recovery Switch
S4	Power Switch
CR1	SOC Enable LED (Green)
CR2	Power LED (Green)
CR3	M.2 LED #2 (Green)
CR4	M.2 LED #1 (Green)
CR5	VDD_IN LED (Red)
CR6	PCIe/SATA 12V LED (Red)

Figure 2. Jetson TX1/TX2 Wireless Connector Placement (Top View)



2.0 JETSON CARRIER BOARD STANDARD CONNECTORS

The Jetson carrier board provides a number of standard expansion connectors to support additional functionality beyond what is integrated on the main platform board. This includes:

- USB 2.0: Micro AB Connector
- USB 3.0: Type A Connector
- Gigabit Ethernet: RJ45 Connector
- SATA: Standard SATA Connector, 22-pin including power
- SD Card (Full size) Connector/Cage
- HDMI: Type A Connector
- M.2, Key E Socket
- PCIe® x4 Connector
- JTAG header, 2x10, 2.54mm pitch

2.1 USB Ports

The carrier board supports two USB Connectors. One is a USB 2.0 Micro AB connector (J20) supporting Device/Host modes as well as USB Recovery mode. The other is a USB 3.0 Type A connector (J19) supporting Host mode only.

Figure 3. USB Port Connections

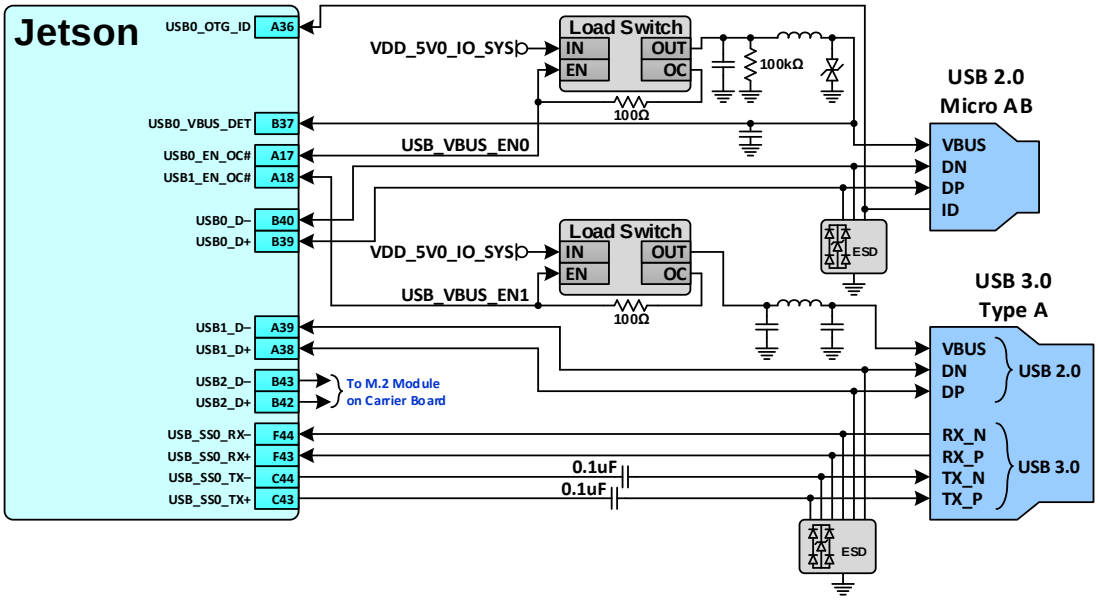


Table 1. USB 2.0 Micro AB & USB 3.0 Type A Connector Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
USB 2.0 Micro AB				
1	VBUS	–	VBUS Supply	Power
2	USB0_IO_CONN_D_N	USB0_D–	USB 2.0 #0 Data -	Bidir
3	USB0_IO_CONN_D_P	USB0_D+	USB 2.0 #0 Data +	Bidir
4	USB0_ID_IO_CONN	USB0_OTG_ID	USB 2.0 #0 Identification	Input
5	GND	–	Ground	Ground
USB 3.0 Type A				
1	VBUS	–	VBUS Supply	Power
2	USB1_D_N	USB1_D–	USB 2.0 #1 Data -	Bidir
3	USB1_D_P	USB1_D+	USB 2.0 #1 Data +	Bidir
4	GND	–	Ground	Ground

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
5	USB3_RX1_N	USB_SS0_RX–	USB 3.0 #0 Receive -	Input
6	USB3_RX1_P	USB_SS0_RX+	USB 3.0 #0 Receive +	Input
7	GND	–	Ground	Ground
8	USB3_TX1_N	USB_SS0_TX–	USB 3.0 #0 Transmit -	Output
9	USB3_TX1_P	USB_SS0_TX+	USB 3.0 #0 Transmit +	Output

Legend	Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to USB Connectors. Input is from USB Connectors. Bidir is for Bidirectional signals.

2.2 Gigabit Ethernet

The carrier board implements an RJ45 connector (J5) along with the necessary magnetics device.

Figure 4. Gigabit LAN Connections

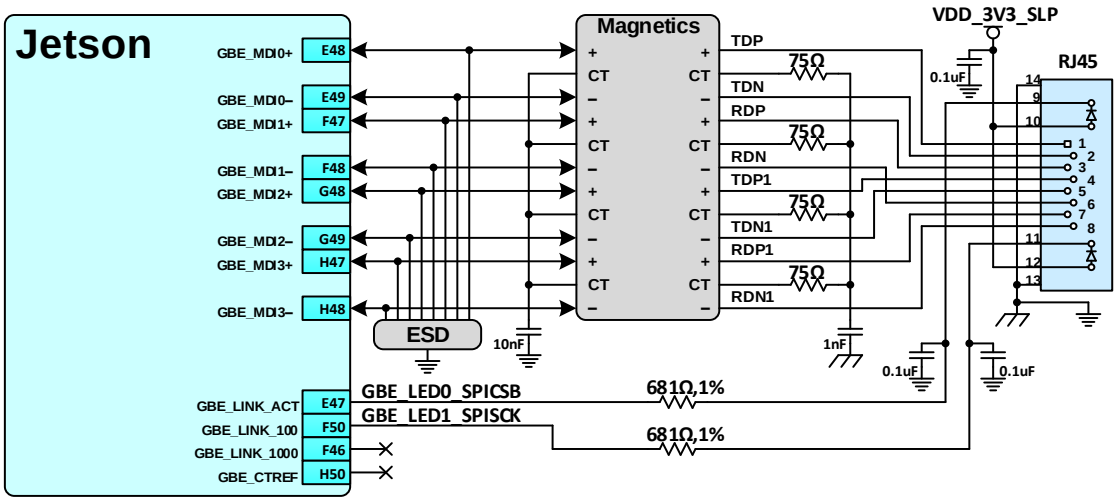


Table 2. Ethernet RJ45 Connector Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	RJ45_TDP	GPE_MDI0+	Gigabit Ethernet MDI 0+	Bidir
2	RJ45_TDN	GPE_MDI0–	Gigabit Ethernet MDI 0–	Bidir
3	RJ45_RDP	GPE_MDI1+	Gigabit Ethernet MDI 1+	Bidir
4	RJ45_TDP1	GPE_MDI2+	Gigabit Ethernet MDI 2+	Bidir
5	RJ45_TDN1	GPE_MDI2–	Gigabit Ethernet MDI 2–	Bidir
6	RJ45_RDN	GPE_MDI1–	Gigabit Ethernet MDI 1–	Bidir
7	RJ45_RDP1	GPE_MDI3+	Gigabit Ethernet MDI 3+	Bidir
8	RJ45_RDN1	GPE_MDI3–	Gigabit Ethernet MDI 3-	Bidir
9	GBE_LED0_SPICSB	GBE_LINK_ACT	Connected to LED #1 through resistor	Output OD
10	LED1A	–	Connected to VDD_3V3_SYS	–
11	GBE_LED1_SPISCK	GBE_LINK100	Connected to LED #2 through resistor	Output OD
12	LED2A	–	Connected to VDD_3V3_SYS	–
13	NC/GND	–	Ground	Ground
14	NC/GND	–	Ground	Ground

Legend	Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to RJ45 Connector. Input is from RJ45 Connector. Bidir is for Bidirectional signals.

2.3 SATA

The Jetson carrier board has a standard SATA connector (J1 - both Data & Power) as shown below.

Figure 5. SATA Connections

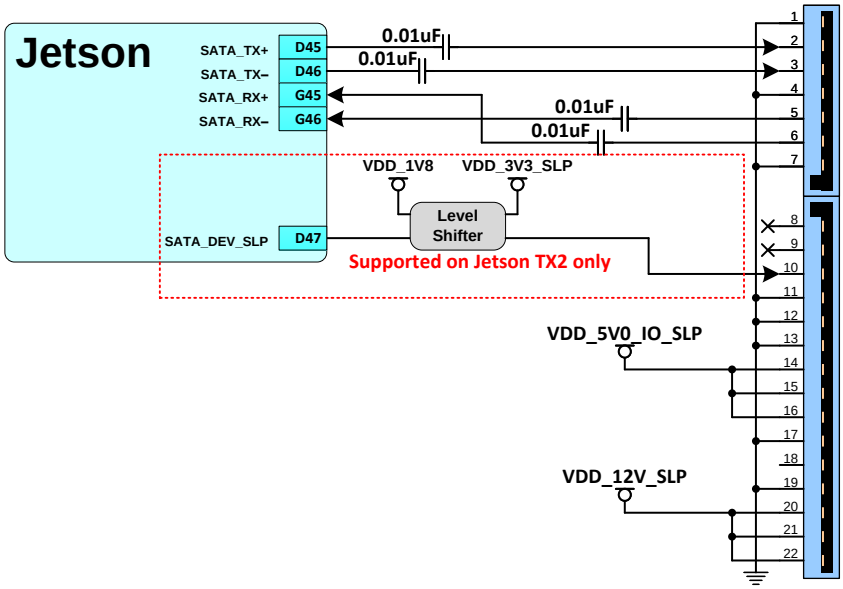


Table 3. SATA Connector Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir
1	GND	–	Ground	Ground	8	NC	–	Unused	Unused
2	SATA_TX_C_P	SATA_TX+	SATA Transmit+	Output	9	NC	–	Unused	Unused
3	SATA_TX_C_N	SATA_TX–	SATA Transmit–	Output	10	SATA_DEV_SLP	SATA_DEV_SLP	SATA Device Sleep	Output
4	GND	–	Ground	Ground	11	GND	–	Ground	Ground
5	SATA_RX_C_N	SATA_RX–	SATA Receive–	Input	12	GND	–	Ground	Ground
6	SATA_RX_C_P	SATA_RX+	SATA Receive+	Input	13	GND	–	Ground	Ground
7	GND	–	Ground	Ground	14	VDD_5V0_IO_SLP	–	Gated version of Main 5.0V Supply	Power
					15	VDD_5V0_IO_SLP	–		Power
					16	VDD_5V0_IO_SLP	–		Power
					17	GND	–	Ground	Ground
					18	NC	–	Unused	Unused
					19	GND	–	Ground	Ground
					20	VDD_12V_SLP	–	12V Supply (From Boost on carrier board)	Power
					21	VDD_12V_SLP	–		Power
					22	VDD_12V_SLP	–		Power

Legend	Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to SATA Connector. Input is from SATA Connector. Bidir is for Bidirectional signals.

2.4 SD Card

A full size SD Card (J12) is implemented, supporting up to SDR104 mode (UHS-1).

Figure 6. SD Card Connections

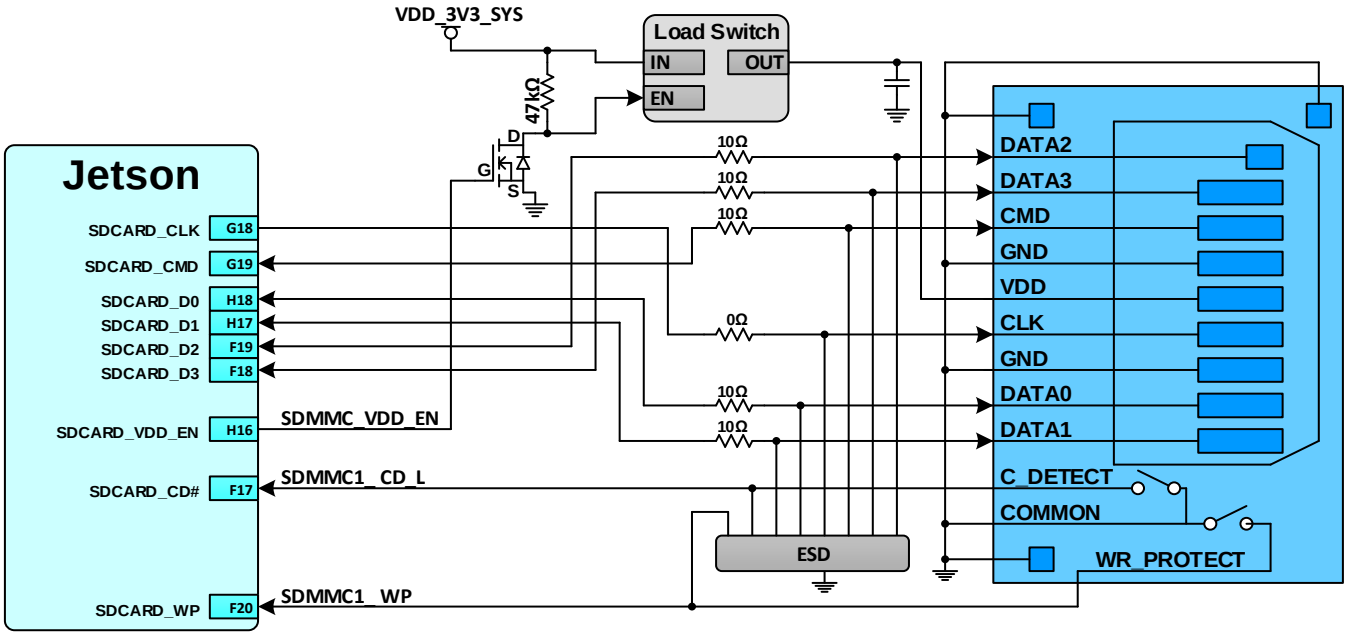


Table 4. SD Card Socket Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	SDCARD_DAT3	SDCARD_D3	SD Card Data #3	Bidir
2	SDCARD_CMD	SDCARD_CMD	SD Card Command	Bidir
3	GND	–	Ground	Ground
4	SD_CARD_SW_PWR	–	SD Card Power	Power
5	SDCARD_CLK	SDCARD_CLK	SD Card Clock	Output
6	GND	–	Ground	Ground
7	SDCARD_DAT0	SDCARD_D0	SD Card Data #0	Bidir
8	SDCARD_DAT1	SDCARD_D1	SD Card Data #1	Bidir
9	SDCARD_DAT2	SDCARD_D2	SD Card Data #2	Bidir
10	SDCARD_CD*	SDCARD_CD#	SD Card, Card Detect	Input
11	GND	–	Ground	Ground
12	SDCARD_WP	SDCARD_WP	SD Card Write Protect	Input
13	GND	–	Ground	Ground
14	GND	–	Ground	Ground
15	GND	–	Ground	Ground

Legend

Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to SD Card Socket. Input is from SD Card Socket. Bidir is for Bidirectional signals.

2.5 HDMI

A standard HDMI type A connector (J16) is supported.

Figure 7. HDMI Connections

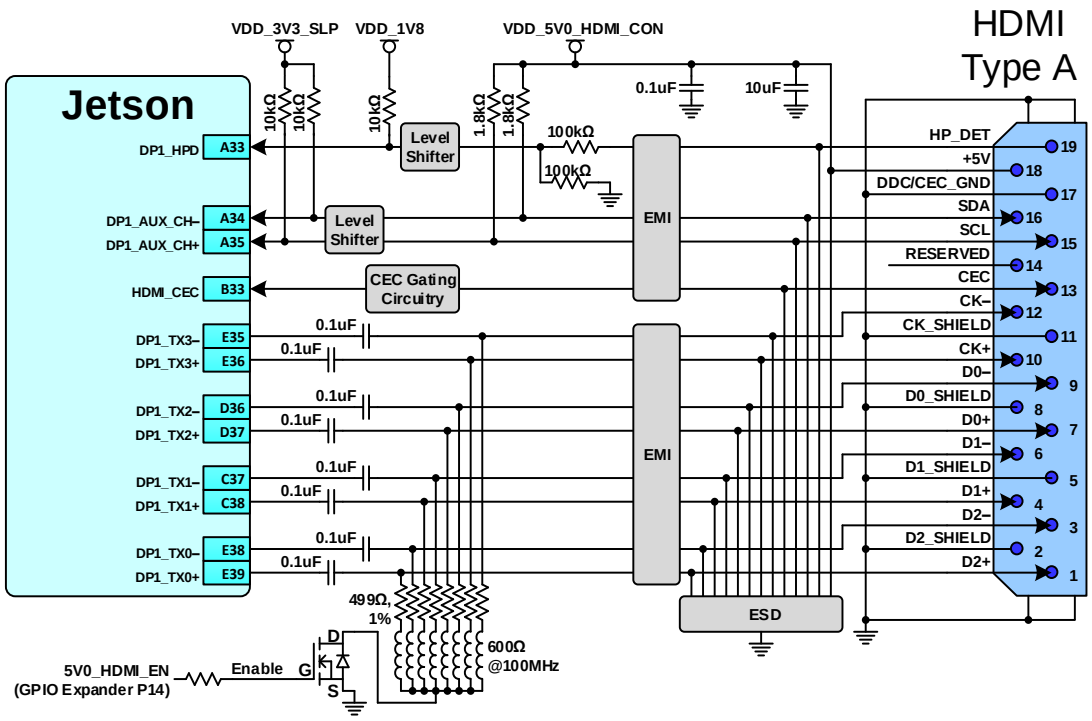


Table 5. HDMI Connector Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	HDMI_TXD2_CON_P	DP1_TXD0+	HDMI Transmit Data 2+	Output
2	SHIELD/GND	–	Ground	Ground
3	HDMI_TXD2_CON_N	DP1_TXD0–	HDMI Transmit Data 2–	Output
4	HDMI_TXD1_CON_P	DP1_TXD1+	HDMI Transmit Data 1+	Output
5	SHIELD/GND	–	Ground	Ground
6	HDMI_TXD1_CON_N	DP1_TXD1–	HDMI Transmit Data 1–	Output
7	HDMI_TXD0_CON_P	DP1_TXD2+	HDMI Transmit Data 0+	Output
8	SHIELD/GND	–	Ground	Ground
9	HDMI_TXD0_CON_N	DP1_TXD2–	HDMI Transmit Data 0–	Output
10	HDMI_TXC_CON_P	DP1_TXD3+	HDMI Transmit Clock+	Output
11	SHIELD/GND			
12	HDMI_TXC_CON_N	DP1_TXD3–	HDMI Transmit Clock–	Output
13	HDMI_CEC_CON	HDMI_CEC	HDMI CEC	Bidir
14	RESERVED	–	Unused	Unused
15	HDMI_DDC_SCL_5V0	DP1_AUX_CH+	HDMI DDC Clock	Output /OD
16	HDMI_DDC_SDA_5V0	DP1_AUX_CH–	HDMI DDC Data	Bidir/OD
17	GND	–	Ground	Ground
18	VDD_5V0_HDMI_CON	–	HDMI 5V Power	Power
19	HDMI_HPD_CON	DP1_HPD	Hot Plug Detect	Input

Legend

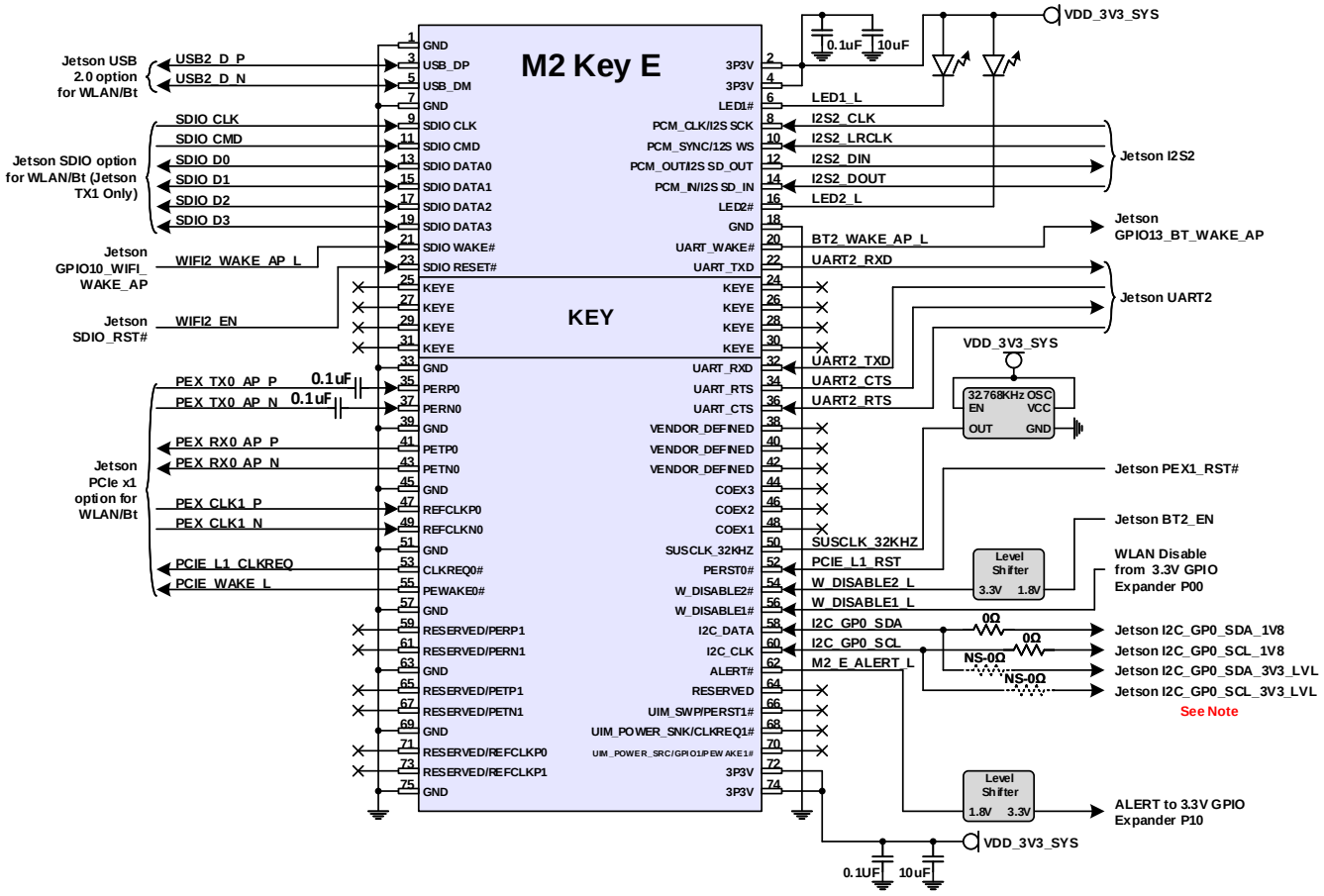
Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to HDMI Connector. Input is from HDMI Connector. Bidir is for Bidirectional signals.

2.6 M.2, Key E Expansion Slot

The Jetson carrier board includes a M.2, Key E Slot Mini-PCIe Expansion slot (J18). This includes interface options for WLAN/BT including PCIe (x1), SDIO (4-bit, Jetson TX1 only), USB 2.0, UART, I2S & I2C. The connections & power rails associated with the connector are shown in the figure below.

Figure 8. M.2 Key E Connections



Note: The I2C IF on pins 58 & 60 come by default directly from the Jetson I2C_GP0 (1.8V signaling). Stuffing resistors can be changed to bring the I2C interface after a level shifter (3.3V signaling). For earlier versions of the M.2 Key E revision spec. (prior to revision 1.1), the I2C interface used 3.3V signaling levels. The 1.1 revision changes this to 1.8V signaling levels.

Table 6. M.2, Key E Expansion Slot Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	GND	–	Ground	Ground		–	–	–	–
3	USB2_D_P	USB2_D+	USB 2.0 Data +	Bidir	2	VDD_3V3_SYS	–	Main 3.3V Supply	Power
5	USB2_D_N	USB2_D–	USB 2.0 Data -	Bidir	4	VDD_3V3_SYS			
7	GND	–	Ground	Ground	6	LED1_L	–	LED #1 (CR4 – Green)Enable	Output
9	SDIO_CLK	SDIO_CLK	SDIO Clock	Output	8	I2S2_CLK	I2S2_CLK	I2S #2 Clock	Bidir
11	SDIO_CMD	SDIO_CMD	SDIO Command	Bidir	10	I2S2_LRCLK	I2S2_LRCLK	I2S #2 Left/Right Clock	Bidir
13	SDIO_DAT0	SDIO_D0	SDIO Data 0	Bidir	12	I2S2_SDIN	I2S2_SDIN	I2S #2 Data In	Input
15	SDIO_DAT1	SDIO_D1	SDIO Data 1	Bidir	14	I2S2_SDOUT	I2S2_SDOUT	I2S #2 Data Out	Bidir
17	SDIO_DAT2	SDIO_D2	SDIO Data 2	Bidir	16	LED2_L	–	LED #2 (CR3 – Green) Enable	Output
19	SDIO_DAT3	SDIO_D3	SDIO Data 3	Bidir	18	GND	–	Ground	Ground
21	WIFI2_WAKE_AP_L	GPIO10_WIFI_WAKE_AP	WLAN #2 Wake AP	Input	20	BT2_WAKE_AP_L	GPIO13_BT_WAKE_AP	Bluetooth #2 Wake AP	Input
23	WIFI2_EN	SDIO_RST	WLAN #2 Enable	Output	22	UART2_RXD	UART2_RX	UART #2 Receive	Input

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
25	NC (Key)	–	Unused	Unused	24	NC (Key)	–	Unused	Unused
27	NC (Key)				26	NC (Key)			
29	NC (Key)				28	NC (Key)			
31	NC (Key)				30	NC (Key)			
33	GND	–	Ground	Ground	32	UART2_TXD	UART2_TX	UART #2 Transmit	Output
35	PEX_TX0_AP_P	PEX1_TX+	PCIe #1 Transmit +	Output	34	UART2_CTS	UART2_CTS#	UART #2 Clear to Send	Input
37	PEX_TX0_AP_N	PEX1_TX–	PCIe #1 Transmit -	Output	36	UART2_RTS	UART2_RTS#	UART #2 Request to Send	Output
39	GND	–	Ground	Ground	38	NC	–	Unused	Unused
41	PEX_RX0_AP_P	PEX1_RX+	PCIe #1 Receive +	Input	40	NC			
43	PEX_RX0_AP_N	PEX1_RX–	PCIe #1 Receive -	Input	42	NC			
45	GND	–	Ground	Ground	44	NC			
47	PEX_CLK1_P	PEX1_REFCLK+	PCIe #1 Reference clock +	Output	46	NC			
49	PEX_CLK1_N	PEX1_REFCLK–	PCIe #1 Reference clock -	Output	48	NC			
51	GND	–	Ground	Ground	50	SUSCLK_32KHZ	–	Suspend Clock (32KHz)	Output
53	PCIE_L1_CLKREQ	PEX1_CLKREQ#	PCIe #1 Clock Request	Bidir	52	PCIE_L1_RST	–	PCIe Reset	Output
55	PCIE_WAKE_L	PEX_WAKE#	PCIe Wake	Input	54	W_DISABLE2_L	–	WLAN Disable #2	Output
57	GND	–	Ground	Ground	56	W_DISABLE1_L	–	WLAN Disable #1 (from 3.3V GPIO Exp. P00)	Output
59	NC	–	Unused	Unused	58	I2C_GP0_SDA_1V8	I2C_GP0_DAT	General I2C Interface #0 Data. See note.	Bidir/OD
61	NC				60	I2C_GP0_SCL_1V8	I2C_GP0_CLK	General I2C Interface #0 Clock. See note.	Bidir/OD
63	GND	–	Ground	Ground	62	M2_E_ALERT_L	–	M.2, Key E Connector Alert (to 3.3V GPIO Exp. P10)	Input
65	NC	–	Unused	Unused	64	NC	–	Unused	Unused
67	NC				66	NC			
69	GND	–	Ground	Ground	68	NC			
71	NC	–	Unused	Unused	70	NC			
73	NC				72	VDD_3V3_SYS	–	Main 3.3V Supply	Power
75	GND	–	Ground	Ground	74	VDD_3V3_SYS			

Legend

Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes:
- In the Type/Dir column, Output is to M.2 Module. Input is from M.2 Module. Bidir is for Bidirectional signals.
- Prior to the M.2 Key E revision 1.1 spec., the I2C interface was referenced to 3.3V. The 1.1 revision changes this to 1.8V. By default, the carrier board connects these pins to the 1.8V level I2C interface. Stuffing resistors can be changed to connect to the I2C interface through level shifters for 3.3V operation instead.

Table 7. M.2 Related Carrier Board PCB Trace Delays

Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for M.2 Module (ps)		Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for M.2 Module (ps)	
PCIe					**SDIO**		**≤ SDR50**	**>SDR50**	**≤ SDR50**	**>SDR50**
PEX1_RX+	539	880	341		SDIO_CLK	230	876	521	646	291
PEX1_RX–	539	880	342		SDIO_CMD	223	876	521	653	298
PEX1_TX+	518	880	362		SDIO_D0	222	876	521	654	299
PEX1_TX–	519	880	361		SDIO_D1	222	876	521	654	299
PEX1_REFCLK+	178	880	702		SDIO_D2	225	876	521	651	296
PEX1_REFCLK–	178	880	702		SDIO_D3	240	876	521	636	281
USB					**I2S**		**All**	**na**	**All**	**na**
USB2_D+	171	960	789		I2S2_CLK	970	3600		2630	
USB2_D–	172	960	788		I2S2_LRCLK	967	3600		2633	
					I2S2_SDIN	931	3600		2669	
					I2S2_SDOUT	924	3600		2676	

Notes: The SDIO interface is not available on the Jetson TX2.

2.7 PCIe x4 Connector

The Jetson carrier board includes a standard 4-lane PCIe connector (J2).

Figure 9. PCIe 4-lane Connector Connections

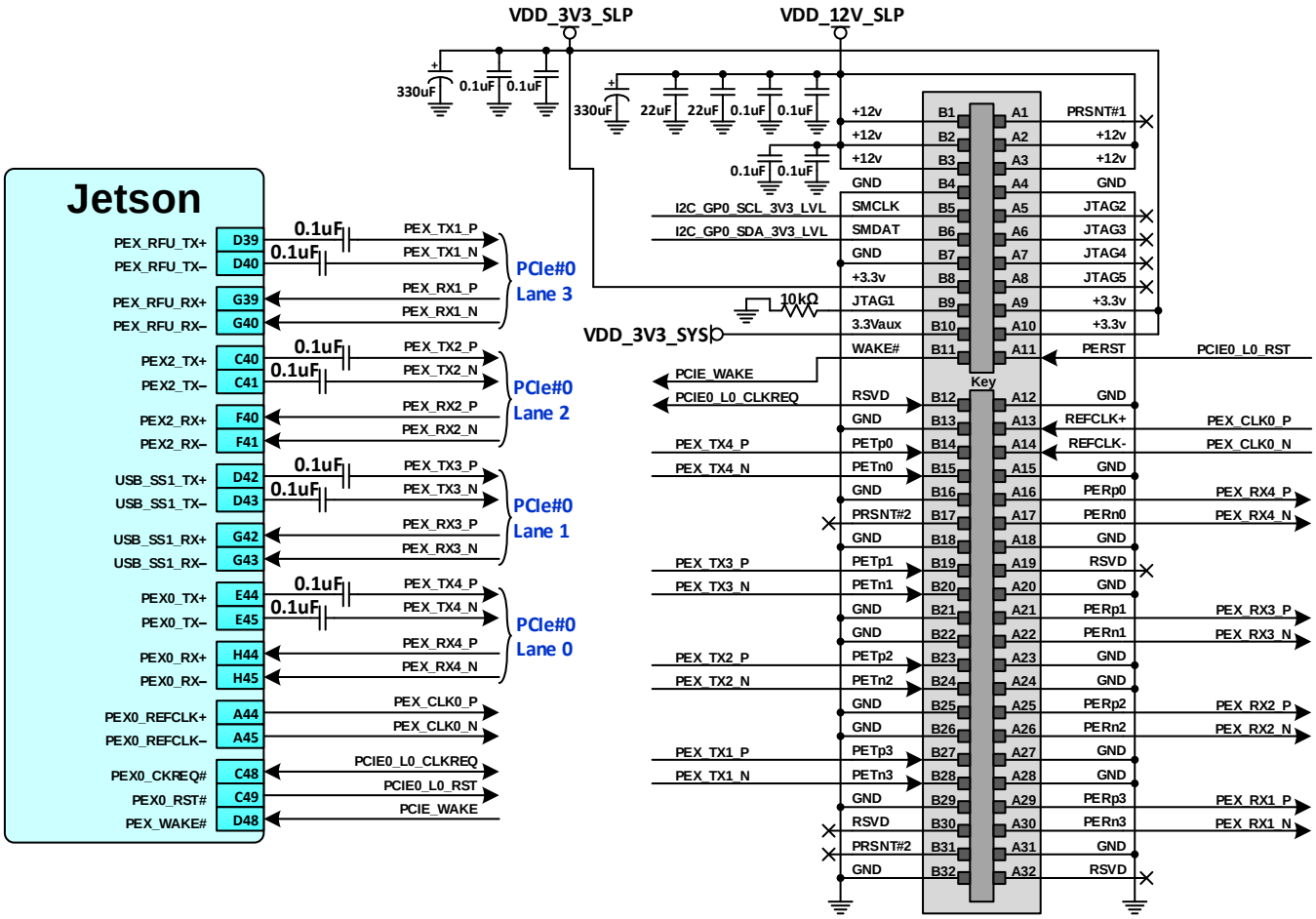


Table 8. PCIe 4-lane Connector Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/ Direction
A1	GND (PRSNT1)	–	Ground	Ground	B1	VDD_12V_SLP	–	12V Supply	Power
A2	VDD_12V_SLP	–	12V Supply (Boost)	Power	B2	VDD_12V_SLP			
A3	VDD_12V_SLP				B3	VDD_12V_SLP			
A4	GND	–	Ground	Ground	B4	GND	–	Ground	Ground
A5	NC	–	Unused	Unused	B5	GEN1_I2C_SCL_3V3_LVL	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD
A6	NC				B6	GEN1_I2C_SDA_3V3_LVL	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD
A7	NC				B7	GND	–	Ground	Ground
A8	NC				B8	VDD_3V3_SLP	–	3.3V supply – off in Deep Slp	Power
A9	VDD_3V3_SLP	–	3.3V supply - off in Deep Slp	Power	B9	PCIE_JTAG_TRST_PD	–	Pulled to GND	–
A10	VDD_3V3_SLP				B10	VDD_3V3_SYS	–	Main 3.3V Supply	Power
A11	PCIE0_L0_RST	PEX0_RST#	PCIe Lane 0 Reset	Output	B11	PCIE_WAKE	PEX_WAKE#	PCIe Wake (Shared)	Input
A12	GND	–	Ground	Ground	B12	PCIE0_L0_CLKREQ	PEX0_CLKREQ#	PCIe Ctlr 0 Clock Req.	Bidir
A13	PEX_CLK0_P	PEX0_REFCLK+	PCIe Ctlr 0 Reference Clock +	Output	B13	GND	–	Ground	Ground
A14	PEX_CLK0_N	PEX0_REFCLK–	PCIe Ctlr 0 Reference Clock –	Output	B14	PEX_TX4_C_P	PEX0_TX+	PCIe Ctlr 0 Lane 0 Transmit +	Output
A15	GND	–	Ground	Ground	B15	PEX_TX4_C_N	PEX0_TX–	PCIe Ctlr 0 Lane 0 Transmit –	Output
A16	PEX_RX4_P	PEX0_RX_P	PCIe Ctlr 0 Lane 0 Receive +	Input	B16	GND	–	Ground	Ground
A17	PEX_RX4_N	PEX0_RX–	PCIe Ctlr 0 Lane 0 Receive –	Input	B17	NC	–	Unused	Unused
A18	GND	–	Ground	Ground	B18	GND	–	Ground	Ground

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/ Direction	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/ Direction
A19	NC	–	Unused	Unused	B19	PEX_TX3_C_P	USB_SS1_TX+	PCIe Ctlr 0 Lane 1 Transmit +	Output
A20	GND	–	Ground	Ground	B20	PEX_TX3_C_N	USB_SS1_TX–	PCIe Ctlr 0 Lane 1 Transmit –	Output
A21	PEX_RX3_P	USB_SS1_RX+	PCIe Ctlr 0 Lane 1 Receive +	Input	B21	GND	–	Ground	Ground
A22	PEX_RX3_N	USB_SS1_RX–	PCIe Ctlr 0 Lane 1 Receive –	Input	B22	GND			
A23	GND	–	Ground	Ground	B23	PEX_TX2_C_P	PEX2_TX+	PCIe Ctlr 0 Lane 2 Transmit +	Output
A24	GND				B24	PEX_TX2_C_N	PEX2_TX–	PCIe Ctlr 0 Lane 2 Transmit –	Output
A25	PEX_RX2_P	PEX2_RX+	PCIe Ctlr 0 Lane 2 Receive +	Input	B25	GND	–	Ground	Ground
A26	PEX_RX2_N	PEX2_RX–	PCIe Ctlr 0 Lane 2 Receive –	Input	B26	GND			
A27	GND	–	Ground	Ground	B27	PEX_TX1_C_P	PEX_RFU_TX+	PCIe Ctlr 0 Lane 3 Transmit +	Output
A28	GND				B28	PEX_TX1_C_N	PEX_RFU_TX–	PCIe Ctlr 0 Lane 3 Transmit –	Output
A29	PEX_RX1_P	PEX_RFU_RX+	PCIe Ctlr 0 Lane 3 Receive +	Input	B29	GND	–	Ground	Ground
A30	PEX_RX1_N	PEX_RFU_RX–	PCIe Ctlr 0 Lane 3 Receive –	Input	B30	NC	–	Unused	Unused
A31	GND	–	Ground	Ground	B31	NC			
A32	NC	–	Unused	Unused	B32	GND	–	Ground	Ground

Legend

Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to the PCIe Connector. Input is from the PCIe Connector. Bidir is for Bidirectional signals.

Table 9. PCIe x4 Related TX1 Carrier PCB Trace Delays

Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for PCI Board (ps)		Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for PCI Board (ps)
PCIe					PEX2_RX+	540	880	340
PEX0_RX+	502	880	378		PEX2_RX–	539	880	341
PEX0_RX–	502	880	378		PEX2_TX+	521	880	359
PEX0_TX+	505	880	375		PEX2_TX–	522	880	358
PEX0_TX–	504	880	376		PEX_RFU_RX+	539	880	341
USB_SS1_RX+	528	880	352		PEX_RFU_RX–	539	880	342
USB_SS1_RX–	527	880	353		PEX_RFU_TX+	518	880	362
USB_SS1_TX+	522	880	358		PEX_RFU_TX–	519	880	361
USB_SS1_TX–	522	880	358		PEX0_REFCLK+	521	880	359
					PEX0_REFCLK–	520	880	360

2.8 JTAG

The Jetson carrier board has a standard 20-pin (2x10, 2.54mm pitch) JTAG header (J7).

Figure 10. JTAG Header Connections

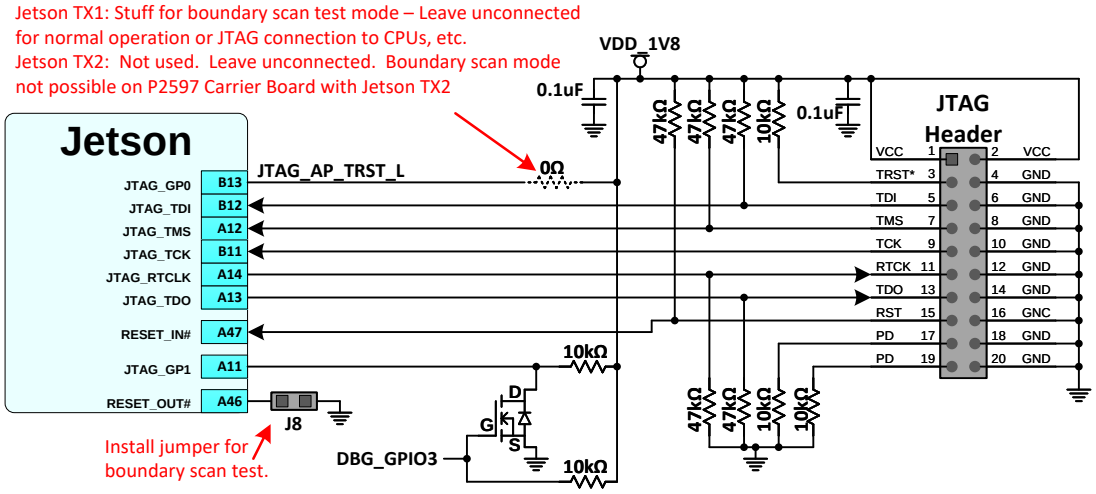


Table 10. JTAG Header Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	VDD_1V8	–	Main 1.8V Supply	Power	2	VDD_1V8	–	Main 1.8V Supply	Power
3	TRST*	–	JTAG Test Reset	Output	4	GND	–	Ground	Ground
5	JTAG_AP_TDI	JTAG_TDI	JTAG Test Data In	Input	6	GND			
7	JTAG_AP_TMS	JTAG_TMS	JTAG Test Mode Select	Input	8	GND			
9	JTAG_AP_TCK	JTAG_TCK	JTAG Test Clock	Input	10	GND			
11	JTAG_AP_RTCK	JTAG_RTCK	JTAG Test Return Clock	Output	12	GND			
13	JTAG_AP_TDO	JTAG_TDO	JTAG Test Data Out	Output	14	GND			
15	RESET_IN_L	RESET_IN#	Main carrier board reset	Input	16	GND			
17	PD	–	Pull-down	–	18	GND			
19	PD	–	Pull-down	–	20	GND			

Legend

Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to JTAG header. Input is from JTAG header. Bidir is for Bidirectional signals.

3.0 CARRIER BOARD CUSTOM EXPANSION CONNECTIONS

The Jetson carrier board supports several custom expansion headers:

- Jetson Module Connector, 8x50, 1.27mm pitch
- Display Expansion Header, 2x60, 0.5mm pitch
- Camera Expansion Header, 2x60, 0.5mm pitch
- Expansion Header, 2x20, 2.54mm pitch
- Serial Port Header, 1x6, 2.54mm pitch
- Debug Connector, 2x30, 0.5mm pitch
- GPIO Expansion Header, 2x15, 2.54mm pitch
- Charge Control Connector, 10-pin Flex Receptacle, 0.8mm pitch
- Fan Header, 4-pin, 1.25mm pitch
- DC Power Jack

The Routing Guidelines for the interfaces supported on the expansion connectors can be found in the Jetson TX1 or Jetson TX2 OEM Product Design Guide (OEM DG). Those guidelines cover the PCB routing from the Jetson module to the peripheral device or actual device connector. When designing modules for one of the Jetson module expansion connectors, the routing on the carrier board must be accounted for. Tables are provided for the critical interfaces that provide the PCB delays on the carrier board. These delays are subtracted from the delays allowed in the OEM DG routing guidelines. The tables also include the max trace guidelines and remaining max trace delay allowed on the peripheral modules. See the OEM DG for other requirements (Impedance, trace spacing, skews between signals, etc.).

3.1 Module Connector

The carrier board interfaces to the Jetson TX1 or Jetson TX2 using a 400-pin (8 x 50) connector (J13). The part number for the connector used on the carrier board can be found in the Jetson TX1 or Jetson TX2 Supported Component List (SCL) document. This interfaces with the module which has a Samtec REF-186137-01 connector. The connector pinout can be found in the OEM DG.

3.2 Display Expansion Connector

The Jetson carrier board includes a 120-pin (2x60, 0.5mm pitch) Display Expansion Connector (J23). The connector used on the carrier board is a Samtec QSH-060-01-H-D-A. The mating connector is a Samtec QTH-060-01-H-D-A. This expansion connector includes interface options for an embedded display and touch controller including:

- DSI 2 x4
- eDP
- eDP HPD
- eDP AUX
- LCD BL EN/PWM
- LCD EN/TE/BIAS EN
- SPI0, SPI2
- I2C_GP1
- Touch INT/RST/CLK
- Display control

Table 11. Display Expansion Connector Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	CON_DSI_B_D3_N	DSI3_D1–	DSI B Data 3-	Output	2	VDD_SYS_BL	–	Backlight power from Main DC supply	Power
3	CON_DSI_B_D3_P	DSI3_D1+	DSI B Data 3+	Output	4	VDD_SYS_BL			
5	GND	–	Ground	Ground	6	VDD_SYS_BL			
7	CON_DSI_B_D2_N	DSI3_D0–	DSI B Data 2-	Output	8	LCD_BL_EN	LCD_BKLT_EN	Backlight Enable	Output
9	CON_DSI_B_D2_P	DSI3_D0+	DSI B Data 2+	Output	10	LCD_BL_PWM	LCD_BKLT0_PWM	Backlight PWM	Output
11	GND	–	Ground	Ground	12	LCD_RST_L	LCD_EN	LCD Enable	Output
13	CON_DSI_B_CLK_N	DSI3_CLK–	DSI B Clock-	Output	14	LCD_TE	LCD_TE	LCD Tearing Effect	Input

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
15	CON_DSI_B_CLK_P	DSI3_CLK+	DSI B Clock+	Output	16	VDD_3V3_SLP	–	3.3V supply - off in Deep Slp	Power
17	GND	–	Ground	Ground	18	BRIDGE_EN	–	Bridge Enable	Output
19	CON_DSI_B_D1_N	DSI2_D1–	DSI B Data 1-	Output	20	BRIDGE_IRQ	–	Bridge Interrupt	Output
21	CON_DSI_B_D1_P	DSI2_D1+	DSI B Data 1+	Output	22	I2C_GP0_CLK_1V8	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD
23	GND	–	Ground	Ground	24	I2C_GP0_DAT_1V8	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD
25	CON_DSI_B_D0_N	DSI2_D0–	DSI B Data 0-	Output	26	AVDD_TS_DIS	–	3.3V supply for touchscreen	Power
27	CON_DSI_B_D0_P	DSI2_D0+	DSI B Data 0+	Output	28	VDD_TS_1V8		1.8V supply for touchscreen	
29	GND	–	Ground	Ground	30	CON_GEN2_I2C_SCL_LT	I2C_GP1_CLK	General I2C #1 Clock	Bidir/OD
31	CON_DSI_A_D3_N	DSI1_D1–	DSI A Data 3-	Output	32	CON_GEN2_I2C_SDA_LT	I2C_GP1_DAT	General I2C #1 Data	Bidir/OD
33	CON_DSI_A_D3_P	DSI1_D1+	DSI A Data 3+	Output	34	TOUCH_INT	GPIO6_TOUCH_INT	Touchscreen Interrupt	Input
35	GND	–	Ground	Ground	36	TOUCH_RST	GPIO7_TOUCH_RST	Touchscreen controller Reset	Output
37	CON_DSI_A_D2_N	DSI1_D0–	DSI A Data 2-	Output	38	SPI0_CLK	SPI0_CLK	Touchscreen SPI Clock	Bidir
39	CON_DSI_A_D2_P	DSI1_D0+	DSI A Data 2+	Output	40	SPI0_MISO	SPI0_MISO	Touchscreen SPI MISO	Bidir
41	GND	–	Ground	Ground	42	SPI0_MOSI	SPI0_MOSI	Touchscreen SPI MOSI	Bidir
43	CON_DSI_A_CLK_N	DSI0_CLK–	DSI A Clock-	Output	44	SPI0_CS0	SPI0_CS0#	Touchscreen SPI Chip Select	Bidir
45	CON_DSI_A_CLK_P	DSI0_CLK+	DSI A Clock+	Output	46	NC	–	Unused	Unused
47	GND	–	Ground	Ground	48	GND	–	Ground	Ground
49	CON_DSI_A_D1_N	DSI0_D1–	DSI A Data 1-	Output	50	TOUCH_CLK	TOUCH_CLK	Touchscreen Controller Clock	Output
51	CON_DSI_A_D1_P	DSI0_D1+	DSI A Data 1+	Output	52	GND	–		Ground
53	GND	–	Ground	Ground	54	VDD_DIS_3V3_LCD	–	Gated 3.3V analog supply	Power
55	CON_DSI_A_D0_N	DSI0_D0–	DSI A Data 0-	Output	56	VDD_DIS_3V3_LCD	–		Power
57	CON_DSI_A_D0_P	DSI0_D0+	DSI A Data 0+	Output	58	VDD_LCD_1V8_DIS		Gated 1.8V supply	
59	GND	–	Ground	Ground	60	GND	–	Ground	Ground
61	VDD_3V3_SYS	–	Main 3.3V Supply (Switcher)	Power	62	LCD_EN	LCD_VDD_EN	LCD Power Enable	Output
63	VDD_3V3_SYS				64	NC	–	Unused	Unused
65	GND	–	Ground	Ground	66	CON_DSI3_CLK_P	DSI3_CLK+	Display DSI 3 Clock+	Output
67	GND				68	CON_DSI3_CLK_N	DSI3_CLK-	Display DSI 3 Clock-	Output
69	VDD_1V8	–	Main 1.8V Supply (Switcher)	Power	70	GND	–	Ground	Ground
71	VDD_1V8				72	CON_DSI4_CLK_P	DSI4_CLK+	Display DSI 4 Clock+	Output
73	GND	–	Ground	Ground	74	CON_DSI4_CLK_N	DSI4_CLK-	Display DSI 4 Clock-	Output
75	GND				76	GND	–	Ground	Ground
77	VDD_1V2	–	1.2V Display Supply (LDO)	Power	78	GND			
79	VDD_1V2				80	VDD_5V0_IO_SYS	–	Main 5.0V Supply (Switcher)	Power
81	GND	–	Ground	Ground	82	NC	–	Unused	Unused
83	GND				84	NC			
85	DP_HPD0_AP	DP_HPD	Display Port 0 Hot Plug Det.	Input	86	ACOK	CHARGER_PRSNT	AC OK	Output
87	EDP_AUX_CH0_N	DP0_AUX_CH–	Display Port 0 Aux Channel-	Bidir	88	LCD_BIAS_EN	–	LCD BIAS Enable	Output
89	EDP_AUX_CH0_P	DP0_AUX_CH+	Display Port 0 Aux Channel+	Bidir	90	GND	–	Ground	Ground
91	GND	–	Ground	Ground	92	GS_V	GSYNC_VSYNC	GSYNC Vsync	Output
93	EDP_TXD0_P	DP0_TX0+	Display Port 0 Data Lane 0-	Output	94	GS_H	GSYNC_HSYNC	GSYNC Hsync	Output
95	EDP_TXD0_N	DP0_TX0–	Display Port Data Lane 0+	Output	96	GND	–	Ground	Ground
97	GND	–	Ground	Ground	98	NVSR_INT	–	NV Sensor Interrupt	Input
99	EDP_TXD1_P	DP0_TX1+	Display Port 0 Data Lane 1-	Output	100	LCD1_BKLT_PWM	LCD_BKLT1_PWM	Backlight PWM	Output
101	EDP_TXD1_N	DP0_TX1–	Display Port 0 Data Lane 1+	Output	102	GND	–	Ground	Ground
103	GND	–	Ground	Ground	104	SPI2_SCK	SPI2_SCK	SPI #2 Clock	Bidir
105	EDP_TXD2_P	DP0_TX2+	Display Port 0 Data Lane 2-	Output	106	SPI2_MISO	SPI2_MISO	SPI #2 Master In, Slave Out	Bidir
107	EDP_TXD2_N	DP0_TX2–	Display Port 0 Data Lane 2+	Output	108	SPI2_MOSI	SPI2_MOSI	SPI #2 Master Out, Slave In	Bidir
109	GND	–	Ground	Ground	110	SPI2_CS0	SPI2_CS0#	SPI #2 Chip Select	Bidir
111	NC	–	Unused	Unused	112	GND	–	Ground	Ground
113	NC				114	NC	–	Unused	Unused
115	GND	–	Ground	Ground	116	NC			
117	EDP_TXD3_P	DP0_TX3+	Display Port 0 Data Lane 3-	Output	118	NC			
119	EDP_TXD3_N	DP0_TX3–	Display Port 0 Data Lane 3+	Output	120	NC			

Legend

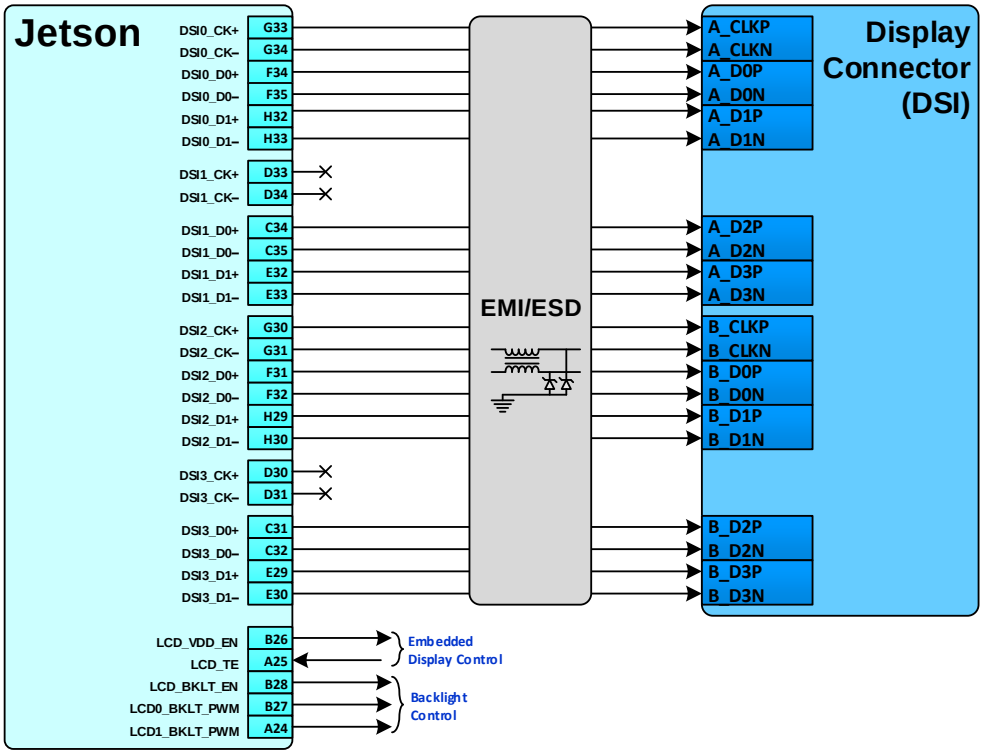
Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to Display Module. Input is from Display Module. Bidir is for Bidirectional signals.

DSI

Tegra supports eight total MIPI DSI data lanes and two clock lanes, allowing up to two 4-lane interfaces. These can be used for two separate displays, or together for a single display (clock lane per 4 data lanes still applies for the single display case. Each data lane has peak bandwidth up to 1.5Gbps.

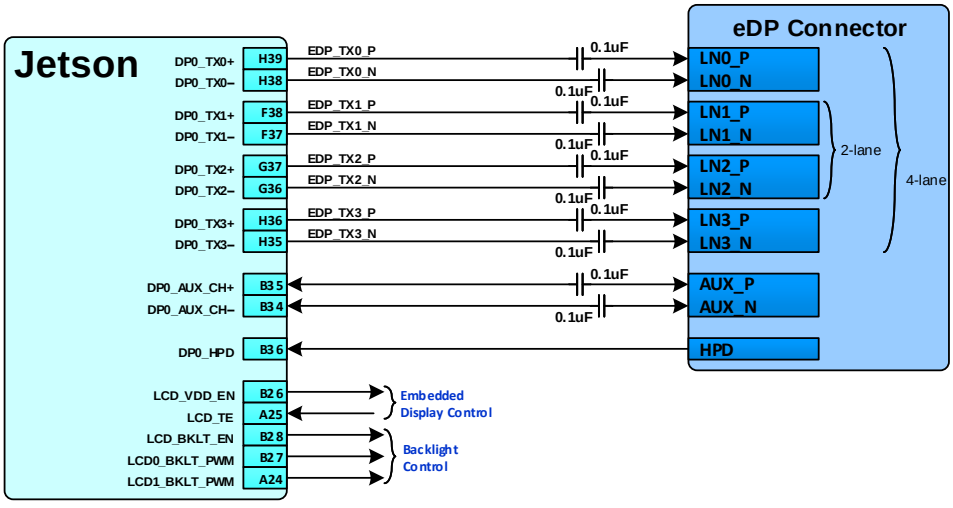
Figure 11: DSI 2 x 4-Lane Connection Example



Note: If EMI/ESD devices are necessary, they must be tuned to minimize impact to signal quality, which must meet the DSI spec. requirements for the frequencies supported by the design.

eDP

Figure 12: eDP 4-Lane Connection Example



DSI & DP/eDP Guidelines

See the Jetson TX1 or Jetson TX2 OEM Product DG for Routing Guidelines. Include the carrier board PCB trace delays in the following tables when calculating max trace length & for skew matching.

Table 12. Display Connector Interface Related TX1 Carrier PCB Trace Delays (DSI & SPI)

Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Display Module (ps)		Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Display Module (ps)
DSI					DSI2_D1+	493	1100	607
DSI0_CK+	494	1100	606		DSI2_D1–	492	1100	608
DSI0_CK–	493	1100	607		DSI3_D0+	496	1100	604
DSI0_D0+	495	1100	605		DSI3_D0–	496	1100	604
DSI0_D0–	496	1100	604		DSI3_D1+	495	1100	605
DSI0_D1+	490	1100	610		DSI3_D1–	496	1100	604
DSI0_D1–	489	1100	611		**SPI**			
DSI1_D0+	492	1100	608		SPI0_CLK	750	1760	1010
DSI1_D0–	493	1100	607		SPI0_MISO	740	1760	1020
DSI1_D1+	495	1100	605		SPI0_MOSI	743	1760	1017
DSI1_D1–	496	1100	604		SPI0_CS0#	758	1760	1002
DSI2_CK+	493	1100	607		SPI2_SCK	658	1760	1101
DSI2_CK–	492	1100	608		SPI2_MISO	650	1760	1110
DSI2_D0+	491	1100	609		SPI2_MOSI	649	1760	1111
DSI2_D0–	491	1100	609		SPI2_CS0#	643	1760	1117

Notes: Max Trace Delay Allowed for SPI assumes a single load case. If two loads are implemented, See the Jetson TX1 or Jetson TX2 OEM Product Design Guide for details.

Table 13. Display Connector Interface Related TX1 Carrier PCB Trace Delays (DP0)

Jetson Module Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)		Max Delay for Display Module (ps)	
		RBR/HBR Stripline	RBR/HBR uStrip	RBR/HBR Stripline	RBR/HBR uStrip
DP0_TX0+	609	1138	975	529	366
DP0_TX0–	608	1138	975	529	367
DP0_TX1+	608	1138	975	529	367
DP0_TX1–	609	1138	975	529	366
DP0_TX2+	623	1138	975	514	352
DP0_TX2–	624	1138	975	513	351
DP0_TX3+	658	1138	975	479	317
DP0_TX3–	659	1138	975	478	316
DP0_AUX_CH+	529	1138	975	608	446
DP0_AUX_CH–	529	1138	975	609	446

3.3 Camera Expansion Header

The Jetson carrier board includes a 120-pin (2x60, 0.5mm pitch) Camera Expansion Connector (J22). The connector used on the carrier board is a Samtec QSH-060-01-H-D-A. The mating connector is a Samtec QTH-060-01-H-D-A. The expansion connector includes interface options for multiple cameras as well as some for audio (I2S & DMIC):

- CSI up to 6x2 lane
- CAM_I2C, Clock & Control GPIOs for the Cameras
- Digital Microphone IF
- I2S
- SPI
- I2C
- UART

Table 14. Camera Expansion Connector Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	CON_CSI_A_D0_P	CSI0_D0+	CSI A Data 0+	Input	2	CON_CSI_B_D0_P	CSI1_D0_P	CSI B Data 0+	Input
3	CON_CSI_A_D0_N	CSI0_D0–	CSI A Data 0-	Input	4	CON_CSI_B_D0_N	CSI1_D0_N	CSI B Data 0-	Input
5	GND	–	Ground	Ground	6	GND	–	Ground	Ground
7	CON_CSI_A_CLK_P	CSI0_CLK+	CSI A Clock+	Input	8	CON_CSI_B_CLK_P	CSI1_CLK_P	CSI B Clock+	Input
9	CON_CSI_A_CLK_N	CSI0_CLK–	CSI A Clock-	Input	10	CON_CSI_B_CLK_N	CSI1_CLK_N	CSI B Clock-	Input
11	GND	–	Ground	Ground	12	GND	–	Ground	Ground
13	CON_CSI_A_D1_P	CSI0_D1+	CSI A Data 1+	Input	14	CON_CSI_B_D1_P	CSI1_D1_P	CSI B Data 1+	Input
15	CON_CSI_A_D1_N	CSI0_D1–	CSI A Data 1-	Input	16	CON_CSI_B_D1_N	CSI1_D1–	CSI B Data 1-	Input
17	GND	–	Ground	Ground	18	GND	–	Ground	Ground
19	CON_CSI_C_D0_P	CSI2_D0+	CSI C Data 0+	Input	20	CON_CSI_D_D0_P	CSI3_D0+	CSI D Data 0+	Input
21	CON_CSI_C_D0_N	CSI2_D0–	CSI C Data 0-	Input	22	CON_CSI_D_D0_N	CSI3_D0–	CSI D Data 0-	Input
23	GND	–	Ground	Ground	24	GND	–	Ground	Ground
25	CON_CSI_C_CLK_P	CSI2_CLK+	CSI C Clock+	Input	26	CON_CSI_D_CLK_P	CSI3_CLK+	CSI D Clock+	Input
27	CON_CSI_C_CLK_N	CSI2_CLK–	CSI C Clock-	Input	28	CON_CSI_D_CLK_N	CSI3_CLK–	CSI D Clock-	Input
29	GND	–	Ground	Ground	30	GND	–	Ground	Ground
31	CON_CSI_C_D1_P	CSI2_D1+	CSI C Data 1+	Input	32	CON_CSI_D_D1_P	CSI3_D1+	CSI D Data 1+	Input
33	CON_CSI_C_D1_N	CSI2_D1–	CSI C Data 1-	Input	34	CON_CSI_D_D1_N	CSI3_D1–	CSI D Data 1-	Input
35	GND	–	Ground	Ground	36	GND	–	Ground	Ground
37	CON_CSI_E_D0_P	CSI4_D0+	CSI E Data 0+	Input	38	CON_CSI_F_D0_P	CSI5_D0+	CSI F Data 0+	Input
39	CON_CSI_E_D0_N	CSI4_D0–	CSI E Data 0-	Input	40	CON_CSI_F_D0_N	CSI5_D0–	CSI F Data 0-	Input
41	GND	–	Ground	Ground	42	GND	–	Ground	Ground
43	CON_CSI_E_CLK_P	CSI4_CLK+	CSI E Clock+	Input	44	CON_CSI_F_CLK_P	CSI5_CLK+	CSI F Clock+	Input
45	CON_CSI_E_CLK_N	CSI4_CLK–	CSI E Clock-	Input	46	CON_CSI_F_CLK_N	CSI5_CLK–	CSI F Clock-	Input
47	GND	–	Ground	Ground	48	GND	–	Ground	Ground
49	CON_CSI_E_D1_P	CSI4_D1+	CSI E Data 1+	Input	50	CON_CSI_F_D1_P	CSI5_D1+	CSI F Data 1+	Input
51	CON_CSI_E_D1_N	CSI4_D1–	CSI E Data 1-	Input	52	CON_CSI_F_D1_N	CSI5_D1–	CSI F Data 1-	Input
53	GND	–	Ground	Ground	54	GND	–	Ground	Ground
55	RSVD	–	Unused	Unused	56	RSVD	–	Unused	Unused
57	RSVD				58	RSVD			
59	CAM_UART3_PSNT_L	–	Camera UART Present – Direction control for level shifter to prevent contention.	–	60	NC			
61	CAM_UART3_TXD	–	Camera UART Transmit, Receive, Clear-to-Send & Request to Send – Can optionally be brought to Serial port connector (J13).	Output	62	SPI2_SCK	SPI2_CLK	SPI #2 Clock	Bidir
63	CAM_UART3_RXD	–		Input	64	SPI2_MISO	SPI2_MISO	SPI #2 MISO	Bidir
65	CAM_UART3_CTS	–		Input	66	SPI2_CS1	SPI2_CS1#	SPI #2 Chip Select	Bidir
67	CAM_UART3_RTS	–		Output	68	SPI2_MOSI	SPI2_MOSI	SPI #2 MOSI	Bidir
69	GND	–	Ground	Ground	70	GND	–	Ground	Ground
71	AO_DMIC_IN_CLK	CAN_GPIO1	Digital Mic Input Clock	Output	72	I2S3_CLK	I2S3_CLK	I2S #3 Clock	Bidir
73	AO_DMIC_IN_DAT	CAN_GPIO0	Digital Mic Input Data	Input	74	I2S3_LRCLK	I2S3_LRCLK	I2S #3 Left/Right Clock	Bidir
75	CAM_I2C_SCL	I2C_CAM_CLK	Camera I2C clock	Bidir	76	I2S3_SDIN	I2S3_SDIN	I2S #3 Serial Data In	Input
77	CAM_I2C_SDA	I2C_CAM_DAT	Camera I2C data	Bidir	78	I2S3_SDOUT	I2S3_SDOUT	I2S #3 Serial Data Out	Bidir
79	GND	–	Ground	Ground	80	GND	–	Ground	Ground
81	AVDD_CAM	–	2.8V Camera supply (LDO)	Power	82	AVDD_CAM	–	2.8V Camera supply (LDO)	Power
83	AVDD_CAM				84	VDD_3V3_SLP	–	3.3V rail - off in Deep Sleep	Power
85	CAM_AF_PWDN	–	Camera auto-focus powerdn	Output	86	CAM_VSYNC	CAM_VSYNC	Camera Vertical Sync	Output
87	I2C_PM_CLK	I2C_PM_CLK	Power Monitor I2C Clock	Bidir/OD	88	CAM1_MCLK	CAM1_MCLK	Camera #1 Master Clock	Output
89	I2C_PM_DAT	I2C_PM_DAT	Power Monitor I2C Data	Bidir/OD	90	CAM1_PWDN	GPIO1_CAM1_PWR	Camera #1 Powerdown	Output
91	CAM0_MCLK	CAM0_MCLK	Camera #0 Master Clock	Output	92	CAM1_RST_L	GPIO3_CAM1_RST	Camera #1 Reset	Output
93	CAM0_PWDN	GPIO0_CAM0_PWR	Camera #0 Powerdown	Output	94	CAM2_MCLK	CAM2_MCLK	Camera #2 Master Clock	Output
95	CAM0_RST_L	GPIO2_CAM0_RST	Camera #0 Reset	Output	96	CAM2_PWDN	–	Camera #2 Powerdown	Output
97	FLASH_EN	GPIO5_CAM_ FLASH_EN	Flash Enable	Output	98	CAM2_RST	–	Camera #2 Reset	Output
99	GND	–	Ground	Ground	100	GND	–	Ground	Ground
101	DVDD_CAM_IO_1V2	–	1.2V digital Camera supply	Power	102	DVDD_CAM_IO_1V8	–	Switched 1.8V Camera supply.	Power
103	FLASH_INHIBIT	–	Flash Inhibit	Output	104	TORCH_EN	–	Torch Enable (GPIO exp. P05)	Output
105	I2C_GP0_CLK_1V8	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD	106	FLASH_STROBE	GPIO4_CAM_STROBE	Flash Strobe	Output
107	I2C_GP0_DAT_1V8	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD	108	VDD_3V3_SLP	–	3.3V supply – off in Deep Slp	Power
109	VDD_5V0_IO_SYS	–	Main 5.0V Supply (Switcher)	Power	110	VDD_3V3_SLP	–	3.3V supply – off in Deep Slp	Power

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
111	NC	–	Unused	Unused	112	MOTION_INT_AP_L	GPIO9_MOTION_INT	Motion Sensor Interrupt	Input
113	NC				114	NC	–	Unused	Unused
115	GND	–	Ground	Ground	116	GND	–	Ground	Ground
117	MDM2AP_READY_1V8	GPIO17_MDM2AP_READY	Modem to Tegra Ready	Input	118	VDD_5V0_IO_SYS	–	Main 5.0V Supply (Switcher)	Power
119	VDD_SYS_EN	–	System power enable	Output	120	VDD_5V0_IO_SYS			

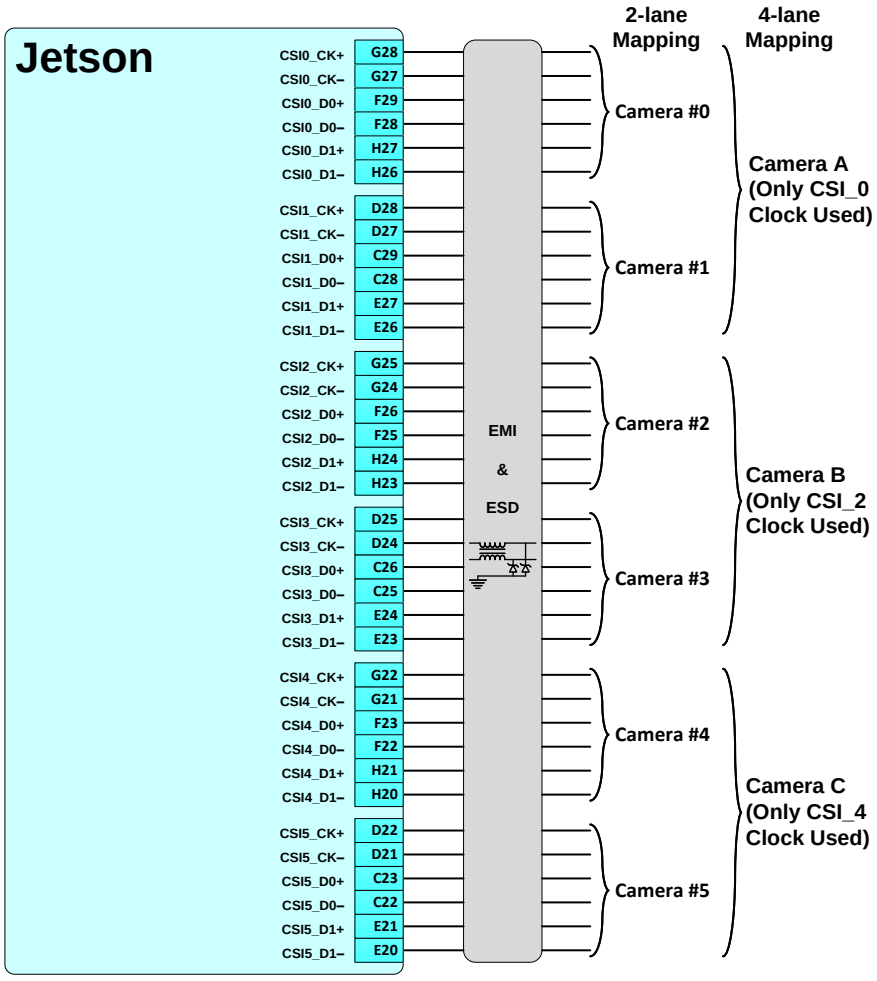
Legend

Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to Camera Module. Input is from Camera Module. Bidir is for Bidirectional signals.

Camera/CSI Guidelines

Figure 13: Camera CSI Connections



Note: Any EMI/ESD devices must be tuned to minimize impact to signal quality and meet the timing & Vil/Vih requirements at the receiver & maintain signal quality and meet requirements for the frequencies supported by the design.

See the Jetson TX1 or Jetson TX2 OEM Product DG for Routing Guidelines. Include the carrier board PCB trace delays in the following table when calculating max trace length & for skew matching.

Table 15. Camera Expansion Connector Related TX1 Carrier PCB Trace Delays

Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Camera Module (ps)		Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Camera Module (ps)
CSI					CSI4_CK+	540	1100	560
CSI0_CK+	626	1100	474		CSI4_CK–	539	1100	561
CSI0_CK–	626	1100	474		CSI4_D0+	540	1100	560
CSI0_D0+	627	1100	473		CSI4_D0–	540	1100	560
CSI0_D0–	627	1100	473		CSI4_D1+	541	1100	559
CSI0_D1+	627	1100	473		CSI4_D1–	540	1100	560
CSI0_D1–	626	1100	474		CSI5_CK+	540	1100	560
CSI1_CK+	626	1100	474		CSI5_CK–	539	1100	561
CSI1_CK–	625	1100	475		CSI5_D0+	541	1100	559
CSI1_D0+	627	1100	473		CSI5_D0–	540	1100	560
CSI1_D0–	626	1100	474		CSI5_D1+	541	1100	559
CSI1_D1+	627	1100	473		CSI5_D1–	540	1100	560
CSI1_D1–	626	1100	474		**I2S**			
CSI2_CK+	587	1100	513		I2S3_CLK	472	3600	3128
CSI2_CK–	586	1100	514		I2S3_LRCLK	485	3600	3115
CSI2_D0+	586	1100	514		I2S3_SDIN	497	3600	3103
CSI2_D0–	585	1100	515		I2S3_SDOUT	457	3600	3143
CSI2_D1+	588	1100	512		**SPI**			
CSI2_D1–	587	1100	513		SPI2_SCK	658	1760	1102
CSI3_CK+	587	1100	513		SPI2_MISO	650	1760	1110
CSI3_CK–	586	1100	514		SPI2_CS1#	513	1760	1247
CSI3_D0+	588	1100	512		SPI2_MOSI	649	1760	1111
CSI3_D0–	587	1100	513					
CSI3_D1+	588	1100	512					
CSI3_D1–	587	1100	513					

Notes: Max Trace Delay Allowed for SPI assumes a single load case. If two loads are implemented, See the Jetson TX1 OEM Product Design Guide for details.

3.4 Expansion Header

The Jetson carrier board includes a 40-pin (2x20, 2.54mm pitch) Expansion Header (J21). The connector used on the carrier board is a Samtec TSM-120-01-S-DV-TR. The expansion connector includes various audio & control interfaces including:

- I2S(See Note)
- Audio Clock/Control
- Digital Microphone IF
- I2C (x2) (See Note)
- SPI (See Note)
- UART (See Note)

Note: Some of these interfaces can be 1.8V or 3.3V. J24 is a 3-pin header that is used to control the voltage of the level shifter these interfaces pass through. If J24 pin 1-2 are shorted, the interfaces are level shifted to 3.3V. If pins 2-3 are shorted, the interfaces are 1.8V. The 3.3V only interfaces/signals are:

- I2C_GP0_x_3V3_LVL
- I2C_GP1_x_3V3
- UART1_x_HDR_3V3
- GPIO_EXP_P[17:16]_3V3
- MOTION_INT_AP_L_LVL
- SAR_TOUT_LVL

Table 16. Expansion Header Pin Descriptions

Pin #	Signal Name	Associated Jetson Module Pin Name	Usage/Description	Type/ Direction	Signal Voltage Level at Header	GPIO Max Drive (I_{OL}/I_{OH}) or Power Pin Current Capability	Notes
1	VDD_3V3_SYS	–	Main 3.3V Supply	Power	–	1A	1
2	VDD_5V0_IO_SYS	–	Main 5.0V Supply	Power	–	1A	1
3	I2C_GP0_SDA_3V3_LVL	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD	3.3V	1mA / -1mA	2
4	VDD_5V0_IO_SYS		Main 5.0V Supply	Power	–	1A	1
5	I2C_GP0_SCL_3V3_LVL	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD	3.3V	1mA / -1mA	2
6	GND	–	Ground	Ground	–	–	–
7	AUDIO_I2S_MCLK_3V3	AUDIO_MCLK	Audio Master Clock	Bidir	1.8/3.3V	20uA / -20uA	3
8	UART1_TXD_HDR_3V3	UART0_TX	UART #0 Transmit	Output	3.3V	24mA / -24mA	4
9	GND	–	Ground	Ground	–	–	–
10	UART1_RXD_HDR_3V3	UART0_RX	UART #0 Receive	Input	3.3V	–	4
11	UART1_RTS_HDR_3V3	UART0_RTS#	UART #0 Request to Send	Output	3.3V	24mA / -24mA	4
12	AUDIO_I2S_SRCLK_3V3	I2S0_SCLK	Audio I2S #0 Clock	Bidir	1.8/3.3V	20uA / -20uA	3
13	AUDIO_CDC_IRQ_LVL	GPIO20_AUD_INT	Audio Codec Interrupt	Bidir	1.8/3.3V	20uA / -20uA	3
14	GND	–	Ground	Ground	–	–	–
15	GPIO_EXP_P17_3V3	–	From GPIO Expander (P17)	Bidir	3.3V	25mA / -10mA	5
16	AO_DMIC_IN_DAT_LVL	AO_DMIC_IN_DAT	Digital Mic Input	Input	1.8/3.3V	20uA / -20uA	3, 8
17	VDD_3V3_SYS	–	Main 3.3V Supply	Power	–	1A	1
18	MDM_WAKE_AP_LVL	GPIO16_MDM_WAKE_AP	Modem Wake AP GPIO	Input	1.8/3.3V	20uA / -20uA	3, 8
19	SPI1_MOSI_3V3	SPI1_MOSI	SPI #1 Master Out/Slave In	Bidir	1.8/3.3V	20uA / -20uA	3
20	GND	–	Ground	Ground	–	–	–
21	SPI1_MISO_3V3	SPI1_MISO	SPI #1 Master In/Slave Out	Bidir	1.8/3.3V	20uA / -20uA	3
22	GPIO_EXP_P16_3V3	–	From GPIO Expander (P16)	Bidir	3.3V	25mA / -10mA	5
23	SPI1_SCK_3V3	SPI1_CLK	SPI #1 Shift Clock	Bidir	1.8/3.3V	20uA / -20uA	3
24	SPI1_CS0_3V3	SPI1_CS0#	SPI #1 Chip Select #0	Bidir	1.8/3.3V	20uA / -20uA	3
25	GND	–	Ground	Ground	–	–	–
26	SPI1_CS1_3V3	SPI1_CS1#	SPI #1 Chip Select #1	Bidir	1.8/3.3V	20uA / -20uA	3
27	I2C_GP1_DAT_3V3	I2C_GP1_DAT	General I2C #1 Data	Bidir/OD	3.3V	1mA / -1mA	6
28	I2C_GP1_CLK_3V3	I2C_GP1_CLK	General I2C #1 Clock	Bidir/OD	3.3V	1mA / -1mA	6
29	AUD_RST_LVL	GPIO19_AUD_RST	Audio Reset	Output	1.8/3.3V	20uA / -20uA	3, 8
30	GND	–	Ground	Ground	–	–	–
31	MOTION_INT_AP_L_LVL	GPIO9_MOTION_INT	Motion Interrupt	Input/OD	3.3V	1mA / -1mA	2, 8
32	AO_DMIC_IN_CLK_LVL	AO_DMIC_IN_CLK	Digital Mic Clock	Output	1.8/3.3V	20uA / -20uA	3, 8
33	AP_WAKE_BT_3V3	GPIO11_AP_WAKE_BT	AP Wake Bt GPIO	Bidir	1.8/3.3V	20uA / -20uA	3, 8
34	GND	–	Ground	Ground	–	–	–
35	AUDIO_I2S_SFSYNC_3V3	I2S0_LRCLK	AUDIO I2S #0 Left/Right Clock	Bidir	1.8/3.3V	20uA / -20uA	3
36	UART1_CTS_HDR_3V3	UART0_CTS#	UART #0 Clear to Send	Input	3.3V	–	4
37	SAR_TOUT_LVL	GPIO8_ALS_PROX_INT	Accelerometer/Proximity Interrupt	Output/OD	3.3V	1mA / -1mA	2, 8
38	AUDIO_I2S_SIN_3V3	I2S0_SDIN	Audio I2S #0 Data in	Input	1.8/3.3V	20uA / -20uA	3, 8
39	GND	–	Ground	Ground	–	–	–
40	AUDIO_I2S_SOUT_3V3	I2S0_SDOUT	Audio I2S #0 Data Out	Output	1.8/3.3V	20uA / -20uA	3, 8

Legend

Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes:

1. This is current capability per power pin.
2. These pins are connected to Tegra through either an I2C (PCA9306) or FET (FDV301N) level shifter. They are open-drain (either pulled up, or driven low by Tegra when configured as outputs). The max drive that meets the Data Sheet V_{OL} is 1mA. 2mA drive is supported at restricted V_{OL} levels. See associated OEM Product Design Guide Pads section for details.
3. These pins connect to TI TXB0108 level translators. The voltage level at the header pins can be selected by J24 to be 1.8V (2-3) or 3.3V (1-2). Due to the design of these devices, the output drivers are very weak so they can be overdriven by another connected device output for bidirectional support.
4. These pins connect to a SN74LVC2T45 buffer, which is powered at 3.3V on the Expansion Header side.
5. These signals come from the TCA9539 GPIO expanders.
6. These pins are directly connected to Tegra. The max drive that meets full Data Sheet V_{OL}/V_{OH} is 1mA. 2mA drive is supported at restricted V_{OL}/V_{OH} levels. See the associated OEM Product Design Guide Pads section for details.
7. In the Type/Dir column, Output is to Expansion Module. Input is from Expansion Module. Bidir is for Bidirectional signals.

8. The direction indicated matches that indicated in the reference design schematics. These signals can be bidirectional.

Table 17. Jetson TX1 Expansion Header Signal Details

Pin #	Signal Name	Tegra Ball Name	Tegra GPIO Port.#	Power-on Default State	Pin State after Pinmux Config.	External PU/PD on module	External PU/PD on carrier board	Pinmux SFIO Functions Supported	Notes
3	I2C_GP0_SDA_3V3_LVL	GEN1_I2C_SDA	–	Z	Z	1kΩ to 1.8V	–	I2C1_DAT	
5	I2C_GP0_SCL_3V3_LVL	GEN1_I2C_SCL	–	Z	Z	1kΩ to 1.8V	–	I2C1_CLK	
7	AUDIO_I2S_MCLK_3V3	AUD_MCLK	BB.03	PD	PU	–	1MΩ to GND	AUD_MCLK	
8	UART1_TXD_HDR_3V3	UART1_TX	U.00	PD	PD	–	PU or PD	UA3_TXD	3
10	UART1_RXD_HDR_3V3	UART1_RX	U.01	PD	PU	–	100kΩ to 3.3V	UA3_RXD	
11	UART1_RTS_HDR_3V3	UART1_RTS_N	U.02	PD	PD	–	PU or PD	UA3_RTS	3
12	AUDIO_I2S_SRCLK_3V3	DAP1_SCLK	B.03	PD	PD	–	1MΩ to GND	I2S1_SCLK	
13	AUDIO_CDC_IRQ_LVL	GPIO_PE6	E.06	PD	PD	–	1MΩ to GND	–	
15	GPIO_EXP_P17_3V3	–	–	Z	Z	–	1MΩ to GND	–	4
16	AO_DMIC_IN_DAT_LVL	DMIC3_DAT	E.05	PD	PD	–	1MΩ to GND	–	
18	MDM_WAKE_AP_LVL	MODEM_WAKE_AP	X.00	PD	PD	–	1MΩ to GND	–	
19	SPI1_MOSI_3V3	SPI1_MOSI	C.00	PD	PD	–	1MΩ to GND	SPI1A_DOUT	
21	SPI1_MISO_3V3	SPI1_MISO	C.01	PD	PD	–	1MΩ to GND	SPI1A_DIN	
22	GPIO_EXP_P16_3V3	–	–	Z	Z	–	1MΩ to GND	–	4
23	SPI1_SCK_3V3	SPI1_SCK	C.02	PD	PD	–	1MΩ to GND	SPI1A_SCK	
24	SPI1_CS0_3V3	SPI1_CS0	C.03	PU	PU	–	1MΩ to GND	SPI1A_CS0	
26	SPI1_CS1_3V3	SPI1_CS1	C.04	PU	PU	–	1MΩ to GND	SPI1A_CS1	
27	I2C_GP1_DAT_3V3	GEN2_I2C_SDA	–	Z	Z	1kΩ to 3.3V	–	I2C2_DAT	
28	I2C_GP1_CLK_3V3	GEN2_I2C_SCL	–	Z	Z	1kΩ to 3.3V	–	I2C2_CLK	
29	AUD_RST_LVL	GPIO_X1_AUD	BB.03	PD	PU	–	1MΩ to GND	–	
31	MOTION_INT_AP_L_LVL	MOTION_INT	X.02	PD	PU	–	47kΩ to 3.3V	–	
32	AO_DMIC_IN_CLK_LVL	DMIC3_CLK	E.04	PD	PD	–	1MΩ to GND	–	
33	AP_WAKE_BT_3V3	AP_WAKE_NFC	H.07	PD	PD	–	1MΩ to GND	–	
35	AUDIO_I2S_SFSYNC_3V3	DAP1_FS	B.00	PD	PD	–	1MΩ to GND	I2S1_LRCK	
36	UART1_CTS_HDR_3V3	UART1_CTS	U.03	PD	PD	–	100kΩ to 3.3V	UA3_CTS	
37	SAR_TOUT_LVL	ALS_PROX_INT	X.03	PD	PD	–	47kΩ to 3.3V	–	
38	AUDIO_I2S_SIN_3V3	DAP1_DIN	B.01	PD	PD	–	1MΩ to GND	I2S1_SDATA_IN	
40	AUDIO_I2S_SOUT_3V3	DAP1_DOUT	B.02	PD	PD	–	1MΩ to GND	I2S1_SDATA_OUT	

Notes:
1. Non-signal pins are not included in table.
2. PD = Tegra Internal Pull-down, PU - Tegra Internal Pull-up, Z – Tristate
3. These pins are used for RAM Code strapping on the module and may be pulled up or down with 4.7kΩ resistors. Care must be taken to make sure these signals are not pulled or driven up/down by any device connected to these pins during initial power-on.
4. These are not Jetson TX2 signals, but are included for completeness.

Table 18. Jetson TX2 Expansion Header Signal Details

Pin #	Signal Name	Tegra Ball Name	Tegra GPIO Port.#	Power-on Default State	Pin State after Pinmux Config.	External PU/PD on module	External PU/PD on carrier board	Pinmux SFIO Functions Supported	Notes
3	I2C_GP0_SDA_3V3_LVL	GEN2_I2C_SDA	–	Z	Z	1kΩ to 1.8V	–	I2C2_DAT	
5	I2C_GP0_SCL_3V3_LVL	GEN2_I2C_SCL	–	Z	Z	1kΩ to 1.8V	–	I2C2_CLK	
7	AUDIO_I2S_MCLK_3V3	AUD_MCLK	J.04	PD	PD	–	1MΩ to GND	AUD_MCLK	
8	UART1_TXD_HDR_3V3	UART1_TX	T.00	PU	PU	–	PU or PD	UA3_TXD	
10	UART1_RXD_HDR_3V3	UART1_RX	T.01	PU	PU	–	100kΩ to 3.3V	UA3_RXD	
11	UART1_RTS_HDR_3V3	UART1_RTS	T.02	PD	PD	–	PU or PD	UA3_RTS	3
12	AUDIO_I2S_SRCLK_3V3	DAP1_SCLK	J.00	PD	PD	–	1MΩ to GND	I2S1_SCLK	
13	AUDIO_CDC_IRQ_LVL	GPIO_AUD0	J.05	PD	PU	–	1MΩ to GND	–	
15	GPIO_EXP_P17_3V3	–	–	Z	Z	–	1MΩ to GND	–	4
16	AO_DMIC_IN_DAT_LVL	CAN_GPIO0	–	PD	PD	–	1MΩ to GND	DMIC3_DAT or DMIC5_DAT	
18	MDM_WAKE_AP_LVL	GPIO_MDM2	Y.01	PD	PU	–	1MΩ to GND	–	
19	SPI1_MOSI_3V3	GPIO_CAM6	N.05	PD	PD	–	1MΩ to GND	VGP6 or SPI4_DOUT	
21	SPI1_MISO_3V3	GPIO_CAM5	N.04	PD	PD	–	1MΩ to GND	VGP5 or SPI4_DIN	

Pin #	Signal Name	Tegra Ball Name	Tegra GPIO Port.#	Power-on Default State	Pin State after Pinmux Config.	External PU/PD on module	External PU/PD on carrier board	Pinmux SFIO Functions Supported	Notes
22	GPIO_EXP_P16_3V3	–	–	Z	Z	–	1MΩ to GND	–	4
23	SPI1_SCK_3V3	GPIO_CAM4	N.03	PD	PD	–	1MΩ to GND	VGP4 or SPI4_SCK	
24	SPI1_CS0_3V3	GPIO_CAM7	N.06	PU	PU	–	1MΩ to GND	SPI4_CS0	
27	I2C_GP1_DAT_3V3	GEN1_I2C_SDA	–	Z	Z	1kΩ to 3.3V	–	I2C1_DAT	
28	I2C_GP1_CLK_3V3	GEN1_I2C_SCL	–	Z	Z	1kΩ to 3.3V	–	I2C1_CLK	
29	AUD_RST_LVL	GPIO_AUD1	J.06	PD	Drive 0		1MΩ to GND	–	
31	MOTION_INT_AP_L_LVL	CAN_GPIO2	AA.02	Z	PU	–	47kΩ to 3.3V	–	
32	AO_DMIC_IN_CLK_LVL	CAN_GPIO1	–	PD	PD	–	1MΩ to GND	DMIC3_CLK DMIC5_CLK	
33	AP_WAKE_BT_3V3	GPIO_PQ5	I.05	PD	Drive 0	–	1MΩ to GND	–	
35	AUDIO_I2S_SFSYNC_3V3	DAP1_FS	J.03	PD	PD	–	1MΩ to GND	I2S1_LRCK	
36	UART1_CTS_HDR_3V3	UART1_CTS	T.03	PD	PD	–	100kΩ to 3.3V	UA3_CTS	
37	SAR_TOUT_LVL	GPIO_PQ4	I.04	PD	PU	–	47kΩ to 3.3V	–	
38	AUDIO_I2S_SIN_3V3	DAP1_DIN	J.02	PD	PD	–	1MΩ to GND	I2S1_SDATA_IN	
40	AUDIO_I2S_SOUT_3V3	DAP1_DOUT	J.01	PD	PD	–	1MΩ to GND	I2S1_SDATA_OUT	

Notes:
1. Non-signal pins and those without functionality on Jetson TX2 are not included in table.
2. PD = Tegra Internal Pull-down, PU - Tegra Internal Pull-up, Z – Tristate
3. These pins are used for RAM Code strapping on the module and may be pulled up or down with 4.7kΩ resistors. Care must be taken to make sure these signals are not pulled or driven up/down by any device connected to these pins during initial power-on.
4. These are not Jetson TX2 signals, but are included for completeness.

Expansion Header Interface Guidelines

See the Jetson TX1 or Jetson TX2 OEM Product DG for Routing Guidelines. Include the carrier board PCB trace delays in the following table when calculating max trace length & for skew matching.

Table 19. Expansion Header Related TX1 Carrier PCB Trace Delays

Jetson Module Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Expansion Module (ps)		Jetson Module Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Max Delay for Expansion Module (ps)
I2S					**SPI**			
I2S0_CLK	69	3600	3531		SPI1_SCK	791	1760	969
I2S0_LRCLK	150	3600	3450		SPI1_MISO	782	1760	978
I2S0_SDIN	60	3600	3540		SPI1_MOSI	783	1760	977
I2S0_SDOUT	127	3600	3473		SPI1_CS0#	786	1760	974
					SPI1_CS1#	791	1760	969

Notes: Max Trace Delay Allowed for SPI assumes a single load case. If two loads are implemented, See the Jetson TX1 or Jetson TX2 OEM Product Design Guide for details.

3.5 Serial Port

UART1 from the Jetson Module is routed through level shifters to a 6-pin, 2.54mm pitch male Serial Port header (J17). The connector used on the carrier board is a Samtec HTSW-106-07-FM-S.

Figure 14. Serial Port Header Connections

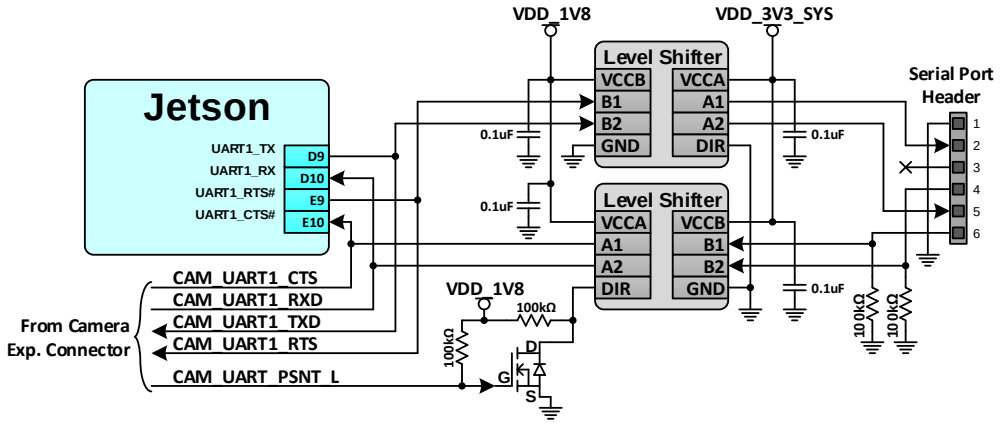


Table 20. Serial Port Header Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	SHIELD/GND	–	Ground	Ground
2	UART1_RTS_3V3_L	UART1_RTS#	UART Request to Send	Output
3	NC	–	Unused	Unused
4	UART1_RXD_3V3	UART1_RX	UART Receive	Input
5	UART1_TXD_3V3	UART1_TX	UART Transmit	Output
6	UART1_CTS_3V3_L	UART1_CTS#	UART Clear to Send	Input

Legend	Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to Serial Port header. Input is from Serial Port header. Bidir is for Bidirectional signals.

3.6 Debug Connector

The carrier board includes a 60-pin (2x30, 0.5mm pitch) Debug Connector (J10). The connector used on the Carrier board is a Samtec QSH-30-01-L-D-A-TR. The debug connector includes the following interfaces/functions:

- JTAG
- UART
- I2C (x3) (See Note)
- Power, Force Recovery & Reset Control
- GPIOs

Table 21. Debug Connector Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	ACOK	CHARGER_PRSNT#	AC power OK	Input	2	VDD_1V8	–	Main 1.8V Supply	Power
3	GND	–	Ground	Ground	4	GND	–	Ground	Ground
5	JTAG_AP_TDI	JTAG_TDI	JTAG Test Data In	Input	6	UART1_TXD_DBG_1V8	UART0_TX	UART #0 Transmit	Output
7	JTAG_AP_TMS	JTAG_TMS	JTAG Test Mode Select	Input	8	UART1_RXD_DBG_1V8	UART0_RX	UART #0 Receive	Input
9	JTAG_AP_TCK	JTAG_TCK	JTAG Test Clock	Input	10	UART1_CTS	UART0_CTS#	UART #0 Clear to Send	Input
11	JTAG_AP_RTCK	JTAG_RTCK	JTAG Return Clock	Output	12	UART1_RTS	UART0_RTS#	UART #0 Request to Send	Output
13	GND	–	Ground	Ground	14	GND	–	Ground	Ground
15	JTAG_AP_TDO	JTAG_TDO	JTAG Test Data Out	Output	16	I2C_GP0_CLK_1V8	I2C_GP0_CLK	General I2C #0 Clock	Bidir/OD
17	RESET_IN_R_L	–	Reset Input	Bidir	18	I2C_GP0_DAT_1V8	I2C_GP0_DAT	General I2C #0 Data	Bidir/OD
19	GND	–	Ground	Ground	20	NC	–	Unused	Unused
21	VDD_1V8	–	Main 1.8V Supply	Power	22	NC			
23	I2C_PM_DAT	I2C_PM_DAT	I2C Interface (PM) Data	Bidir/OD	24	GND	–	Ground	Ground
25	I2C_PM_CLK	I2C_PM_CLK	I2C Interface (PM) Clock	Bidir/OD	26	VDD_1V8	–	Main 1.8V Supply	Power
27	UART4_TXD_DBG	RSVD (D5)	UART #4 Transmit	Output	28	LED_VDD_CORE	–	Enable for SOC EN LED	Output

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default	Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
29	UART4_RXD_DBG	RSVD (D8)	UART #4 Receive	Input	30	NC	–		Unused
31	LED_VDD_CORE	–	Enable for SOC Enable LED	Output	32	DBG_GPIO1	UART0_CTS	UART #0 Clear to send	Input
33	CPU_PWR_REQ	–	Tied to GND	na	34	DBG_GPIO2	UART0_RTS	UART #0 Request to send	Output
35	GND	–	Ground	Ground	36	GND	–	Ground	Ground
37	NC	–	Unused	Unused	38	NC	–	Unused	Unused
39	NC				40	RESET_IN_R_L	RESET_IN#	From Reset Button/JTAG Conn.	Input
41	NC				42	FORCE_RECOVERY_R_L	FORCE_RECOV#	From Recovery button	Input
43	NC				44	RESET_IN_R_L	RESET_IN#	From Reset Button/JTAG Conn.	Input
45	NC				46	POWER_BTN_R	POWER_BTN#	From Power Button	Input
47	NC				48	NC	–	Unused	Unused
49	NC				50	NC			
51	GND	–	Ground	Ground	52	GND	–	Ground	Ground
53	JTAG_AP_TRST_L	JTAG_GP0	Debug GPIO #0	Input	54	I2C_GP1_CLK_3V3	I2C_GP1_CLK	General I2C #1 Clock	Bidir/OD
55	D_FORCE_OFF_L	–	Force Off	Input	56	I2C_GP1_DAT_3V3	I2C_GP1_DAT	General I2C #1 Data	Bidir/OD
57	NC	–	Unused	Unused	58	GND	–	Ground	Ground
59	NC				60	VAUX_5V	–	5V Supply from Debug Conn.	Power

Legend

Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to Debug Module. Input is from Debug Module. Bidir is for Bidirectional signals.

Debug Connector Interface Guidelines

See the Jetson TX1 or Jetson TX2 OEM Product DG for Routing Guidelines. Include the carrier board PCB trace delays when calculating max trace length & for skew matching.

3.7 GPIO Expansion Header

The carrier board includes a 30-pin (2x15, 2.54mm pitch) GPIO Expansion Header (J26) including an I2S IF and several GPIOs.

Table 22. GPIO Expansion Header Pin Descriptions

Pin #	Signal Name	Associated Jetson Module Pin Name	Usage/Description	Type/ Direction	Signal Voltage Level at Header	GPIO Max Drive (I_{OL}/I_{OH}) or Power Pin Current Capability	Notes
1	CAN_WAKE	CAN_WAKE	CAN Wake	Output	3.3V	1mA / -1mA	2, 4
2	VDD_3V3_SYS	–	Main 3.3V Supply	Power	–	1A	1
3	CAN0_STBY	–	Unused	Unused	–	–	–
4	VDD_1V8	–	Main 1.8V Supply	Power	–	1A	1
5	CAN0_RX	CAN0_RX	CAN #0 Receive	Output	3.3V	1mA / -1mA	2, 4
6	AP2MDM_READY	GPIO15_AP2MDM_READY	AP to Modem Ready GPIO	Bidir	–	1mA / -1mA	2, 4
7	CAN0_TX	CAN0_TX	CAN #0 Transmit	Input	3.3V	1mA / -1mA	2, 4
8	VDD_5V0_IO_SYS	–	Main 5.0V Supply	Power	–	1A	1
9	CAN0_ERR	CAN0_ERR	CAN #0 Error	Output	3.3V	1mA / -1mA	2, 4
10	GND	–	Ground	Ground	–	–	–
11	GND	–	Ground	Ground	–	–	–
12	I2C_GP2_CLK	I2C_GP2_CLK	General I2C #2 Clock	Bidir/OD	1.8V	1mA / -1mA	2
13	CAN1_STBY	CAN1_STBY	CAN #1 Standby	Input	3.3V	1mA / -1mA	2, 4
14	I2C_GP2_DAT	I2C_GP2_DAT	General I2C #2 Data	Bidir/OD	1.8V	1mA / -1mA	2
15	CAN1_RX	CAN1_RX	CAN #1 Receive	Output	3.3V	1mA / -1mA	2, 4
16	WDT_TIME_OUT_L	WDT_TIME_OUT#	Watchdog Timer Output	Output		1mA / -1mA	2, 4
17	CAN1_TX	CAN1_TX	CAN #1 Transmit	Input	3.3V	1mA / -1mA	2, 4
18	I2C_GP3_CLK	I2C_GP3_CLK	General I2C #3 Clock	Bidir/OD	1.8V	1mA / -1mA	2
19	CAN1_ERR	CAN1_ERR	CAN #1 Error	Output	3.3V	1mA / -1mA	2, 4
20	I2C_GP3_DAT	I2C_GP3_DAT	General I2C #3 Data	Bidir/OD	1.8V	1mA / -1mA	2
21	GND	–	Ground	Ground	–	–	–
22	SLEEP	SLEEP#	Sleep Indicator	Output	1.8V	1mA / -1mA	2, 4
23	I2S1_CLK	I2S1_CLK	I2S #1 Clock	Bidir	1.8V	1mA / -1mA	2
24	I2S1_SDOUT	I2S1_SDOUT	I2S #1 Data Out	Bidir	1.8V	1mA / -1mA	2
25	I2S1_SDIN	I2S1_SDIN	I2S #1 Data In	Input	1.8V	1mA / -1mA	2, 4
26	I2S1_LRCLK	I2S1_LRCLK	I2S #1 Left/Right Clock	Bidir	1.8V	1mA / -1mA	2
27	DSPK_OUT_CLK	DSPK_OUT_CLK	Digital Speaker Out Clock	Output	1.8V	1mA	2, 4

Pin #	Signal Name	Associated Jetson Module Pin Name	Usage/Description	Type/ Direction	Signal Voltage Level at Header	GPIO Max Drive (I_{OL}/I_{OH}) or Power Pin Current Capability	Notes
28	GND	–	Ground	Ground	–	–	–
29	DSPK_OUT_DAT	DSPK_OUT_DAT	Digital Speaker Out Data	Output	1.8V	1mA	2, 4
30	GNSS_PSS	Reserved	–	–	–	–	–

Legend

Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved/Not Available

Notes:
1. This is current capability per power pin.
2. These pins are directly connected to Tegra. The max drive that meets full Data Sheet V_{OL}/V_{OH} is 1mA. 2mA drive is supported at restricted V_{OL}/V_{OH} levels. See the associated OEM Product Design Guide Pads section for details.
3. In the Type/Dir column, Output is to Exp. Module. Input is from Exp. Module. Bidir is for Bidirectional signals.
4. The direction indicated matches that indicated in the reference design schematics. These signals can be bidirectional.

Table 23. Jetson TX1 GPIO Expansion Header Signal Details

Pin #	Signal Name	Tegra Ball Name	Tegra GPIO Port.#	Power-on Default State	Pin State after Pinmux Config.	External PU/PD on module	External PU/PD on carrier board	Pinmux SFIO Functions Supported	Notes
6	AP2MDM_READY	AP_READY	V.05	PD	Drive 0	–	–	–	
22	SLEEP	BUTTON_SLIDE_SW	Y.00	PU	PU	–	–	–	
23	I2S1_CLK	GPIO_PK3	–	PD	PD	–	–	I2S5B_SCLK	
24	I2S1_SDOUT	GPIO_PK2	–	PD	PD	–	–	I2S5B_SDATA_OUT	
25	I2S1_SDIN	GPIO_PK1	–	PD	PD	–	–	I2S5B_SDATA_IN	
26	I2S1_LRCLK	GPIO_PK0	–	PD	PD	–	–	I2S5B_LRCK	

Notes:
1. Signal pins that do not have functionality on Jetson TX1 are not included above.
2. PD = Tegra Internal Pull-down, PU - Tegra Internal Pull-up, Z – Tristate.

Table 24. Jetson TX2 GPIO Expansion Header Signal Details

Pin #	Signal Name	Tegra Ball Name	Tegra GPIO Port.#	Power-on Default State	Pin State after Pinmux Config.	External PU/PD on module	External PU/PD on carrier board	Pinmux SFIO Functions Supported	Notes
1	CAN_WAKE	CAN_GPIO4	AA.04	Z	PU	–	–	–	
5	CAN0_RX	CAN0_DIN	–	PU	PU	–	–	CAN0_DIN	
6	AP2MDM_READY	UFS0_REF_CLK	BB.00	Drive 0	Drive 0	–	–	–	
7	CAN0_TX	CAN0_DOUT	–	PU	PU	–	–	CAN0_DOUT	
9	CAN0_ERR	CAN0_GPIO5	AA.05	Z	Z	–	–	–	
12	I2C_GP2_CLK	GEN7_I2C_SCL	L.00	Z	Z	1kΩ to 1.8V	–	I2C7_CLK	
13	CAN1_STBY	CAN0_GPIO6	AA.06	PD	Drive 0	–	–	–	
14	I2C_GP2_DAT	GEN7_I2C_SDA	L.01	Z	Z	1kΩ to 1.8V	–	I2C7_DAT	
15	CAN1_RX	CAN0_DIN	–	PU	PU	–	–	CAN1_DIN	
16	WDT_TIME_OUT_L	GPIO_SEN7	V.07	Drive 1	Drive 1	–	–	WDT_RESET_OUTA	
17	CAN1_TX	CAN0_DOUT	–	PU	PU	–	–	CAN1_DOUT	
18	I2C_GP3_CLK	GEN9_I2C_SCL	L.02	Z	Z	1kΩ to 1.8V	–	I2C9_CLK	
19	CAN1_ERR	CAN0_GPIO3	AA.03	Z	Z	–	–	–	
20	I2C_GP3_DAT	GEN9_I2C_SDA	L.03	Z	Z	1kΩ to 1.8V	–	I2C9_CLK	
22	SLEEP	GPIO_SW2	FF.02	PU	PU	–	–	–	2
23	I2S1_CLK	DAP2_SCLK	–	PD	PD	–	–	I2S2_SCLK	
24	I2S1_SDOUT	DAP2_DOUT	–	PD	PD	–	–	I2S2_SDATA_OUT	
25	I2S1_SDIN	DAP2_DIN	–	PD	PD	–	–	I2S2_SDATA_IN	
26	I2S1_LRCLK	DAP2_FS	–	PD	PD	–	–	I2S2_LRCK	
27	DSPK_OUT_CLK	GPIO_AUD3	K.00	PU	PU	–	–	DSPK1_CLK SPDIF_OUT	
29	DSPK_OUT_DAT	GPIO_AUD2	J.07	PD	PD	–	–	DSPK1_DAT SPDIF_IN	

Notes:
1. PD = Tegra Internal Pull-down, PU - Tegra Internal Pull-up, Z – Tristate.

2. This pin is used for RAM Code strapping on the module and may be pulled up or down with 4.7kΩ resistors. Care must be taken to make sure this signal is not pulled or driven up/down by any device connected to these pins during initial power-on.

GPIO Header Interface Guidelines

See the Jetson TX1 or Jetson TX2 OEM Product DG for Routing Guidelines. Include the carrier board PCB trace delays in the following table when calculating max trace length & for skew matching.

Table 25. GPIO Header Related TX1 Carrier PCB Trace Delays

Jetson Module Signal	Carrier Board PCB Delay (ps)	Max Trace Delay Allowed (ps)	Avail. Trace Delay for GPIO Module (ps)
I2S1_CLK	900	3600	2700
I2S1_SDIN	893	3600	2707
I2S1_SDOUT	916	3600	2684
I2S1_LRCLK	911	3600	2689
CAN0_RX	850	1360	510
CAN0_TX	825	1360	535
CAN1_RX	876	1360	484
CAN1_TX	886	1360	474

3.8 Charge Control Receptacle

The Jetson carrier board includes a 10-pin, 0.8mm pitch flex receptacle (J27) including an I2C IF & charge control/status signals.

Table 26. Charge Control Receptacle Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	ACOK	CHARGER_PRSNT#	AC power OK	Input
2	CHARGING	CHARGING#	Charging indicator	Input
3	LOW_BAT	BATLOW#	Low Battery indicator	Input
4	GND	–	Ground	Ground
5	I2C_PM_CLK	I2C_PM_CLK	I2C (Power Monitor) Clock	Bidir/OD
6	I2C_PM_DAT	I2C_PM_DAT	I2C (Power Monitor) Data	Bidir/OD
7	CHG_OC_L (Jetson TX1) INA_PREG_THERM_WARN_L (Jetson TX2)	RSVD (C8)	SOC THERM on Tegra BATT_OC on PMIC	Input
8	BAT_DET_L	–	Battery Detect – Pulled up to VDD_3V3_SYS	Na
9	TYPEC_INT	–	Type C Interrupt from 1.8V GPIO Exp. P0	Output
10	CHG_BD_PRSNT_L	–	Charge Present from 1.8V GPIO Exp. P14	Output

Legend Ground | Power | Not available on Jetson TX1 | Not available on Jetson TX2 | Reserved | Unassigned on carrier board

Notes:
- In the Type/Dir column, Output is to Charger Ctrl board. Input is from Charger Ctrl board. Bidir is for Bidirectional signals.
- When a Jetson TX2 module is used, an Auto-Power-On option is available. To enable this function, the CHARGER_PRSNT# pin must be tied to GND. This can be accomplished by installing a 0Ω resistor at R313. This will allow the Developer Kit carrier board to power on immediately after the main power is connected (without the need for a power button press. This will not work with the Jetson TX1 module.

Charge Receptacle Interface Guidelines

See the Jetson TX1 or Jetson TX2 OEM Product DG for Routing Guidelines. Include the carrier board PCB trace delays when calculating max trace length & for skew matching.

3.9 Fan Connector

The Jetson carrier board includes a 4-pin Fan Header (J15).

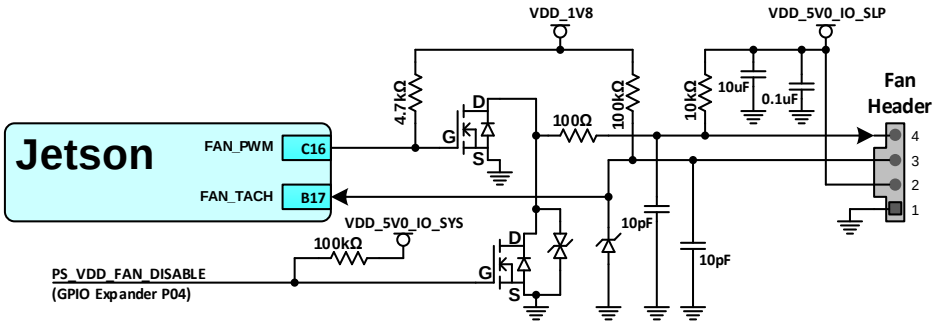


Table 27. Fan Connector Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	GND	–	Ground	Ground
2	VDD_5V0_IO_SLP	–	Gated version of Main 5.0V Supply (Enabled by VDD_3V3_SLP)	Power
3	FAN_TACH	FAN_TACH	Fan Tachometer signal	Input
4	FAN_PWM_Q*	FAN_PWM	Fan Pulse Width Modulation signal	Output

Legend	Ground	Power	Not available on Jetson TX1	Not available on Jetson TX2	Reserved	Unassigned on carrier board

Notes: In the Type/Dir column, Output is to Fan Connector. Input is from Fan Connector. Bidir is for Bidirectional signals.

3.10 DC Power Jack

The Jetson carrier board uses a DC power jack (J25) to bring in the power from the included DC power supply. The jack used on the Carrier board is a Singatron Enterprise 2DC-213-B51. The mating plug is the Singatron Enterprise 2DP-313-B01.

Table 28. DC Jack Pin Descriptions

Pin #	Signal Name	Jetson Module Pin Name	Usage/Description	Type/Dir Default
1	VDD_19V_CON	–	Main DC input supplying VDD_IN/VDD_MOD	Power
2	GND	–	Ground	Ground
3	GND	–	Ground	Ground
4	GND	–	Ground	Ground
5	GND	–	Ground	Ground
6	GND	–	Ground	Ground

4.0 MISCELLANEOUS

4.1 GPIO Expanders

The carrier board design includes two I2C interface controlled GPIO expander ICs. One operates at 1.8V and the other at 3.3V. The GPIO pins on the expanders are either used to interface to onboard devices/supplies or are routed to several of the expansion connectors. The connections are shown in the figures & tables below. The I2C address for the 1.8V GPIO Expander is strapped to be 7'h77, while the address for the 3.3V GPIO expander is strapped to 7'h74.

Figure 15. GPIO Expander (1.8V)

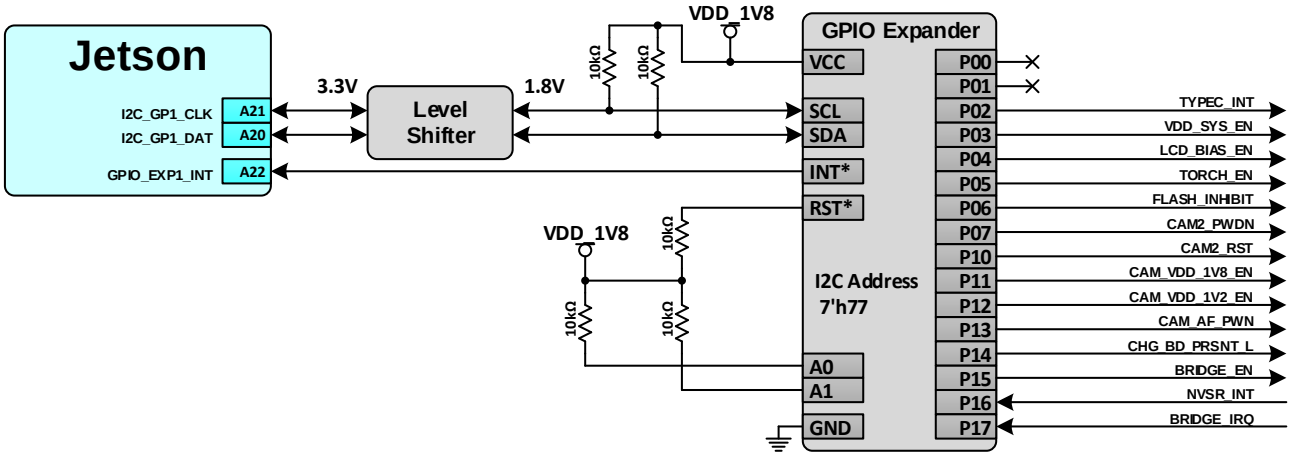


Table 29. 1.8V GPIO Expansion Signal Descriptions

Expander GPIO #	Carrier Board Signal Name	Usage/Description	Direction
P00	No connect	Not available for use	NA
P01	No connect	Not available for use	NA
P02	TYPEC_INT	Type C Interrupt – to pin 9 of Charger Control header (J27)	Output
P03	VDD_SYS_EN	VDD_SYS enable - to pin 119 of Camera Expansion connector (J22)	Output
P04	LCD_BIAS_EN	LCD Bias Enable - to pin 88 of Display Expansion connector (J23)	Output
P05	TORCH_EN	Torch Enable - to pin 104 of Camera Expansion connector (J22)	Output
P06	FLASH_INHIBIT	Flash inhibit - to pin 103 of Camera Expansion connector (J22)	Output
P07	CAM2_PWDN	Camera #2 Power-down - to pin 96 of Camera Expansion connector (J22)	Output
P10	CAM2_RST	Camera #2 Reset - to pin 98 of Camera Expansion connector (J22)	Output
P11	CAM_VDD_1V8_EN	Camera 1.8V supply enable – to ON pin of load switch supplying DVDD_CAM_IO_1V8 to Camera Expansion connector (J22) on carrier board.	Output
P12	CAM_VDD_1V2_EN	Camera 1.2V supply enable – to chip enable of 1.2V LDO supplying DVDD_CAM_IO_1V2 to Camera Expansion connector (J22) on carrier board.	Output
P13	CAM_AF_PWDN	Camera Autofocus Power-down - to pin 85 of Camera Expansion connector (J22)	Output
P14	CHG_BD_PRSNT_L	Type C Interrupt – to pin 10 of Charger Control header (J27)	Output
P15	BRIDGE_EN	Bridge Enable - to pin 18 of Display Expansion connector (J23)	Output
P16	NVSR_INT	Nvidia Sensor Interrupt - to pin 98 of Display Expansion connector (J23)	Input
P17	BRIDGE_IRQ	Bridge Interrupt - to pin 20 of Display Expansion connector (J23)	Input

Notes: In the Direction column, Output is from GPIO expander. Input is to GPIO expander. Bidir is for Bidirectional signals.

Figure 16. GPIO Expander (3.3V)

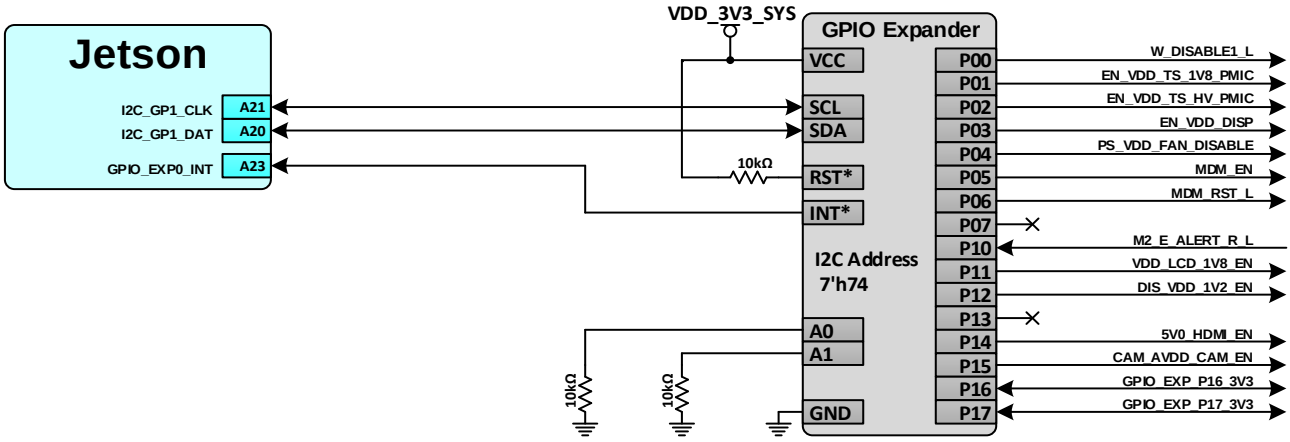


Table 30. 3.3V GPIO Expansion Signal Descriptions

Expander GPIO #	Carrier Board Signal Name	Usage/Description	Direction
P00	W_DISABLE1_L	WLAN Disable 1 - to pin 56 of M.2 Key E connector (J18)	Output
P01	EN_VDD_TS_1V8_PMIC	Touchscreen 1.8V supply enable – to ON pin of 1.8V load switch supplying VDD_TS_1V8 to Display Expansion connector (J23) on carrier board.	Output
P02	EN_VDD_TS_HV_PMIC	Touchscreen 3.3V supply enable – to ON pin of 3.3V load switch supplying AVDD_TS_DIS to Display Expansion connector (J23) on carrier board.	Output
P03	EN_VDD_DISP	Display 3.3V supply enable – to ON pin of load switch supplying VDD_DIS_3V3_LCD to Display Expansion connector (J23) on carrier board.	Output
P04	PS_VDD_FAN_DISABLE	Fan disable – Enables/Disables PWM going to fan header (J15)	Output
P05	MDM_EN	Modem Enable – Not assigned (goes to unstuffed R526)	Output
P06	MDM_RST_L	Modem Reset – Not assigned (goes to unstuffed R527)	Output
P07	No connect	Not available for use	NA
P10	M2_E_ALERT_R_L	M2 Key E alert – from pin 62 of M.2 connector (J18)	Input
P11	VDD_LCD_1V8_EN	LCD 1.8V supply enable – to ON pin of load switch supplying VDD_LCD_1V8_DIS to Display Expansion connector (J23) on carrier board.	Output
P12	DIS_VDD_1V2_EN	LCD 1.2V supply enable – to chip enable of LDO supplying VDD_1V2 to Display Expansion connector (J23) on carrier board.	Output
P13	5V0_HDMI_EN	HDMI 5V Enable – to enable of load switch supplying VDD_5V0_HDMI_CON on carrier board.	Output
P14	No connect	Not available for use	NA
P15	CAM_AVDD_CAM_EN	Camera analog supply enable – to enable of 2.8V LDO supplying AVDD_CAM to Camera Expansion connector (J22) on carrier board.	Output
P16	GPIO_EXP_P16_3V3	GPIO expander P16 – connects to Expansion Header (J21) pin 22.	Bidir
P17	GPIO_EXP_P17_3V3	GPIO expander P17 – connects to Expansion Header (J21) pin 15.	Bidir

Notes: In the Direction column, Output is from GPIO expander. Input is to GPIO expander. Bidir is for Bidirectional signals.

4.2 Buttons, Jumpers & Indicators

Table 31. Buttons (switches)

Button	Description	Usage
S1	Reset button	Used to force a full system reset.
S2	Volume down (Sleep) button	Used to put system into sleep mode.
S3	Recovery button	Used to enter Force Recovery Mode. Button is held down while either system is first powered on, or by pressing & releasing reset button while Recovery button is pressed.
S4	Power button	Used to power system up if off, or power down if on. If held for >10 seconds, will force a full system power cycle.

Table 32. Jumpers

Jumper	Description	Usage
J3	Reset switch header	Available if a remote reset button is required.
J4	Power LED header	Available to connect to remote Power LED
J6	Power switch header	Available if a remote power button is required.
J8	Reset out Header	Used to hold Tegra in reset. Jumper must be installed in order to enter boundary scan test mode.
J9	Force recovery header	Available if a remote force recovery button is required.
J11	Force off header	Can be jumpered to force system to off state. Also available if a remote button is required to force system off.
J24	Voltage select header	Selects the level shifter voltage on the non-Jetson module side of the level shifters for the signals listed below. When a jumper is on pins 1-2, 3.3V level is selected. When on pins 2-3, 1.8V level is selected. - AUDIO_I2S_MCLK/SFSYNC/SOUT/SIN/SRCLK, AUDIO_CDC_IRQ, AUD_RST - MDM_WAKE_AP_1V8 - SPI1_MOSI/MISO/SCK/CS0/CS1 - AP_WAKE_BT - AO_DMIC_IN_CLK/DAT

Table 33. Indicators (LEDs)

LEDs	Description	Usage
CR1	SOC Enable LED (Green)	Indicates when the VDD_CORE (SOC) supply is active.
CR2	Power LED (Green)	Indicates when the carrier board is powered on (VDD_1V8 & VDD_3V3_SYS rails are valid).
CR3	M.2 LED #2 (Green)	Indicates when the M.2 Key E LED2# is active.
CR4	M.2 LED #1 (Green)	Indicates when the M.2 Key E LED1# is active.
CR5	VDD_IN LED (Red)	Indicates when main 5.5V-19.6V supply is active and connected to the carrier board.
CR6	PCIe/SATA 12V LED #2 (Red)	Indicates when the 12V supply for PCIe/SATA is active.

4.3 Power Monitors

There are two Power monitors on the Jetson TX1/TX2 carrier board. One monitors the main DC input (VDD_MUX), the main 5V IO supply (VDD_5V0_IO_SYS) and the main 3.3V system supply (VDD_3V3_SYS). The other monitors the 3.3V Run Supply (VDD_3V3_SLP), the main 1.8V system supply (VDD_1V8) and the M.2 3.3V supply (VDD_3V3_SYS_M2). The I2C interface used for both monitors is I2C_GP1. The I2C address for the first power monitor is 7'h42 and for the second power monitor is 7'h43.

Figure 17. Power Monitor (VDD_MUX, VDD_5V0_IO_SYS, VDD_3V3_SYS)

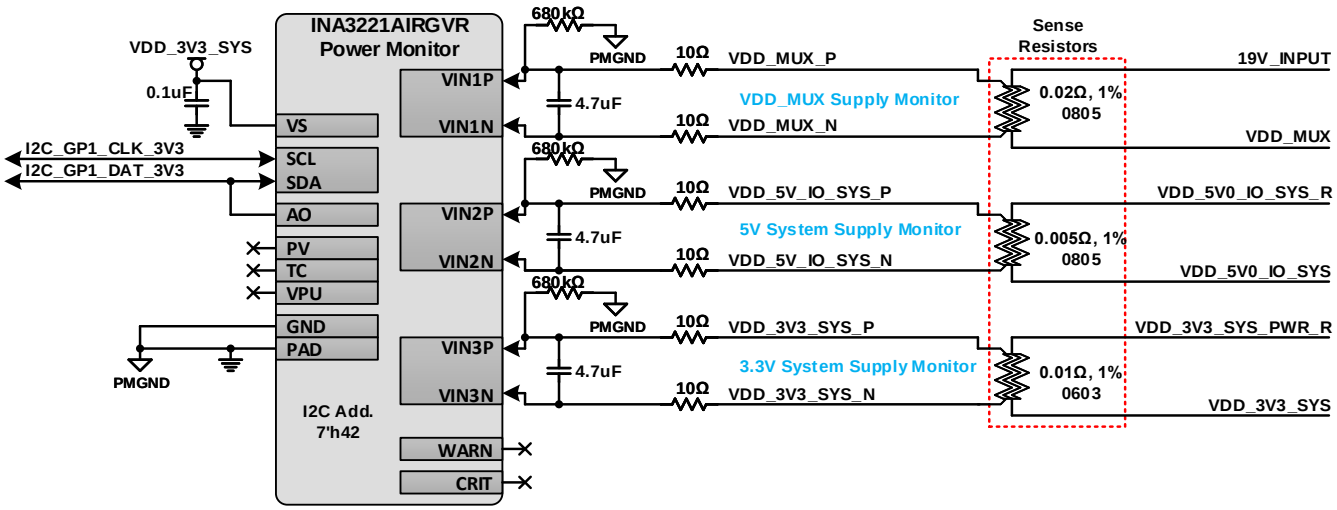
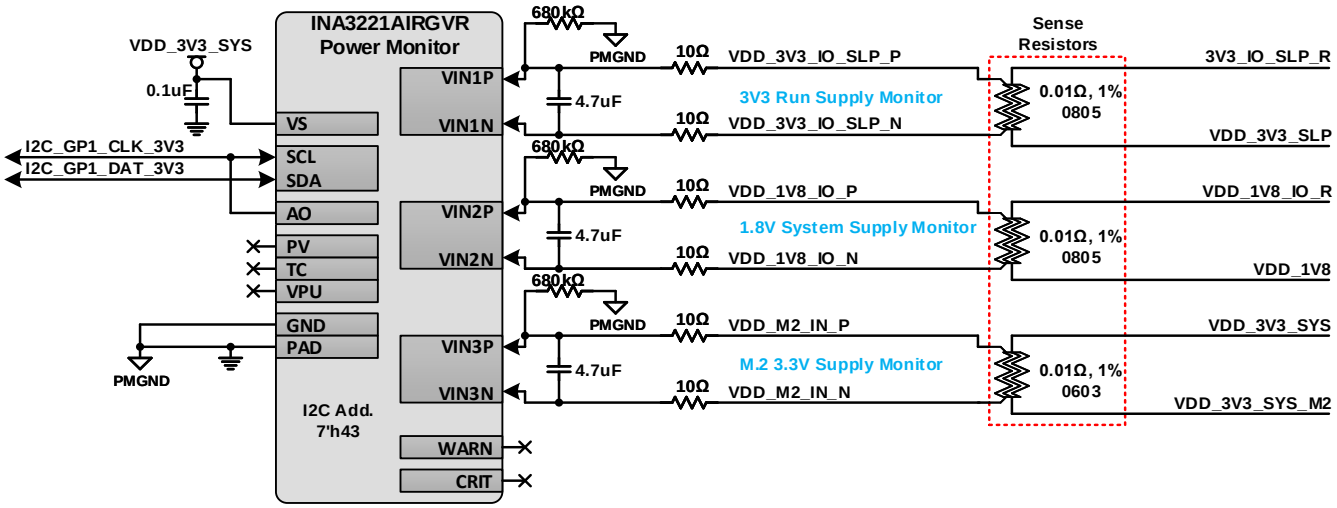
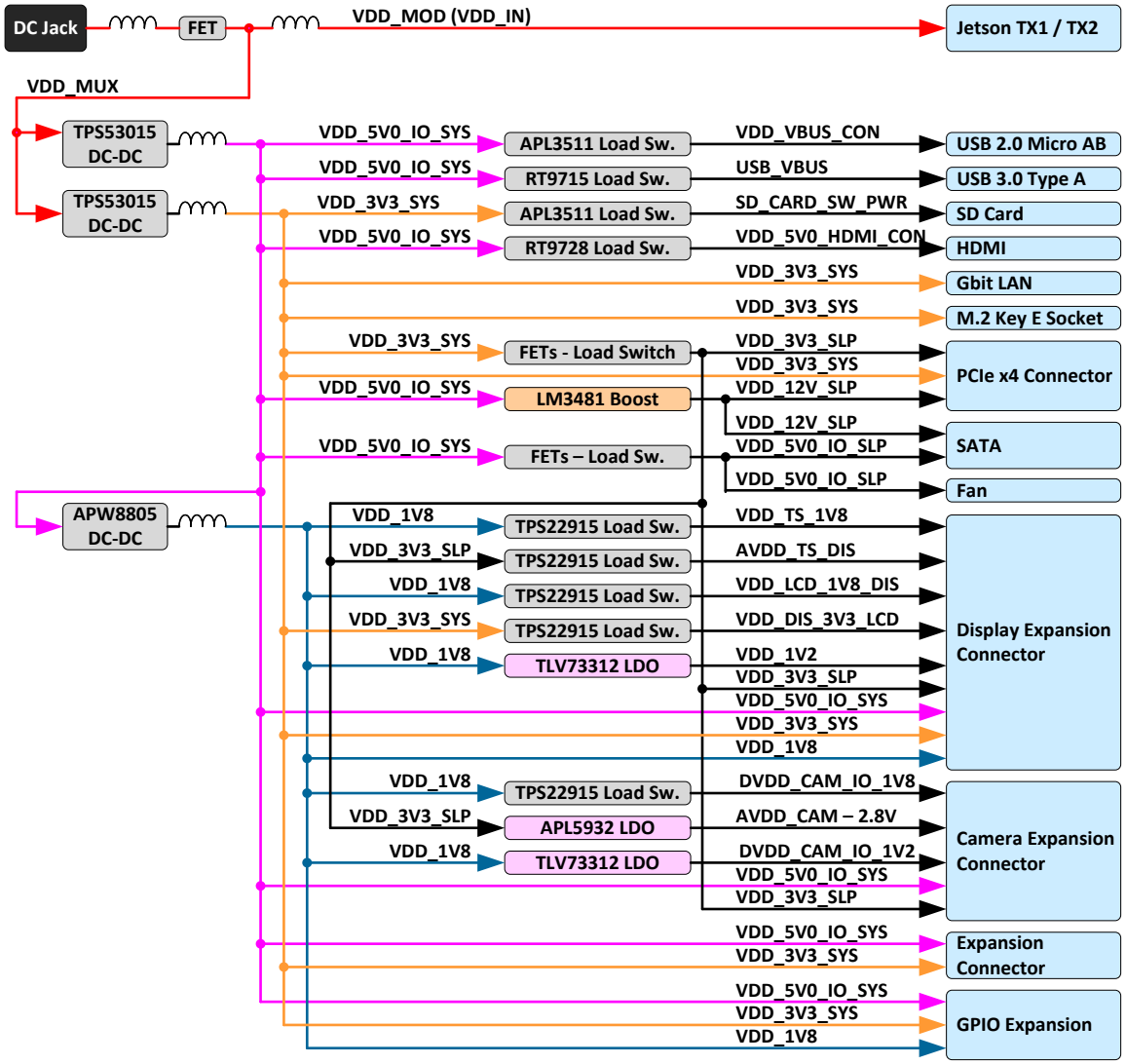


Figure 18. Power Monitor (VDD_3V3_SLP, VDD_1V8, VDD_3V3_SYS_M2)



5.0 INTERFACE POWER

Figure 19. Interface Connector Power Diagram



The tables below show the allocation of supplies to the connectors on the Jetson carrier board and current capabilities.

Table 34 Interface Power Supply Allocation

Power Rails	Usage	(V)	Power Supply or Gate	Source	Enable
VDD_IN/VDD_MUX	Main power input from DC Adapter	5.5-19.6	FETs	**DC Adapter**	
VDD_5V0_IO_SYS	Main 5V supply	5.0	TPS53015	**VDD_MUX**	CARRIER_PWR_ON
VDD_3V3_SYS	Main 3.3V supply	3.3	TPS53015	**VDD_MUX**	3V3_SYS_BUCK_EN
VDD_1V8	Main 1.8V supply	1.8	APW8805	**VDD_5V0_IO_SYS**	1V8_IO_VREG_EN (VDD_3V3_SYS_PG)
VDD_3V3_SLP	3.3V rail, off in Sleep (various)	3.3	FETs	**VDD_3V3_SYS**	SOC_PWR_REQ
VDD_5V0_IO_SLP	5V rail, off in Sleep (SATA/FAN)	5.0	FETs	**VDD_5V0_IO_SYS**	SOC_PWR_REQ
VDD_12V_SLP	12V rail, off in Sleep (PCIe® x4 & SATA)	12.0	LM3481MMX Boost	**VDD_5V0_IO_SYS**	VDD_3V3_SLP
VDD_VBUS_CON	5V VBUS for USB 2.0 Type AB conn.	5.0	APL3511CBI Load Switch	**VDD_5V0_IO_SYS**	USB_VBUS_EN0
USB_VBUS	5V VBUS for USB 3.0 Type A conn.	5.0	RT9715 Load Switch	**VDD_5V0_IO_SYS**	USB_VBUS_EN1
SD_CARD_SW_PWR	SD Card power rail	3.3	APL3511DBI Load Switch	**VDD_3V3_SYS**	SDCARD_VDD_EN
VDD_5V0_HDMI_CON	5V rail for HDMI connector		RT9728 Load Switch	**VDD_5V0_IO_SYS**	5V0_HDMI_EN (GPIO Expander U32, P14)
VDD_TS_1V8	1.8V rail for touch screen		TPS22915 Load Switch	**VDD_1V8**	EN_VDD_TS_1V8_PMIC (GPIO Expander U32, P01)
AVDD_TS_DIS	High voltage rail for touch screen	3.3	TPS22915 Load Switch	**VDD_3V3_SLP**	EN_VDD_TS_HV_PMIC (GPIO Expander U32, P02)
VDD_LCD_1V8_DIS	1.8V rail for panel		TPS22915 Load Switch	**VDD_1V8**	VDD_LCD_1V8_EN (GPIO Expander U32, P11)
VDD_DIS_3V3_LCD	High voltage rail for panel		TPS22915 Load Switch	**VDD_3V3_SYS**	EN_VDD_DISP (GPIO Expander U32, P03)
VDD_1V2	Generic 1.2V display rail	1.2	TLV73312 LDO	**VDD_1V8**	DIS_VDD_1V2_EN (GPIO Expander U32, P12)
VDD_SYS_BL	Rail to LCD backlight driver	Device Dep.	Stuffing option Resistors	**VDD_MUX VDD_5V0_IO_SYS**	Na
DVDD_CAM_IO_1V8	1.8V rail for camera I/O	1.8	TPS22915 Load Switch	**VDD_1V8**	CAM_VDD_1V8_EN (GPIO Expander U31, P11)
AVDD_CAM	High voltage rail for cameras	2.8	APL5932	**VDD_3V3_SLP**	CAM_AVDD_CAM_EN (GPIO Expander U32, P15)
DVDD_CAM_IO_1V2	1.2V rail for camera I/O	1.2	TLV73312	**VDD_1V8**	CAM_VDD_1V2_EN (GPIO Expander U31, P12)

Table 35 Interface Supply Current Capabilities

Power Rails	Usage	(V)	Max Current (mA)
VDD_IN/VDD_MUX	Main power input from DC Adapter	5.5-19.6	~4000
VDD_5V0_IO_SYS	Main 5V supply	5.0	7000
VDD_3V3_SYS	Main 3.3V supply	3.3	7000
VDD_1V8	Main 1.8V supply	1.8	2000
VDD_12V_SLP	12V rail for PCIe x4 & SATA	12.0	2300
DVDD_CAM_IO_1V8	1.8V rail for camera I/O	1.8	1000
AVDD_CAM	High voltage rail for cameras	2.8	1000
DVDD_CAM_IO_1V2	1.2V rail for camera I/O	1.2	200

Notes:
1. When operated near the minimum voltage, the power supported by some of the supplies may be reduced.
2. The supplied power adapter is rated to 90W.
3. The values shown in the “Supported Current” column indicate the total power available on the expansion connectors (not per pin).
4. If a given voltage rail cannot provide enough current, a possible solution is for the user to use a regulator from VDD_5V0_IO_SYS, VDD_3V3_SYS or VDD_1V8 to generate the desired rail.

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