Pin Descriptions – SPI Mode/ Mode_SEL = 1 kΩ to VDD

PIN		TYPE	DESCRIPTION
NAME	NO.		
CONTROL/INDICATOR I/O			
ENABLE	6	Input, 4-Level	Powers down device when pulled low 1 kΩ to VDD: • Power down until valid signal detected Float(**Default**): • Power down until valid signal detected 20 kΩ to GND: • Reserved 1 kΩ to GND: • Power down including signal detects and Reset Registers upon power-up
LOCK	16	Output, 2.5-V LVCMOS, 2-Level	Indicates CDR lock detect status High: • CDR locked Low: • CDR not locked
LOS_INT_N	13	Output, LVCMOS Open-Drain, 2-Level	Programmable Interrupt caused by change in LOS, violation of internal eye monitor threshold, or change in lock. External 4.7-kΩ pullup resistor is required. This pin is 3.3-V LVCMOS tolerant.
MISO	15	Output, 2.5-V LVCMOS, 2-Level	SPI Master Input / Slave Output. LMH1218 SPI data transmit
MODE_SEL	1	Input, 4-Level	Determines Device Configuration: SPI or SMBus 1 kΩ to VDD: • SPI mode. See *Initialization Set Up*.
MOSI	4	Input, 2-Level	SPI Master Output / Slave Input. LMH1218 SPI data receive
RESERVED	5, 17, 18	—	No Connect
SCK	3	Input, 2.5V LVCMOS, 2-Level	SPI serial clock input
SMPTE_10GbE	14	—	No Connect
SS_N	2	Input, 2-Level	SPI Slave Select. This pin has internal pullup
HIGH-SPEED DIFFERENTIAL I/O			
IN0+	11	Input, Analog	Inverting and noninverting differential inputs. An on-chip 100-Ω terminating resistor connects IN0+ to IN0-. Inputs require 4.7-µF, AC-coupling capacitors.
IN0–	12	Input, Analog	
IN1+	8	Input, Analog	Inverting and noninverting differential inputs. An on-chip 100-Ω terminating resistor connects IN1+ to IN1-. Inputs require 4.7-µF, AC-coupling capacitors.
IN1–	9	Input, Analog	
OUT0+	20	Output, 75-Ω CML Compatible	Inverting and noninverting 75-Ω outputs. An on-chip 75-Ω terminating resistor connects OUT0+ and OUT0- to VDD. Outputs require 4.7-µF, AC-coupling capacitors
OUT0–	19	Output, 75-Ω CML Compatible	
OUT1+	23	Output, Analog	Inverting and noninverting differential outputs. An on-chip 100-Ω terminating resistor connects OUT1+ to OUT1-. Outputs require 4.7-µF, AC-coupling capacitors
OUT1–	22	Output, Analog	
POWER			
DAP	—	Ground	Exposed DAP, connect to GND using at least 5 vias (see package drawing)
VDD	7, 21	2.5-V Supply	2.5 V ± 5%
VSS	10, 24	Ground	Ground