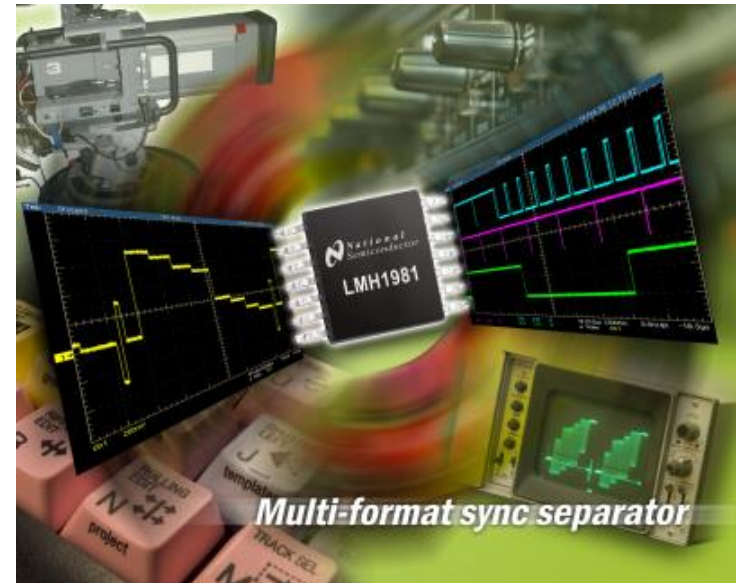


LMH1981 Video Sync Separator

Features and Benefits

- **Supports major analog video standards**
 - NTSC, PAL, 480I/P, 576I/P, 720P, 1080I/P
 - Auto format detection
- **Low HSYNC output jitter**
 - Helps to meet 3G-SDI Output Timing Jitter spec and/or relax PLL loop bandwidth
- **50% sync slicing of 0.5 to 2 VPP inputs**
 - Supports improper video input termination
- **Low HSYNC propagation delay variation**
 - Reduces PLL clock phase drift
- **-40 to +85°C operation**
- **3.3 to 5V supply voltage**



Multi-format sync separator

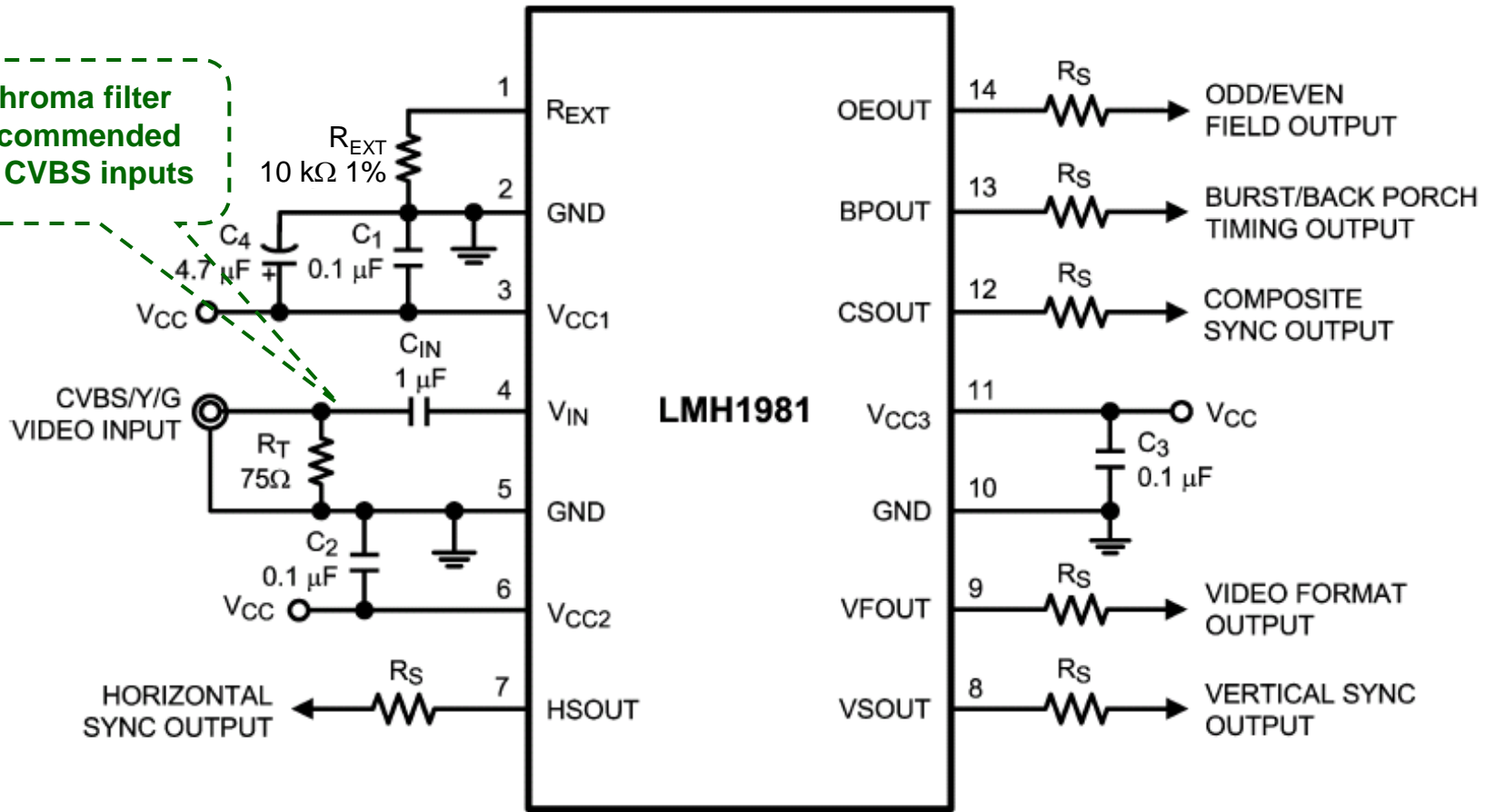
Applications

- **Broadcast/Pro Video Equipment**
- **Genlock Circuits**
- **Video Capture and Editing**
- **Set-Top Boxes (STB) & Digital Video Recorders (DVR)**
- **HDTV/DTV Systems**
- **TV/Video Displays**

Pinout and Test Circuit

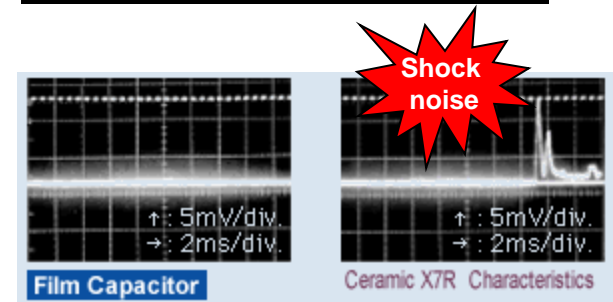
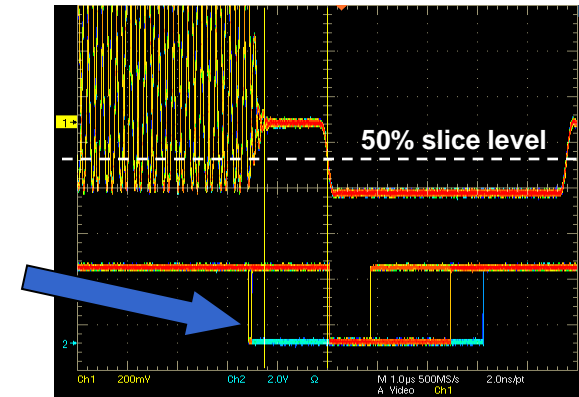
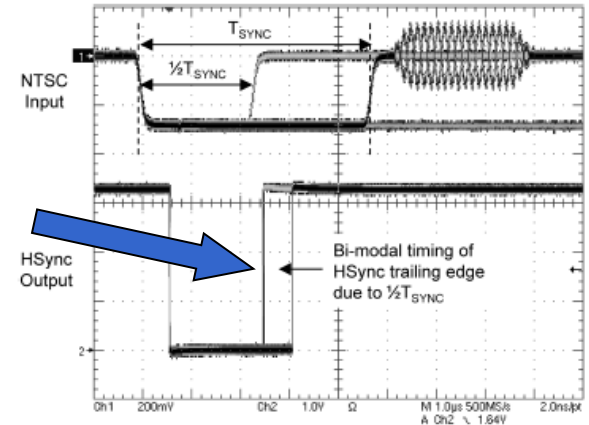
Low component count, small TSSOP package → Easy application

Chroma filter recommended for CVBS inputs



LMH1981 Design Tips

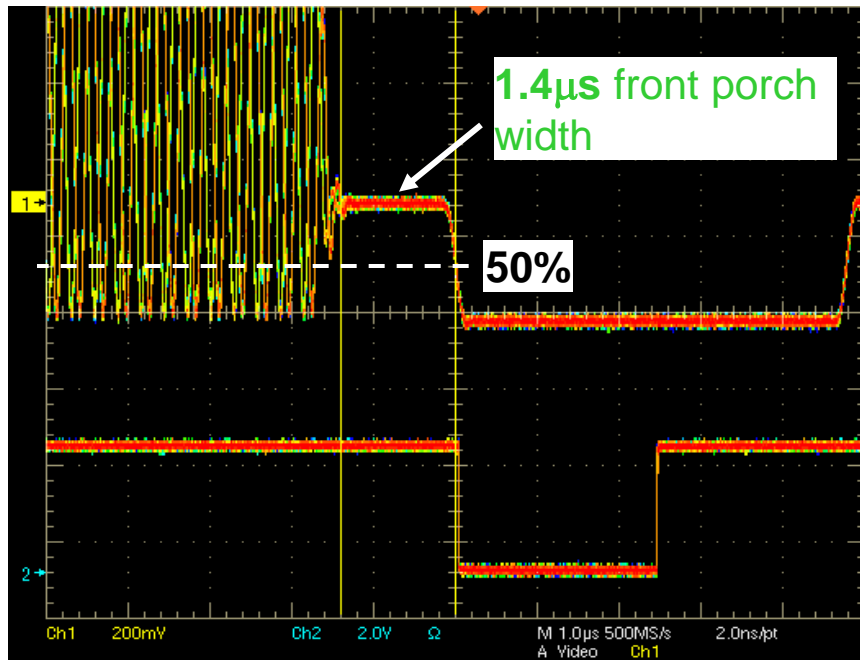
- Use the HSYNC leading edge for the PLL's reference edge
- Use an input low-pass filter to prevent chroma-triggered output glitches for NTSC/PAL
 - Don't exceed 50% sync slice level
- Select a proper input coupling capacitor (C_{in}) value and type
 - E.g. Panasonic ECHU/ECPU series



Glitches on Outputs

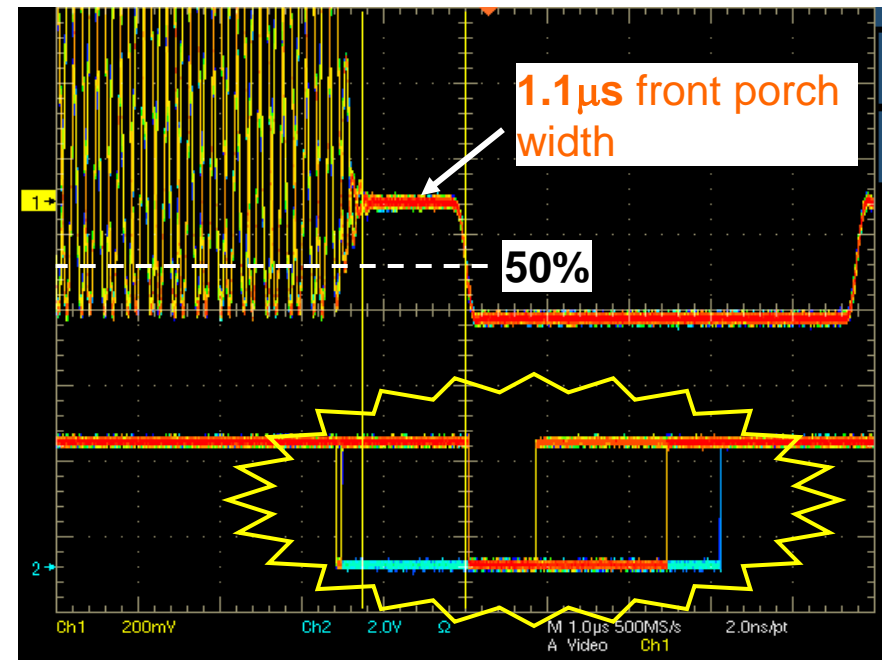
Due to Improper Sync Slicing on Large Chroma Signal

NTSC 100% Red Field



Normal HSync

NTSC 100% Red Field

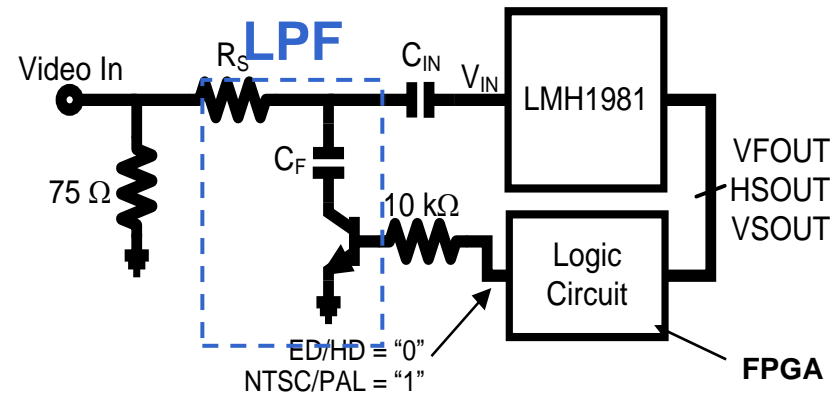


HSync with **Glitches**

Use a low-pass filter to prevent glitches due to large chroma signal near the sync tip.

Chroma Filter

- Attenuates large chroma amplitudes and noise
 - Prevents Output Glitches!
- Switch-controlled LPF
 - For ED/HD video inputs, the transistor turns off to disable the LPF
 - Logic circuit should latch 3rd MSB* of VFOUT data to hold switch state over field
 - Can be implemented in FPGA or discrete logic



Format	VFOUT[3]*	Filter
NTSC/PAL	1 (high)	ON
ED/HD	0 (low)	OFF

Chroma Filter: Component Values

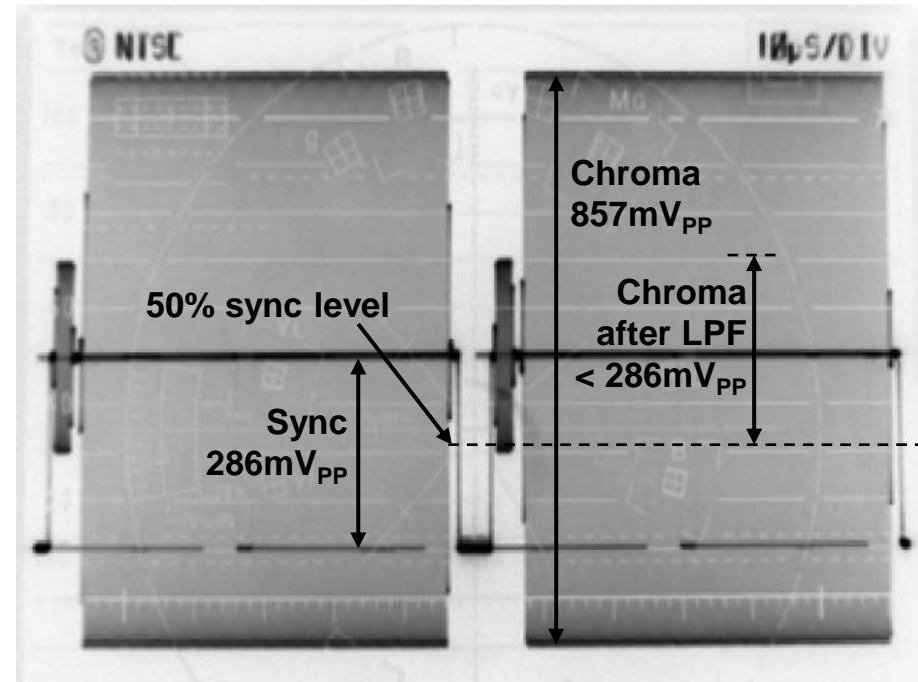
- **Rule of Thumb**: Ensure min. chroma level at V_{IN} (pin 4) is above 50% sync level to prevent glitch.
- R_S & C_F determine filter cutoff frequency (f_{CO})
- f_{CO} depend on chroma attenuation needed:
 - Subcarrier Frequency
 - Chroma Level
 - Chroma Amplitude and Luma Component
- Output prop. delay increases as f_{CO} decreases

Chroma Filter: Design Example

- What values for R_S & C_F ensure no output glitches for this worst-case test signal?
- Need $\text{Chroma}_{PP} < \text{Sync}_{PP}$:
 $A = 20 \log_{10}(286\text{mV} / 857\text{mV})$
 $= -9.6\text{dB} @ f_{SC} = 3.58\text{MHz}$
- RC LPF gain equation:
 $A = 20 \log_{10}[\text{sqrt}(1+(f_{SC}/f_{CO})^2)]^{-1}$
- Solve for f_{CO} :
 $f_{CO} = 1.26 \text{ MHz} = 1 / 2\pi R_S C_F$
- $R_S=240\Omega$ & $C_F=560\text{pF}$ give $f_{CO}=1.18\text{MHz}$, or $-10\text{dB} @ f_{SC}$.

NTSC No Setup ($f_{SC} = 3.58\text{MHz}$)

Chroma Level = 120% (856.8mVp-p)



C_{IN} Value Selection

- Depends on Output Coupling Type of Video Source
- **DC-coupled** video source:
 - Large value (1 – 4.7 uF) will optimize HSync jitter.
 - Smaller values will:
 - Reduce start-up time.
 - Offset video-dependent “jitter” due to Source DAC nonlinearity.
 - Increase rejection of Source AC hum.
- **AC-coupled** source with C_{OUT} ≥ 220uF:
 - Small value (1 – 31 nF) must be used.
 - *Otherwise*, missing sync pulses occur w/ APL changes, ie: alternating W-B fields.