LONTIUM SEMICONDUCTOR CORPORATION

ClearEdge™ Technology

LT9211

MIPI/TTL/2-Port LVDS to MIPI/TTL/2-Port LVDS Converter

Datasheet

1. Features

- **MIPI Transmitter**
  - Compliant with DCS1.02, D-PHY1.2 ,DSI1.2 and CSI-2 1.00
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - Two Port Simultaneous Display Supported
  - Up to 1.8Gb/s per Data Lane
  - Resolution Up to 1920x1200 60Hz or any other Resolution whose Pixel Clk less than 200MHz
  - Data Lane and Polarity Swapping
  - Both Non-Burst and Burst Video Mode Supported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2 Video Format
- **Dual-Port LVDS Transmitter**
  - Compatible with VESA and JEIDA standard
  - 1~2 Configurable Port
  - Two Port Simultaneous Display Supported
  - Resolution Up to 1920x1200 60Hz or any other Resolution whose Pixel Clk less than 200MHz
  - Support DE Mode
  - Data Port , Data Lane and Polarity Swapping
  - Programmable Pre-emphasis
  - Support output SSC(30KHz±5%)
- **TTL Output**
  - Support 24-bit RGB and BT656/BT1120
  - Both DDR and SDR Sampling supported
  - Support both 1.8V and 3.3V Voltage Output
  - Resolution Up to 1920x1200 60Hz or any other Resolution whose Pixel Clk less than 200MHz
- **MIPI Receiver**
  - Compliant with DCS1.02, D-PHY1.2 ,DSI1.2 and CSI-2 1.00
  - 1 Clock Lane and 1~4 Configurable Data Lanes
  - Two Port Input switchable
  - Up to 1.8Gb/s per Data Lane
  - Resolution Up to 1920x1200 60Hz or any other Resolution whose Pixel Clk less than 200MHz
  - Data Lane and Polarity Swapping
  - Both Non-Burst and Burst Video Mode Supported
  - Support RGB666, Loosely RGB666, RGB888, RGB565, 16-bit YCbCr4:2:2, 24-bit YCbCr 4:2:2 Video Format
- **Dual-Port LVDS Receiver**
  - Compatible with VESA and JEIDA standard
  - 1~2 Configurable Port
  - Resolution Up to 1920x1200 60Hz or any other Resolution whose Pixel Clk less than 200MHz
  - Support DE Mode
  - Data Port , Data Lane and Polarity Swapping
  - Internal Rterm Calibration with Less than 5% Error
  - Support input Dessc(30KHz±5%)
- **TTL Input**
  - Support 24-bit RGB and BT656/BT1120
  - Both DDR and SDR Sampling supported
  - Support SYNC Mode and DE Mode
  - Support both 1.8V and 3.3V Input Voltage
  - Resolution Up to 1920x1200 60Hz or any other Resolution whose Pixel Clk less than 200MHz
- **Miscellaneous**
  - 1.8V and 3.3V Power Supply
  - Alternative Input and Output configuration for LVDS/TTL/MIPI
  - MIPI/LVDS muxer and splitter supported
  - MIPI-LVDS level shifter for FPGA Application
  - Support 100KHz and 400KHz I2C Slave
  - External 25MHz ± 200ppm Crystal Reference Clock is Preferred
  - Temperature Range: -40°C ~ +85°C
  - Packaged in QFN64 7.5mm x 7.5mm

2. General Description

The Lontium LT9211 is a high performance convertor which interconvertible between MIPI DSI/CSI-2/Dual-Port LVDS and TTL except for 24bit TTL to 24bit TTL with both SYNC and DE. The LT9211 deserializes input MIPI/LVDS/TTL video data, decodes packets, and converts the formatted video data stream to MIPI/LVDS/TTL transmitter output between AP and mobile display panel or camera.

The LT9211 can be used as 2-Port MIPI/LVDS Repeater which support maximum 14dB input equalization and programmable pre-emphasis to improve performance.

The LT9211 can also be used as MIPI/LVDS Muxer and Splitter. **For MIPI Repeater, Muxer and Splitter, we do not support CSI RAW format.**

The LT9211 is fabricated in advanced CMOS process and implemented in 7.5x7.5mm QFN64 package. This package is RoHS compliant and specified to operate from -40°C to +85°C.

3. Applications

- Mobile systems
- Cellular handsets
- Digital video cameras
- Digital still cameras
- Tablet PC, Notebook PC
- Car Display and Camera System

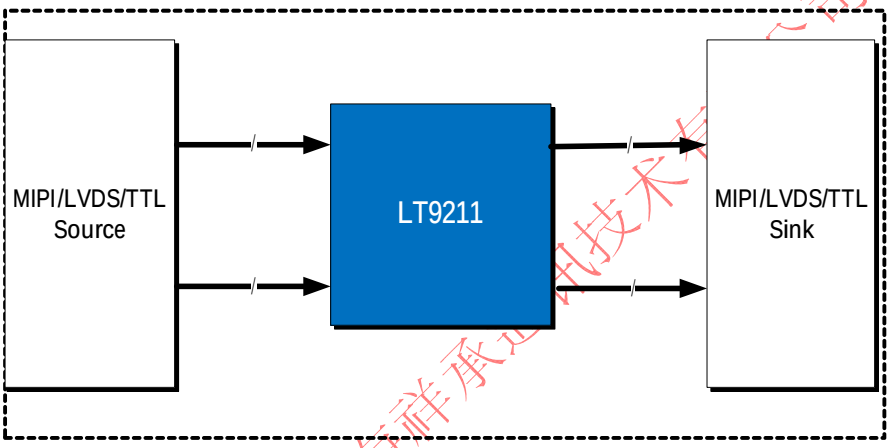

Figure 3.1 LT9211 Typical Application Diagram

4. Ordering Information

Table 4.1 Ordering Information

Part Number	Product Version	Product Status	Operating Temperature Range	Package	Packing Method
LT9211	U2	NRND	-40°C to +85°C	QFN64 (7.5*7.5)	Tray
LT9211	U4	RND	-40°C to +85°C	QFN64 (7.5*7.5)	Tray
NRND: Not Recommended for New Designs. RND: Recommended for New Designs.					

Table 4.2 IC Version Information

Product Version	Information	Note
U2	If the MIPI source does not have “eotp packet”, LT9211’s MIPI Receiver do not work well. Any other conversions between MIPI DSI/CSI-2/Dual-Port LVDS and TTL are OK.	
U4	MIPI Receiver solved the issue which MIPI source does not have “eotp packet”.	

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5. Revision History

Version	Owner	Content	Date
R1.0	Y C	Initial datasheet creation	03/30/2018
R2.0	Y C	Change input and output data format	07/10/2018
R2.1	Y C	Add power consumption	10/09/2018
	N Wang	Update package information	4/13/2019
R2.2	PP J	Update Figure 7.1.1	07/31/2019
R2.3	Y C	Add Power Consumption	08/30/2019
R2.4	Y C	Modify feature description and power consumption	01/16/2020
R2.4a	Y C	Modify Absolute Maximum Conditions Description	04/16/2020
R2.4b	Y C	Delete Pin description about EPAD	05/12/2020
R2.5	Y C	Modify Table4.2 IC Version Information	06/04/2020

6. Pinning Information

6.1 Pin Configuration

To improve signal integrity, all differential pairs should be routed with 100Ω±10% differential impedance a. Maximum trace length mismatch should be less than 2.5mil and keep total trace length to a minimum for all differential traces. It is highly recommended to route differential pairs on top or bottom layer with no vias on signal path.

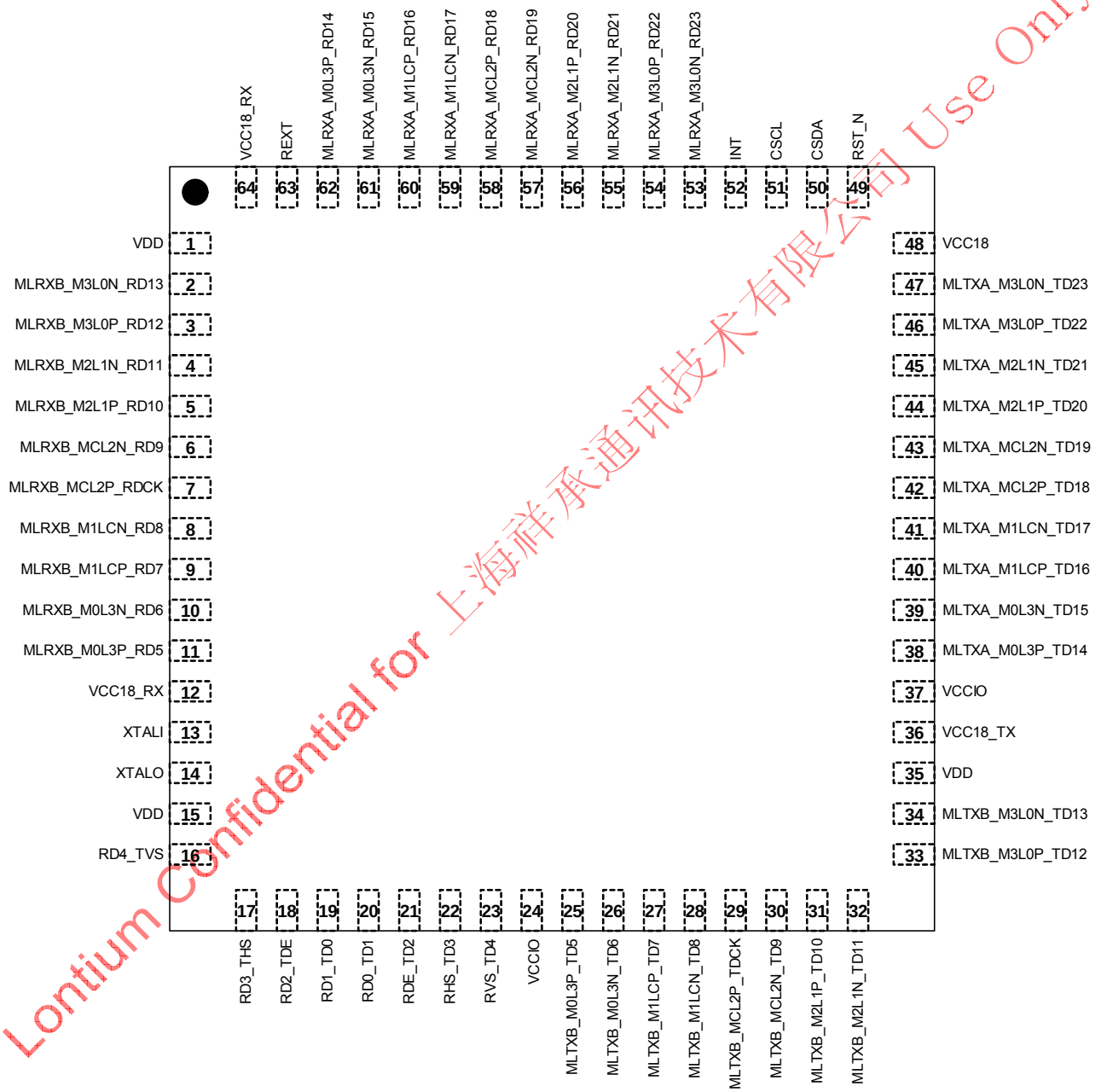


Figure 6.1.1 QFN64 Pin Configuration

To minimize the power supply noise floor, at least one 0.1μF and one 0.01μF decoupling capacitor is recommended to be installed near all the LT9211 1.8V/3.3V power pins. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power input pins must be minimized.

6.2 Pin Description

Table 6.2.1 QFN64 Pin Description

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
53,54	MLRXA_M3L0N_RD23 MLRXA_M3L0P_RD22	MIPI LVDS LVTTL	I	**Port-A MIPIRX Lane-3/LVDSRX Lane-0 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
55,56	MLRXA_M2L1N_RD21 MLRXA_M2L1P_RD20	MIPI LVDS LVTTL	I	**Port-A MIPIRX Lane-2/LVDSRX Lane-1 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
57,58	MLRXA_MCL2N_RD19 MLRXA_MCL2P_RD18	MIPI LVDS LVTTL	I	**Port-A MIPIRX Lane-C/LVDSRX Lane-2 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
59,60	MLRXA_M1LCN_RD17 MLRXA_M1LCP_RD16	MIPI LVDS LVTTL	I	**Port-A MIPIRX Lane-1/LVDSRX Lane-C and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
61,62	MLRXA_M0L3N_RD15 MLRXA_M0L3P_RD14	MIPI LVDS LVTTL	I	**Port-A MIPIRX Lane-0/LVDSRX Lane-3 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
2,3	MLRXB_M3L0N_RD13 MLRXB_M3L0P_RD12	MIPI LVDS LVTTL	I	**Port-B MIPIRX Lane-3/LVDSRX Lane-0 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
4,5	MLRXB_M2L1N_RD11 MLRXB_M2L1P_RD10	MIPI LVDS LVTTL	I	**Port-B MIPIRX Lane-2/LVDSRX Lane-1 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
6,7	MLRXB_MCL2N_RD9 MLRXB_MCL2P_RDCK	MIPI LVDS LVTTL	I	**Port-B MIPIRX Lane-C/LVDSRX Lane-2 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
8,9	MLRXB_M1LCN_RD8	MIPI	I	**Port-B MIPIRX Lane-1/LVDSRX Lane-C and TTL Input**

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
	MLRXB_M1LCP_RD7	LVDS LVTTL		MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
10,11	MLRXB_M0L3N_RD6 MLRXB_M0L3P_RD5	MIPI LVDS LVTTL	I	**Port-B MIPIRX Lane-0/LVDSRX Lane-3 and TTL Input** MIPI input of polarity swappable differential pairs up to 1.8Gb/s ; LVDS input of polarity swappable differential pairs up to 1.2Gb/s ; TTL input up to 200Mbps.
16,17 18,19 20,21 22,23	RD4_TVS,RD3_THS RD2_TDE,RD1_TD0 RD0_TD1,RDE_TD2 RHS_TD3,RVS_TD4	LVTTL	I/O	**TTL Data and Control Signal and Debug GPO Output** These Pins can be selected as TTL input or output. Also, they can be configured as outputs for debug function.
38,39	MLTXA_M0L3P_TD14 MLTXA_M0L3N_TD15	MIPI LVDS LVTTL	O	**Port-A MIPITX Lane-0/LVDSTX Lane-3 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
40,41	MLTXA_M1LCP_TD16 MLTXA_M1LCN_TD17	MIPI LVDS LVTTL	O	**Port-A MIPITX Lane-1/LVDSTX Lane-C and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
42,43	MLTXA_MCL2P_TD18 MLTXA_MCL2N_TD19	MIPI LVDS LVTTL	O	**Port-A MIPITX Lane-C/LVDSTX Lane-2 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
44,45	MLTXA_M2L1P_TD20 MLTXA_M2L1N_TD21	MIPI LVDS LVTTL	O	**Port-A MIPITX Lane-2/LVDSTX Lane-1 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
46,47	MLTXA_M3L0P_TD22 MLTXA_M3L0N_TD23	MIPI LVDS LVTTL	O	**Port-A MIPITX Lane-3/LVDSTX Lane-0 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
25,26	MLTXB_M0L3P_TD5 MLTXB_M0L3N_TD6	MIPI LVDS LVTTL	O	**Port-B MIPITX Lane-0/LVDSTX Lane-3 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
27,28	MLTXB_M1LCP_TD7 MLTXB_M1LCN_TD8	MIPI LVDS	O	**Port-B MIPITX Lane-1/LVDSTX Lane-C and TTL Output** MIPI output of polarity swappable differential pairs up to

PIN#	PIN NAME	I/O TYPE	I/O DIR	DESCRIPTION
		LVTTL		1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
29,30	MLTXB_MCL2P_TDCK MLTXB_MCL2N_TD9	MIPI LVDS LVTTL	O	**Port-B MIPITX Lane-C/LVDSTX Lane-2 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
31,32	MLTXB_M2L1P_TD10 MLTXB_M2L1N_TD11	MIPI LVDS LVTTL	O	**Port-B MIPITX Lane-2/LVDSTX Lane-1 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
33,34	MLTXB_M3L0P_TD12 MLTXB_M3L0N_TD13	MIPI LVDS LVTTL	O	**Port-B MIPITX Lane-3/LVDSTX Lane-0 and TTL Output** MIPI output of polarity swappable differential pairs up to 1.8Gb/s ; LVDS output of polarity swappable differential pairs up to 1.2Gb/s ; TTL output up to 200Mbps.
63	REXT	Analog	I/O	**BandGap External Resistor** External 6.04K (1%) resistor tie to ground for setting internal reference current.
13,14	XTALI XTALO	LVTTL	I/O	**25M Crystal oscillator interface** A 25MHz±200ppm Crystal is Preferred.
49	RST_N	LVTTL	I	**Hardware Reset Input** Chip reset signal, active low, both 1.8V and 3.3V voltage level should be OK.
50,51	CSDA CSCL	LVTTL OPD	I/O	**I2C Serial Clk and Data Input and Output** It serves as 3.3V or 1.8V serial port clk and data IO slave for register access. The I2C device address is 0x5A.
52	INT	LVTTL OPD	I/O	**Interrupt Request Output** This pin is interrupt request output. It can be configured as Open-drain or CMOS output, when configured as CMOS output, the output high voltage is 1.8V.
12,64	VCC18_RX	PWR	I/O	**1.8V RX Power** 1.8V power for RX.
36	VCC18_TX	PWR	I/O	**1.8V TX Power** 1.8V power for TX.
24,37	VCCIO	PWR	I/O	**IO Power** 1.8V or 3.3V power for TTL input and output. When 3.3V TTL voltage level input, it should be connect to 3.3V. For TTL output, the output high-voltage is VCCIO.
48	VCC18	PWR	I/O	**1.8V Power for Control Signal** 1.8V power for control signal.
1,15,35	VDD	PWR	I/O	**1.8V Power** 1.8V power for digital block.

7. Function Description

7.1 Function Block Diagram

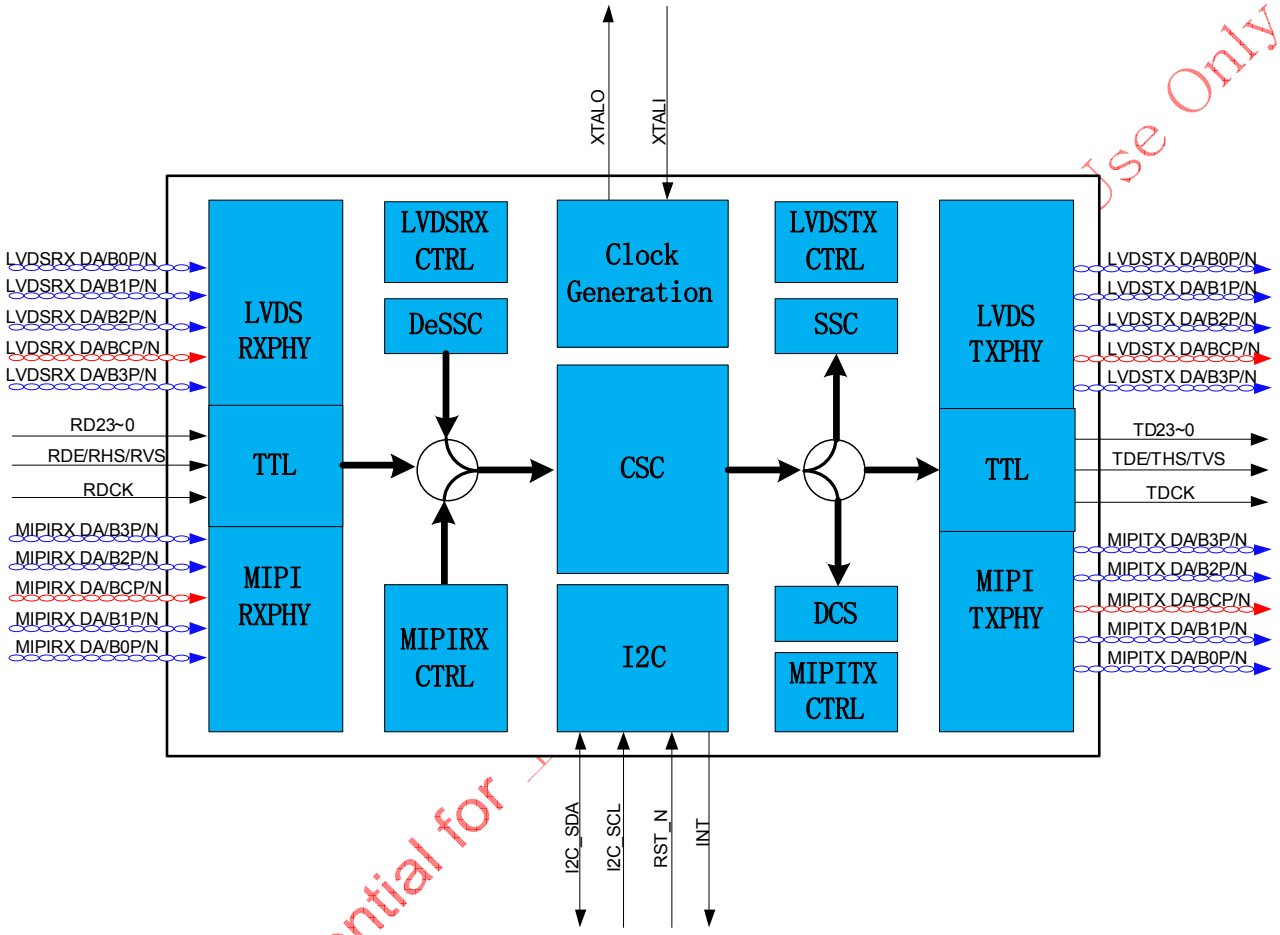


Figure 7.1.1 Function Block Diagram

8. Specification

8.1 Absolute Maximum Conditions

Table 8.1.1 Absolute Maximum Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VCC18,VDD	1.8V Power Supply Voltage	-0.3		2.4	V
VCCIO	1.8V/3.3V Power Supply Voltage	-0.3		4	V
V_I/ V_O	CMOS Terminal Input/output Voltage Range	-0.3		VCCIO+ 0.3	V
T_S	Storage Temperature	-65		150	℃
T_J	Junction Temperature			125	℃
ESD	HBM Electrostatic Discharge Level		2K		V
Notes: Permanent device damage may occur if absolute maximum conditions are exceeded.					

8.2 Normal Operating Conditions

Table 8.2.1 Normal Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	Unit
VCC18_RX, VCC18_TX VCC18,VDD	1.8V Power Supply Voltage	1.62	1.8	1.98	V
VCCIO	1.8V Power Supply Voltage	1.62		1.98	V
	3.3V Power Supply Voltage	2.97		3.63	V
T_A	Operating Free-air Temperature	-40	27	85	℃
θ_{JC}	Junction to Case Thermal Resistance		15		℃/W

8.3 DC Characteristics

Table 8.3.1 DC Characteristics

MIPI HS Line Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIDTH	Differential input high voltage threshold			70	mV
VIDTL	Differential input low voltage threshold	-70			mV
VIHHS	Single ended input high voltage			460	mV
VILHS	Single ended input low voltage	-40			mV
VCMRXDC	Input common mode voltage	70	200	330	mV
Rterm	Differential input impedance	80	100	125	Ω
MIPI LP Line Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIL	Input low voltage			550	mV
VIH	Input high voltage, data rate<1.5Gbps	880			mV
	Input high voltage, data rate>1.5Gbps	740			mV
VHYST	Input hysteresis	25			mV
MIPI HS Line Transmitter DC Specifications					

Symbol	Parameter	MIN	TYP	MAX	Unit
Vcm	HS Transmit Static Common mode Voltage	150	200	250	mV
Vod	HS Transmit Differential Voltage	140	200	270	mV
Vohhs	HS Transmit Output High Voltage			360	mV
Zos	Single ended output impedance	40	50	62.5	Ω
MIPI LP Line Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VOL	Output low-level SE voltage	-50	0	50	mV
VOH	Output high-level SE voltage	1.1	1.2	1.3	V
ZOLP	Single-ended output impedance	110			Ω
LVDS Receiver DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VIDTH	Differential input high voltage threshold			50	mV
VIDTL	Differential input low voltage threshold	-50			mV
VCMRXDC	Input common mode voltage	0	1200	1800	mV
Rterm	Termination Resister	80	100	125	Ω
LVDS Transmitter DC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
VOD	Differential Out Voltage: RL=100Ω	150	350	500	mV
VOC	Common Mode Voltage: RL=100Ω	1.1	1.25	1.4	V
IOS	Output Short Circuit Current : Vout=0V, RL=100Ω			-24	mA
LVTTL I/O DC Specifications					
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**
VIH	Input high voltage	1.2			V
VIL	Input low voltage			0.6	V
VOH	1.8V Output high voltage	1.3			V
	3.3V Output high voltage	2.4			
VOL	1.8V Output low voltage			0.4	V
	3.3V Output low voltage			0.4	

8.4 AC Characteristics

Table 8.4.1 AC Characteristics

MIPI HS Line Receiver AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
ΔVCMRX(HF)	Common mode interference beyond 450MHz			200	mVpp
ΔVCMRX(LF)	Common mode interference between 50MHz and 450MHz	-50		50	mVpp
Ccm	Common mode termination			60	pF
MIPI LP Line Receiver AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
eSPIKE	Input pulse rejection			300	V.ps
TMIN	Minimum pulse response	20			ns
VINT	Peak interference voltage			200	mV
fINT	Interference frequency	450			MHz
MIPI HS Line Transmitter AC Specifications					

Symbol	Parameter	MIN	TYP	MAX	Unit
Δ Vcmtx(hf)	Common mode Voltage variation above 450MHz			15	mVrms
Δ Vcmtx(lf)	Common mode Voltage variation between 50-450MHz			25	mVpeak
Rise/Fall Time 20%-80%	Data rate <1Gbps	150		0.3UI	ps
	Data rate 1Gbps~1.5Gbps	100		0.35UI	ps
	Data rate >1.5Gbps	50		0.4UI	ps
MIPI LP Line Transmitter AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
trlp , tflp	Single ended output rise/fall time, 15% to 85%, CL< 70pF			25	ns
treot	Single ended output rise/fall time, 30% to 85%, CL< 70pF			35	ns
LVDS Receiver AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
Tc	output clk cycle	6.25		37	ns
T0	Input data position0	-0.15	0	0.15	ns
T1	Input data position1	Tc/7-0.15		Tc/7+0.15	ns
T2	Input data position2	2Tc/7-0.15		2Tc/7+0.15	ns
T3	Input data position3	3Tc/7-0.15		3Tc/7+0.15	ns
T4	Input data position4	4Tc/7-0.15		4Tc/7+0.15	ns
T5	Input data position5	5Tc/7-0.15		5Tc/7+0.15	ns
T6	Input data position6	6Tc/7-0.15		6Tc/7+0.15	ns
LVDS Transmitter AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
Tc	output clk cycle	6.25		37	ns
trise	VOD rise time, 20% to 80%	250	350	500	ps
tfall	VOD fall time, 20% to 80%	250	350	500	ps
T0	Output data position0	-0.15	0	0.15	ns
T1	Output data position1	Tc/7-0.15		Tc/7+0.15	ns
T2	Output data position2	2Tc/7-0.15		2Tc/7+0.15	ns
T3	Output data position3	3Tc/7-0.15		3Tc/7+0.15	ns
T4	Output data position4	4Tc/7-0.15		4Tc/7+0.15	ns
T5	Output data position5	5Tc/7-0.15		5Tc/7+0.15	ns
T6	Output data position6	6Tc/7-0.15		6Tc/7+0.15	ns
TTL Input AC Timing Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
T_{CIP}	SDR Mode DCK Period, one pixel per clock	5		40	ns
F_{CIP}	SDR Mode DCK Frequency, one pixel per clock	25		200	MHz
T_{CIP_DDR}	DDR Mode DCK Period, dual-edge clock	10		40	ps
F_{CIP_DDR}	DDR Mode DCK Frequency, dual-edge clock	25		100	MHz
T_{JITTER}	DCK TIE jitter @1.5M			0.02	T_{CIP}
T_{DUTY}	SDR Mode DCK Duty Cycle	40%		60%	
T_{DUTY_DDR}	DDR Mode DCK Duty Cycle	45%		55%	
T_{SDF}	Setup Time to DCK falling edge in SDR mode	1.2			ns
T_{HDF}	Hold Time to DCK falling edge in SDR mode	1.2			ns
T_{SDR}	Setup Time to DCK rising edge in SDR mode	1.1			ns
T_{HDR}	Hold Time to DCK rising edge in SDR mode	1.1			ns
T_{SDD}	Setup Time to DCK edge in DDR mode	1.1			ns

T_{HDD}	Hold Time to DCK edge in DDR mode	1.2			ns
TTL Output AC Timing Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
T_{CIP}	SDR Mode DCK Period, one pixel per clock	5		40	ns
F_{CIP}	SDR Mode DCK Frequency, one pixel per clock	25		200	MHz
T_{CIP_DDR}	DDR Mode DCK Period, dual-edge clock	10		40	ps
F_{CIP_DDR}	DDR Mode DCK Frequency, dual-edge clock	25		100	MHz
T_{DUTY}	SDR Mode DCK Duty Cycle	40%		60%	
T_{DUTY_DDR}	DDR Mode DCK Duty Cycle	45%		55%	
Configuration I2C AC Specifications					
Symbol	**Parameter**	**MIN**	**TYP**	**MAX**	**Unit**
f_{SCL}	I2C clock frequency		100	400	kHz
t_f	Fall time of both SDA and SCL signals			300	ns
t_r	Rise time of both SDA and SCL signals			300	ns
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	Low period of SCL clock	1.3			µs
t_{HIGH}	High period of SCL clock	0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD;DAT}$	Data hold time	0.3			µs
$t_{SU;DAT}$	Data setup time	250			ns
$t_{SU;STO}$	Setup time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs

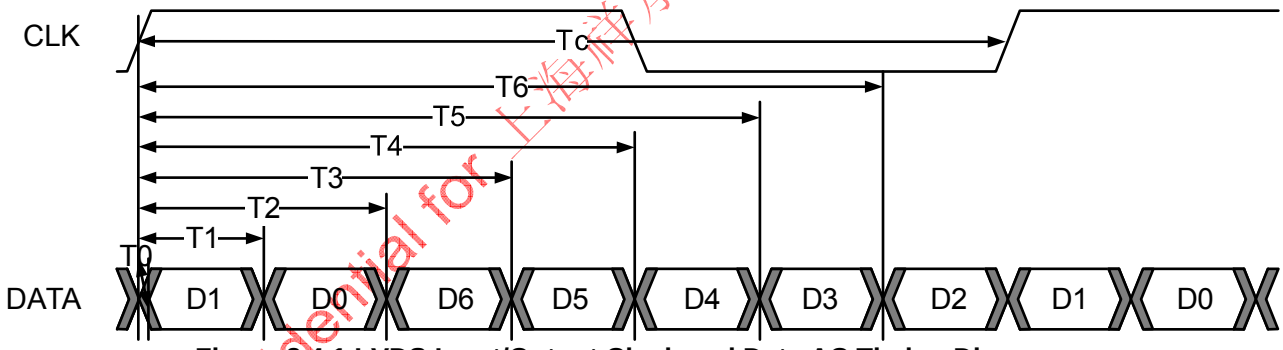


Figure 8.4.1 LVDS Input/Output Clock and Data AC Timing Diagram

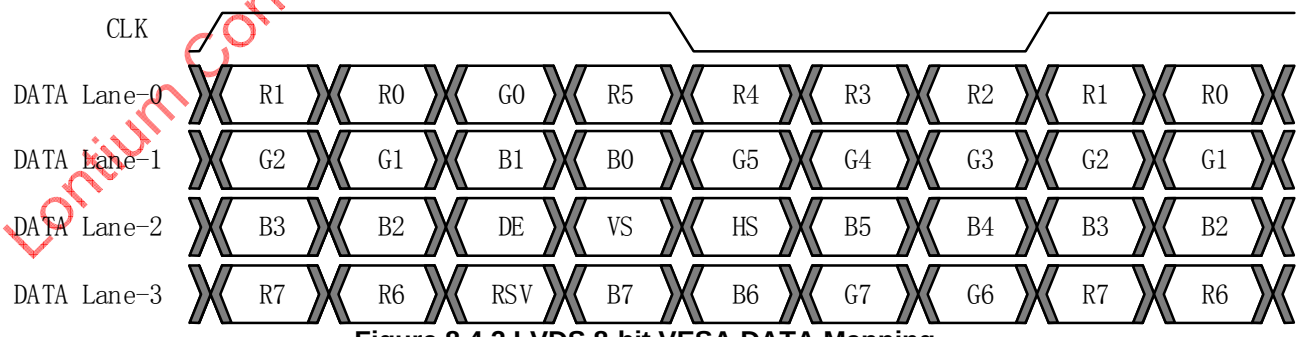


Figure 8.4.2 LVDS 8-bit VESA DATA Mapping

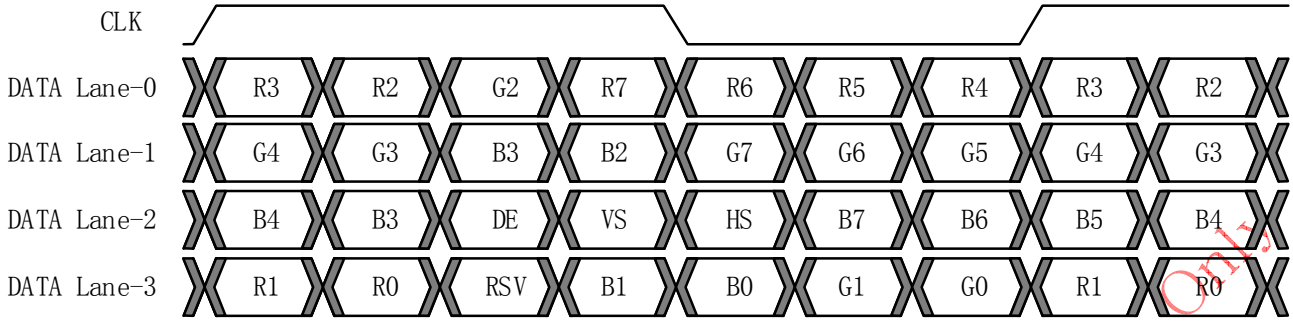


Figure 8.4.3 LVDS 8-bit JIEDA DATA Mapping

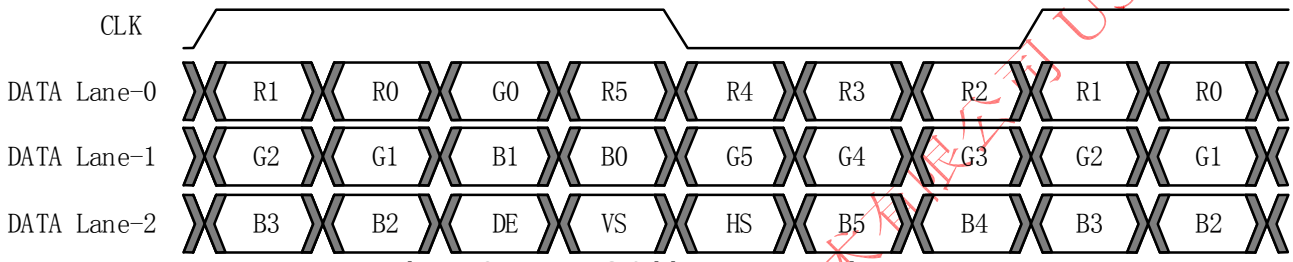


Figure 8.4.4 LVDS 6-bit DATA Mapping

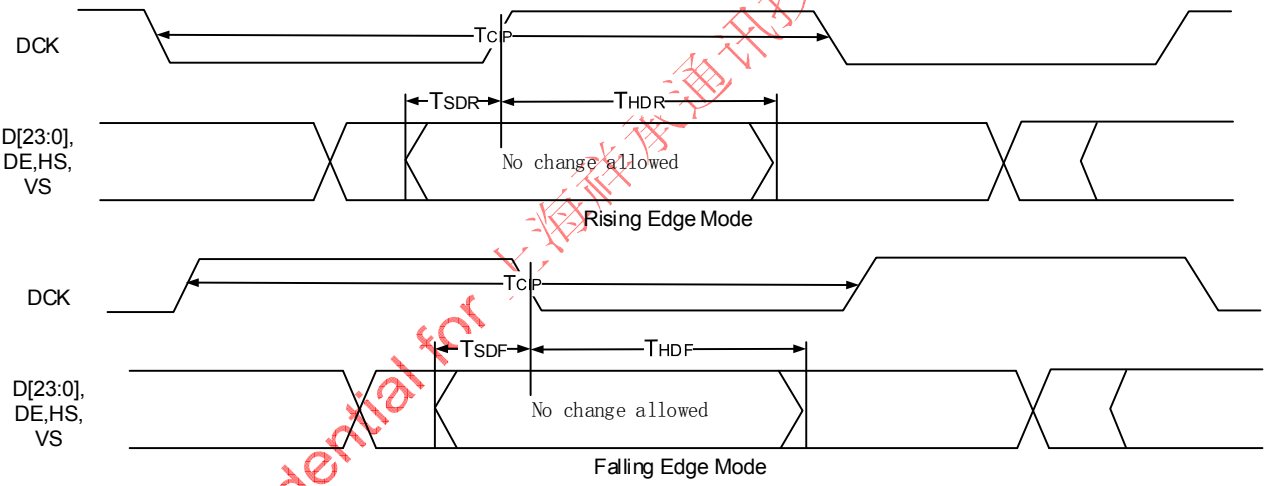


Figure 8.4.5 TTL SDR Mode Data and Clock Timing Diagram6

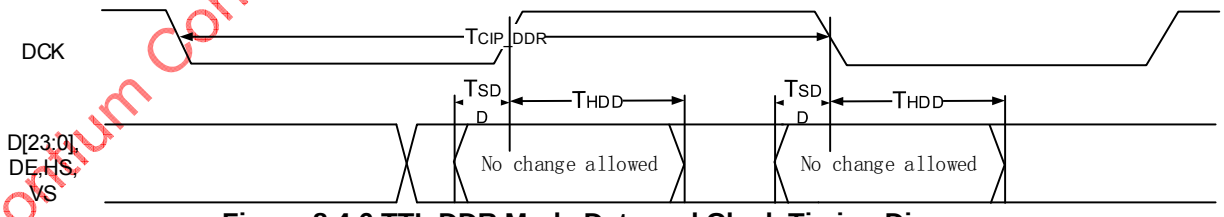


Figure 8.4.6 TTL DDR Mode Data and Clock Timing Diagram

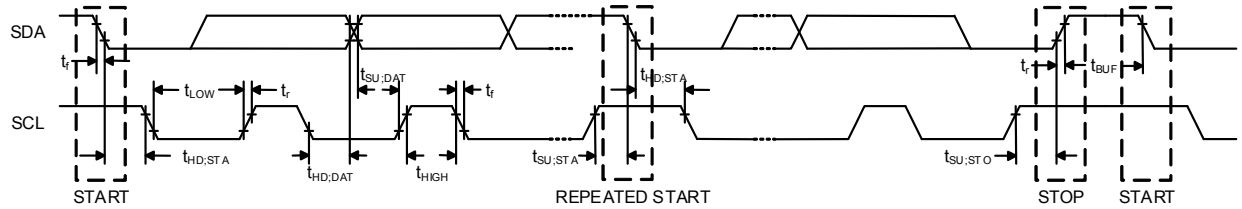


Figure 8.4.7 Configuration I2C Timing Diagram

8.5 Power Consumption

Table 8.5.1 MIPI to LVDS Power Consumption

Symbol	Condition	Min	Typ	Max	Unit
I_{VCC18}	MIPI to 2-Port LVDS @1080P 60Hz		231	252	mA
I_{VCCIO}			1	1	mA

Table 8.5.2 MIPI to TTL Power Consumption

Symbol	Condition	Min	Typ	Max	Unit
I_{VCC18}	MIPI to BT1120 @1080P 60Hz		155	171	mA
I_{VCCIO}=3.3V			16	17	mA
I_{VCCIO}=1.8V			7	8	

Table 8.5.3 MIPI Splitter Power Consumption

Symbol	Condition	Min	Typ	Max	Unit
I_{VCC18}	MIPI Splitter @ 1080P 60Hz		255	281	mA
I_{VCCIO}			1	1	mA

Table 8.5.4 LVDS Splitter Power Consumption

Symbol	Condition	Min	Typ	Max	Unit
I_{VCC18}	LVDS Splitter @ 1080P 60Hz		238	264	mA
I_{VCCIO}			1	1	mA

Table 8.5.5 LVDS to TTL Power Consumption

Symbol	Condition	Min	Typ	Max	Unit
I_{VCC18}	2-Port LVDS to BT1120 @1080P 60Hz		175	194	mA
I_{VCCIO}=3.3V			17	20	mA
I_{VCCIO}=1.8V			8	9	

Table 8.5.6 LVDS to MIPI Power Consumption

Symbol	Condition	Min	Typ	Max	Unit
I_{VCC18}	2-Port LVDS to MIPI @1080P 60Hz		242	267	mA
I_{VCCIO}			1	1	mA
I_{VCC18}	2-Port LVDS to MIPI w/ two Port Simultaneous Display @1080P 60Hz		272	299	mA

IVCCIO			1	1	mA

Table 8.5.7 TTL to MIPI Power Consumption

Symbol	Condition	Min	Typ	Max	Unit
IVCC18	BT1120 to MIPI @1080P 60Hz w/ Two Port Simultaneous Display		229	252	mA
IVCCIO=3.3V			1	1	mA
IVCCIO=1.8V			1	1	mA
IVCC18	BT1120 to Single Port MIPI @1080P 60Hz		199	219	mA
IVCCIO=3.3V			1	1	mA
IVCCIO=1.8V			1	1	mA

Table 8.5.8 TTL to LVDS Power Consumption

Symbol	Condition	Min	Typ	Max	Unit
IVCC18	BT1120 to 2-Port LVDS @1080P 60Hz		201	221	mA
IVCCIO=3.3V			1	1	mA
IVCCIO=1.8V			1	1	

Note: The Typical value is measured at room temperature and VCC18=1.8V, the Maximum value is measured at 80℃ and VCC18=1.98V.

8.6 Power-up and Reset Sequence

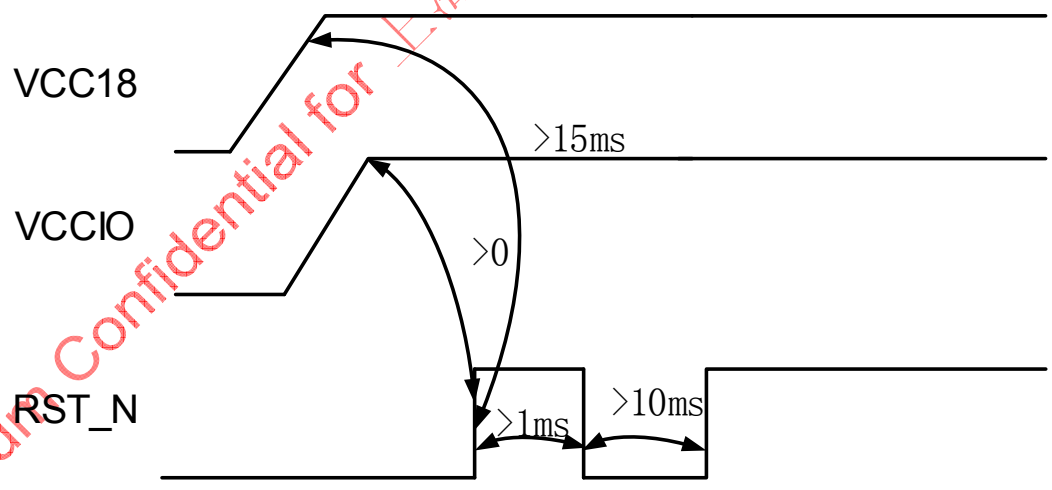


Figure 8.6.1 Power-up Sequence

9. Package Information

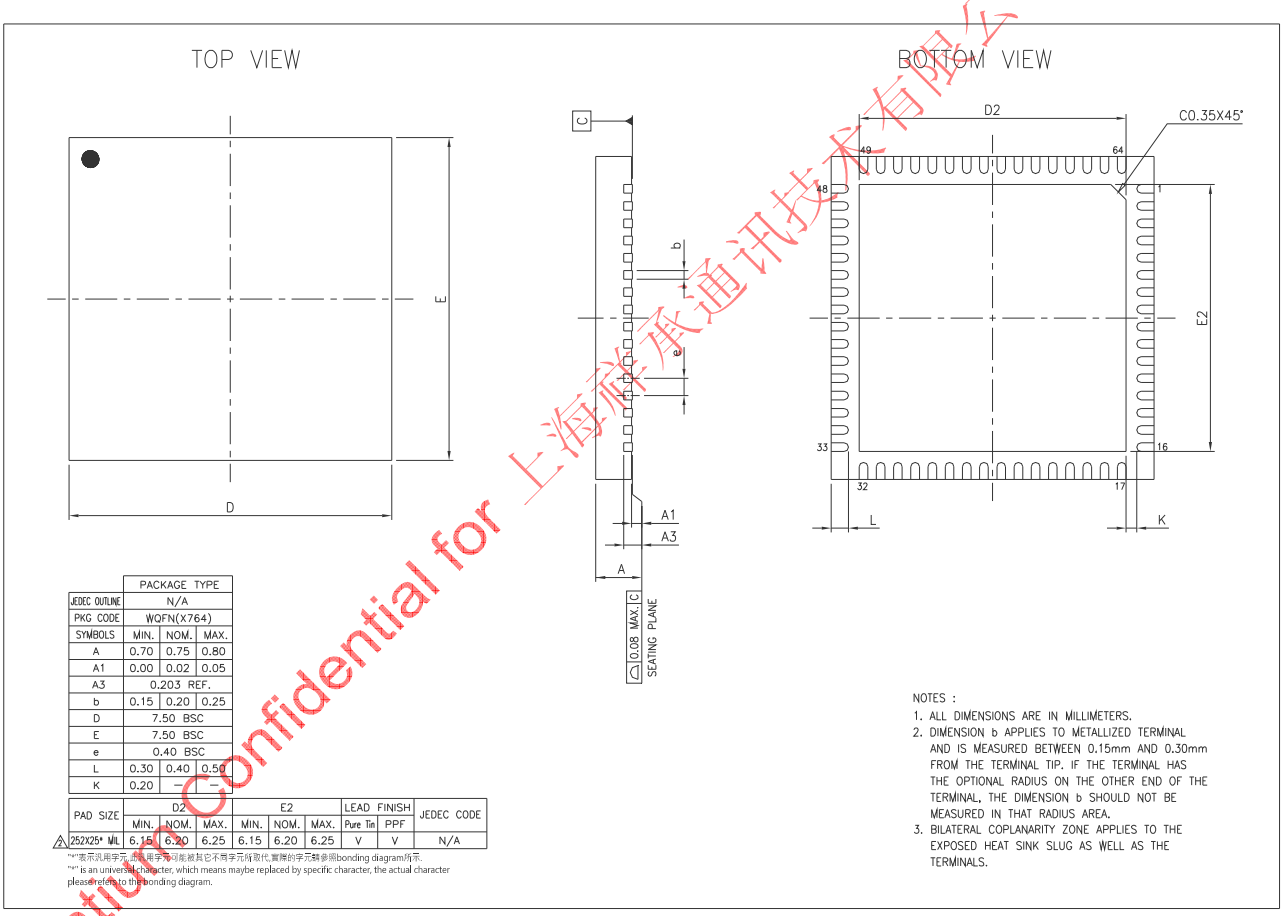
9.1 ePad Enhancement

The LT9211 is packaged in QFN64 package with ePad.

The ePad needs to be soldered to the PCB. The information in the following paragraphs is provided for applications which solder the ePad to the PCB.

The ePad must not be electrically connected to any other voltage level except ground (GND). A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts.

9.2 Package Dimensions



	PACKAGE TYPE		
JEDEC OUTLINE	N/A		
PKG CODE	WQFN(X764)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	7.50 BSC		
E	7.50 BSC		
e	0.40 BSC		
L	0.30	0.40	0.50
K	0.20	—	—

PAD SIZE	D2			E2			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
⚠252X25* MIL	6.15	6.20	6.25	6.15	6.20	6.25	V	V	N/A

"*"表示通用字元，此通用字元可能被其它不同字元所取代實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Figure 9.2.1 QFN64 Package Dimensions

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