

FLG 1



FLG2

FIG. 1 is the schematic diagram of the connection between the TI chip DS92LV1021A and DS92LV1212A at present. Through the use of fpga to send and receive data, figure 2 is the inter-plate signal connection diagram, and several problems encountered during the development process are as follows:

1. Local (unit) send 10 bit parallel data to DS92LF1021A FPGA, converted to a serial signal to the other board (the host), the motherboard through DS92LV1212A serial signal into 10 bit parallel data to the FPGA, the link test no problem.

2. The local (unit) transmits the serial signal of the other board (host) to 10bit parallel signal through DS92LV1212A, and the parallel signal is input to the local FPGA, and the data is found to be in error.