

AN-1194 Failsafe Biasing of LVDS Interfaces

ABSTRACT

Failsafe biasing of a data line receiver sets a known state under certain line conditions. There are multiple situations where this may be required depending upon the specific application. The LVDS line has three possible states. Two are the active states where the LVDS line driver is either in the logic HIGH state or logic LOW state. The third state is the un-driven state. This could occur if:

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1 INTRODUCTION

Failsafe biasing of a data line receiver sets a known state under certain line conditions. There are multiple situations where this may be required depending upon the specific application. The LVDS line has three possible states. Two are the active states where the LVDS line driver is either in the logic HIGH state or logic LOW state. The third state is the un-driven state. This could occur if:

1. The LVDS driver is in TRI-STATE
2. The LVDS driver is powered-off ($V_{CC} = 0V$ or open)
3. The LVDS driver is disconnected from the line (unplugged)

There are other conditions where failsafe biasing of the LVDS receiver may be desired, these include:

1. The LVDS receiver is disconnected from the line (inputs may be open or terminated)
2. The LVDS receiver was multiple channels and not all are required by the application

There are also several line fault conditions that may require failsafe biasing:

1. The LVDS pair is open-circuited
2. The LVDS pair is shorted together

From the variety of this list of failsafe conditions shown above, the true application dependency of failsafe biasing can be seen. Also, most applications expect a HIGH receiver output under failsafe conditions. This is typically the case supported, however it should be noted that some applications may require a LOW state.

Failsafe biasing of LVDS receivers is vendor and device specific. The respective LVDS receiver datasheets should be reviewed to determine if and what type of failsafe support is provided by the specific circuit. Also some implementations of failsafe biasing may not be compatible with others.

National has basically two types of LVDS receivers currently available. One provides failsafe support, while the other does not. The advantages and disadvantages of each are discussed next.

High-Speed Line Receiver—some of National's very high-speed LVDS receivers do not provide internal (on-chip) failsafe biasing. Failsafe biasing causes minor AC distortion at high rates (above 800 Mbps). For these applications it has been removed to eliminate the impact to skew and jitter. Also with serialized data streams with embedded clocks, the deserializer chip tends to provide a lock status output. When the link is inactive, the deserializer detects the missing clocks and flags this bus condition.

National's standard speed LVDS Receivers tend to provide internal failsafe biasing for open input conditions, terminated conditions, and in most cases shorted ($V_{ID} = 0V$) conditions. Please refer to the respective datasheets to determine which conditions are supported.

Thresholds

The LVDS Standard (ANSI/TIA/EIA-644-A) specifies a maximum threshold of 100 mV for the receiver. This is shown in the Voltage Transfer Curve (VTC) in [Figure 1](#). The typical National LVDS receiver switches at about -30 mV. Note that with $V_{ID} = 0V$, the output will be in a HIGH state. With an external failsafe bias of $+25$ mV applied, the typical differential noise margin is now the difference from the switch point to the bias point. In the example below, this would be 55 mV of Differential Noise Margin ($+25$ mV $-$ -30 mV). If more DNM is required, then a stronger failsafe bias point can be set by simply changing resistor values.

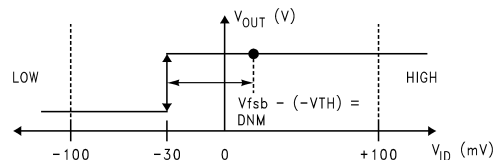


Figure 1. VTC Curve of a National Standard Speed LVDS Receiver

Open input failsafe is the most secure and commonly required failsafe support. If a multi-channel receiver is being used and not all channels are required, then it is best to leave the unused channel's inputs open. Internal biasing networks pull the plus input towards 2.5V and the minus input towards ground with high value impedance. This bias insures that the unused channel does not pick up noise and falsely switch needlessly increasing power dissipation. This same support is also valuable in multidrop applications where a node may be disconnected from the line. When this occurs, the inputs are open and if the part is powered up, the output will be a HIGH state.

Terminated failsafe is for the case of a receiver that has a 100Ω termination across its inputs. This state can occur under a few situations: the terminated receiver may be unplugged from the bus, or the driver may be TRI-STATED, powered-off or removed. In the second case, the cable may still be present and floating. If it picks up "differential" coupled noise, the receiver may respond. Recall that a receiver is designed to detect very small amplitude and width signals and recover them to standard logic levels. This is the reason that twisted pair cables tend to be recommended, as they help to ensure that noise is coupled common to both lines and rejected by the receivers (not coupled as differential noise). Shielding is also recommended in applications where coupled noise levels are high. Terminated failsafe in most cases is not designed to operate over the full common-mode range. If this case is required, National recommends the use of external biasing resistors that provide a small bias to set the differential input voltage while the line is un-driven. The resistors also set a common-mode point, which is equal to the typical offset (V_{OS}) of the driver. Under nominal conditions the common-mode voltage of the line is held constant and does not modulate between active data states and un-driven states. A modulation of common-mode voltage creates "even" mode current in the line which in turn generates noise and unwanted EMI. See [Figure 2](#).

Other vendors have implemented failsafe with different approaches. Again, these have some features and also limitations. One approach pulled both lines to V_{CC} with internal pull up resistors. National does not support this approach due to the common-mode modulation between active and un-driven states. The driver biases the line to +1.25V nominal, but when the line is un-driven, it gets pulled to 3.3V common mode. This large 2V transition from +1.25 to +3.3 is a common-mode modulation and is undesirable. Also depending upon the driver being used and the total number of receivers on the line, the first active data bit that a driver sends out may be distorted while the driver pulls down the common-mode voltage. Other reported problems with this include incompatibility with other receivers and forward biasing of external ESD protection diodes if they are powered from an isolated supply. Recently this vendor introduced a new approach to failsafe biasing to resolve and enhance the failsafe feature. This new approach resolves some issues but causes others. The new approach uses a window detector to detect the un-driven line. If the line is un-driven for 600 ns (1 μs maximum per datasheet), the output is switched to a failsafe HIGH state. The limitation is that during the "failsafe" state, a very limited differential noise margin is provided. The data line receiver has 50 mV (typical) of hysteresis (no minimum specified), thus if the line has 50 mV of differential noise, the data line receiver does its job and recovers the signal resetting the failsafe logic. This is noted in reference #2 (page 6). While it is a unique solution, the differential noise margin remains limited to only 50 mV typical during "failsafe". Also, it is possible for the line to be driven HIGH, and then switch to a LOW state (for example with -60 mV V_{ID}), in this case the receiver output will switch LOW, then 600 ns later switch to the failsafe HIGH state. The slow time delay of 1 μs may not be acceptable for all applications.

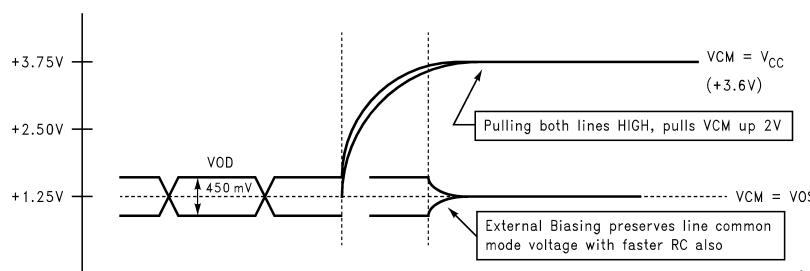


Figure 2. Single-Ended Waveforms Showing Common Mode Voltage between Driven and Un-Driven States vs Failsafe Implementation

National recommends external failsafe biasing on its first and second generation LVDS receivers for a number of system level and signal quality reasons. First, only an application that requires failsafe biasing needs to employ it. Second, the amount of failsafe biasing is now an application design parameter and can be custom tailored for the specific application. In applications in low noise environments, they may choose to use a very small bias if any. For applications with less balanced interconnects and/or in high noise environments, they may choose to boost failsafe further. National's "LVDS Owner's Manual (REF #1)" provides detailed calculations for selecting the proper failsafe biasing resistors. Third, the common-mode voltage is biased by the resistors during the un-driven state. This is selected to be close to the nominal driver offset voltage (V_{OS}). Thus when switching between driven and un-driven states, the common-mode modulation on the bus is held to a minimum. The external low value (a few k Ω typical) resistors R1 and R3 provide a low impedance path from the line to power/ground. This has multiple benefits: it provides a common-mode return path, it provides a shunt path for ESD and EOS events making the already rugged parts even more robust, and it also makes coupled noise lower in magnitude. For example, if a 25 mV failsafe bias point is required (V_{fsb}), first determine the amount of bias current. 25 mV/100 Ω is 250 μ A. The bias current should be at least an order of magnitude smaller than the 3 mA loop current. Next determine the total resistance from the bias supply to ground \rightarrow 3.3V/250 μ A = 13 k Ω . Since R_T is 100 Ω it can be ignored. Next determine the ratio of R3 to R1. This is 1.25V/3.3V = 0.378. Next calculate R3 as 0.378 of 13 k Ω and round down to a standard value (4.99 k Ω). R1 is equal to 13 k Ω - R3 = 8 k Ω . This network will provide a bias of +25 mV to the receiver. The R_T (R_2) resistor should be located as close to the receiver as possible to minimize the stub length. The location of R1 and R3 is less important.

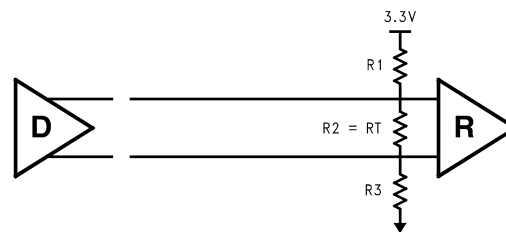


Figure 3. External Failsafe Biasing of an LVDS Link

Noise Margins—driven (active) and un-driven bus states

When the bus is active an LVDS driver's output voltage is between 250 mV and 450 mV. The receiver's worst case threshold per the LVDS standard is 100 mV. Thus with the smallest V_{OD} (250 mV) and the maximum threshold of 100 mV, the differential noise margin (DNM) is 150 mV. This seems small, but due to the differential nature of the bus, it is not considered a problem. Most noise is coupled onto the line as common-mode and rejected by the receivers. Also the use of a well balanced media (like closely-coupled traces or twisted pairs) help to ensure common-mode coupling. Keeping noisy single-ended signals away and using shields is also a good form of isolation. Differential noise margin also needs to be taken into account when the LVDS line is un-driven and other parts of the system are still active or external noise still present. During this un-driven state, the differential noise margin is less than the driven states even with external failsafe biasing. A common argument against external failsafe biasing approach is related to "reduced" differential noise margins and waveform distortion. Depending upon the resistors selected, an external failsafe biasing may impact V_{OD} by ± 25 mV. In one active state it will boost the V_{OD} by 25 mV and in the other it will reduce it by 25 mV. Differential noise margin is reduced when it—see [Figure 5](#). The 150 mV is now 125 mV. This is still acceptable and also about 3X the differential noise margin of the un-driven bus—see [Figure 6](#). The AC distortion to the line is minimal at most, as we will see most LVDS receivers have very tight thresholds 30 mV to 40 mV in magnitude (typical), thus a V_{OD} of 225 mV or 275 mV has no real difference or impact to the receiver. In the case of the window detector, differential noise of 50 mV can cause the data line receiver to switch. If it does the failsafe logic is reset and the output switches, 600 ns later it returns to a failsafe HIGH, but only after the false switch (see REF #2). The 50 mV is related to the nominal hysteresis of the data receiver thresholds with no minimum specified in current datasheets. Thus differential noise margin is only 50 mV nominal for this approach. External failsafe biasing can be selected to provide this same amount of biasing or more if desired and required by the specific application.

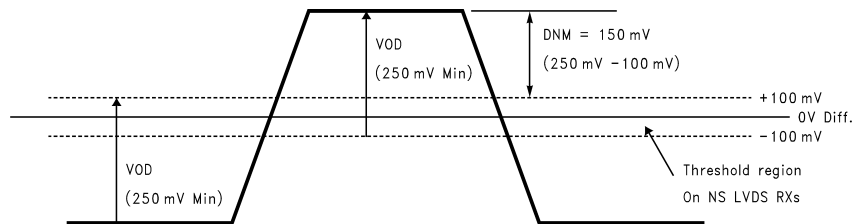


Figure 4. Differential Noise Margin Calculations

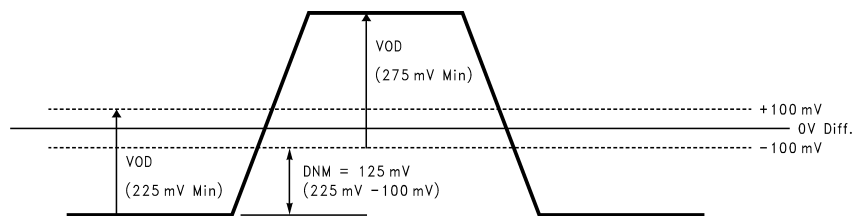


Figure 5. Differential Noise Margin Calculations with External Failsafe Biasing

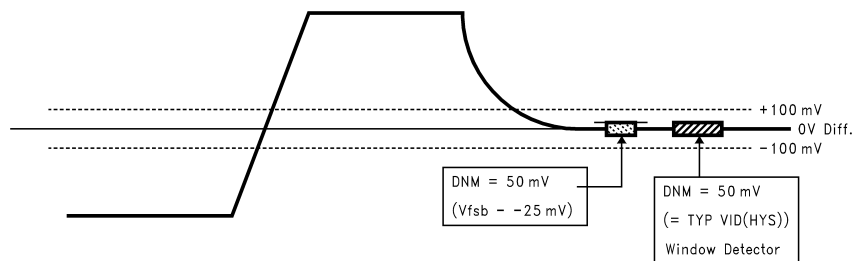


Figure 6. Differential Noise Margin for the Un-Driven Bus State vs Failsafe Implementation

National's LVDS receivers tend to have offset thresholds to the negative side to support the shorted failsafe condition. With $V_{ID} = 0V$, the output will be HIGH on devices that support this feature. The switch point is typically at about -25 mV as shown in Figure 1. The $\pm 100\text{ mV}$ limits are related to the threshold limited specified by the LVDS standard and are unrelated to the actual parts characterization and design. Limitation of ATE testers have defaulted to publishing the looser limits in datasheets to date. Recent developments in ATE equipment now support tighter step size and resolution, thus third generation receivers are being released with tighter threshold limits (see DS92CK16 for example with 70 mV threshold). With an external failsafe bias of $+25\text{ mV}$, a nominal differential noise margin of 50 mV is obtained, along with the benefits of the common-mode bias point and low impedance shunt path.

2 SUMMARY

External biasing for failsafe allows optimization of failsafe support per the specific application needs. It also provides the benefits of a common-mode set point and helps to control coupled noise. Differential noise margins in the un-driven state are of equal performance to other alternatives. With external biasing, the differential noise margin is user selectable at the expense of the external resistors. Waveform distortion caused by external biasing is minimal due to the switching performance of the LVDS receiver and its tight thresholds.

3 REFERENCES

1. LVDS Owner's Manual, 2nd Edition, Summer 2000, Lit#550062-002, National Semiconductor Corp.
2. The active Fail-safe Feature of the SN65LVDS32B, Application Report, SLLA082A, November 2000, Texas Instruments.

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