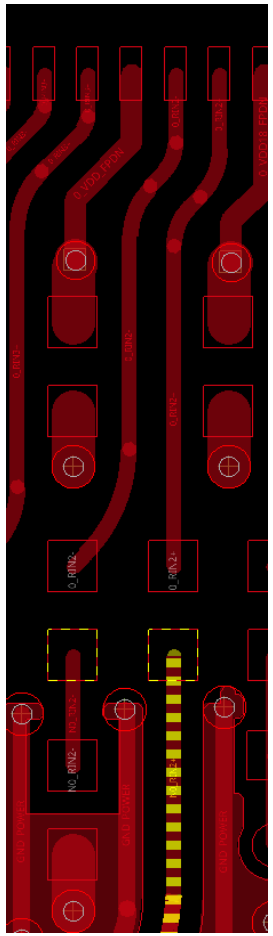
Layout Review 960

FPD-Link Applications

Tightly-Controlled Impedance Requirements

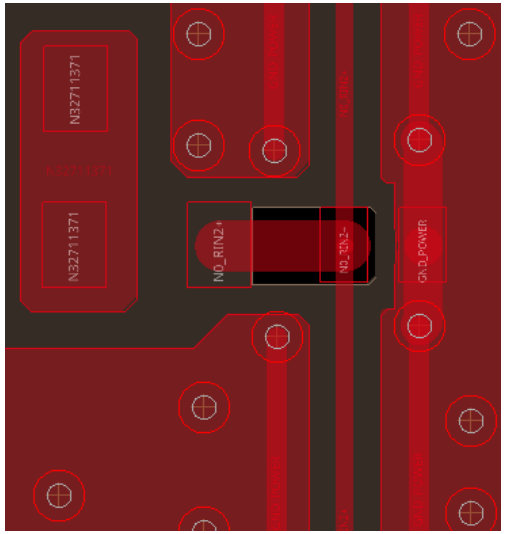
- High-speed signal traces require tight impedance control
- Make sure that the single-ended RIN+/- traces on the 960 each have tightly controlled 50-Ohms (+/-10%) single-ended impedance
  - consider routing RIN- to connector alongside RIN+ for EMI mitigation
- Recommend no breaks in ground reference plane underneath RIN trace
- The RIN- trace should be loosely-coupled to the RIN+ trace following AC capacitor
  - Spacing between RIN+/- traces should be at least 3 times the trace width, to minimize crosstalk

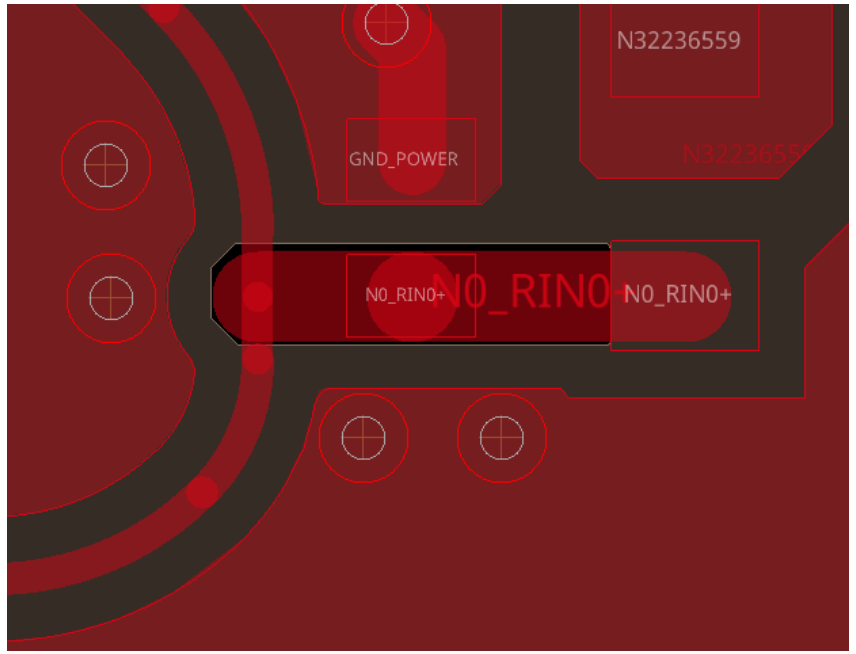
Single-ended impedance depends on a number of factors in your PCB, such as trace width, stack height, dielectric, etc.



PoC routing

- Anti-pad should present on the first inductor pad touching the DOUT trace
  - Recommend anti pad being placed under both of the component pads, only the component pads
  - Will assist minimizing impedance mismatch through the trace
  - First inductor should be placed orthogonally to the RIN trace, barely touching
- Recommend verifying trace length, PoC insertion loss and return loss channel specifications are met
- Confirm DOUT+ traces can carry PoC current without significant temperature rise

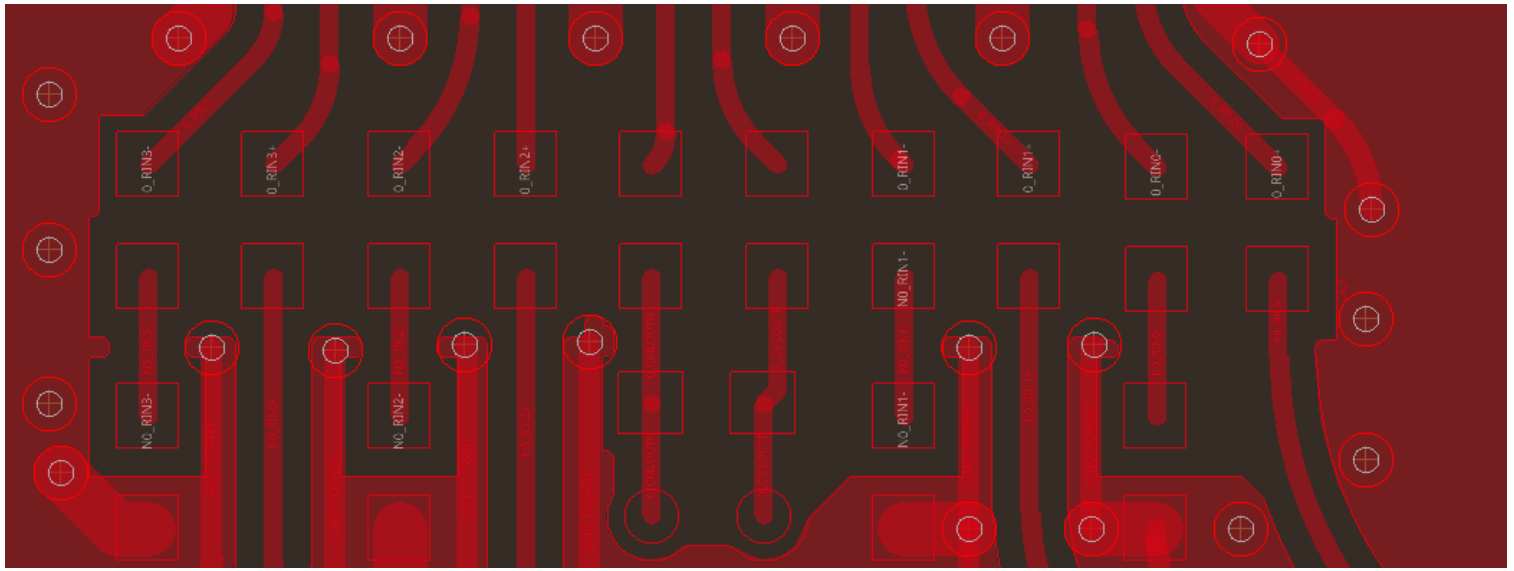


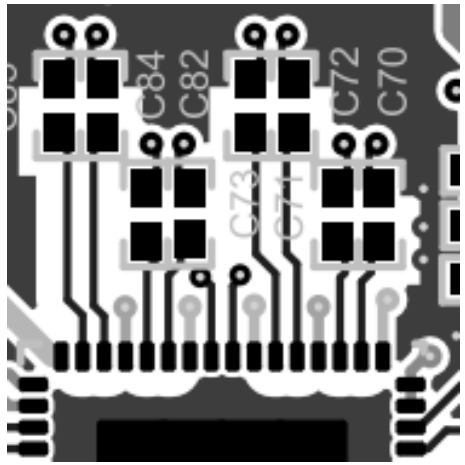


Take care to confirm no significant impedance mismatch with change in trace width through the PoC network routing

RIN AC Coupling Capacitors

- Recommend placing anti-pads under the AC coupling capacitor pads on the RIN trace
  - size of the anti-pad should match the size of the capacitor pad
- Recommend moving AC coupling capacitors as close as possible to the device
  - Prior to AC coupling capacitor 100 ohm differential impedance between Rin+/- pair
  - Following AC coupling capacitors 50 ohm single ended impedance on the Rin traces
- AC coupling capacitors should be slightly staggered to prevent crosstalk between traces

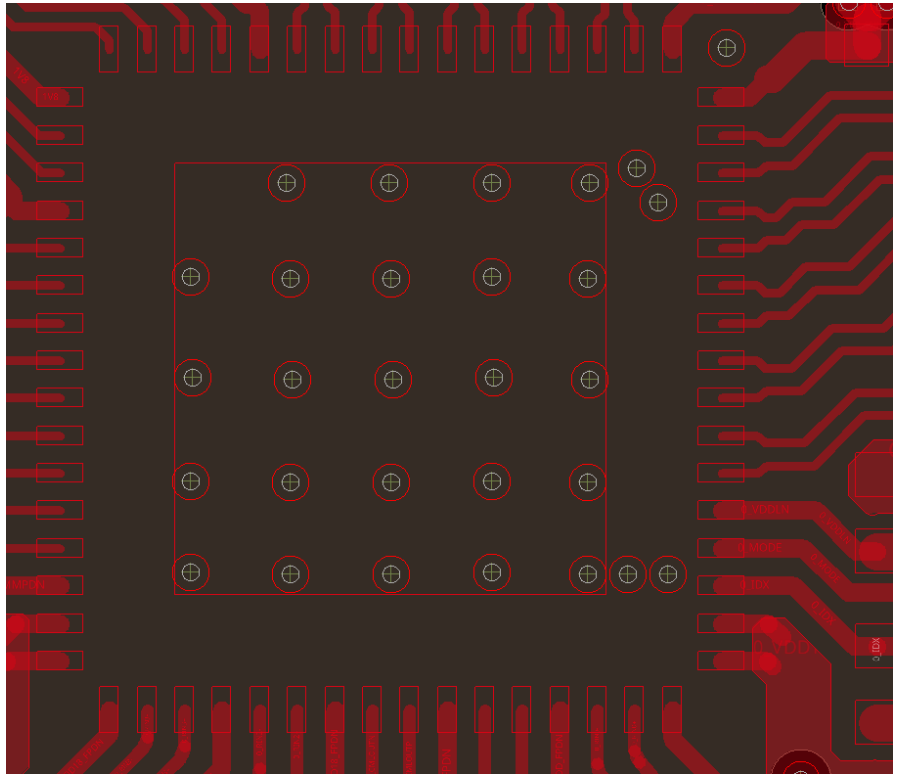


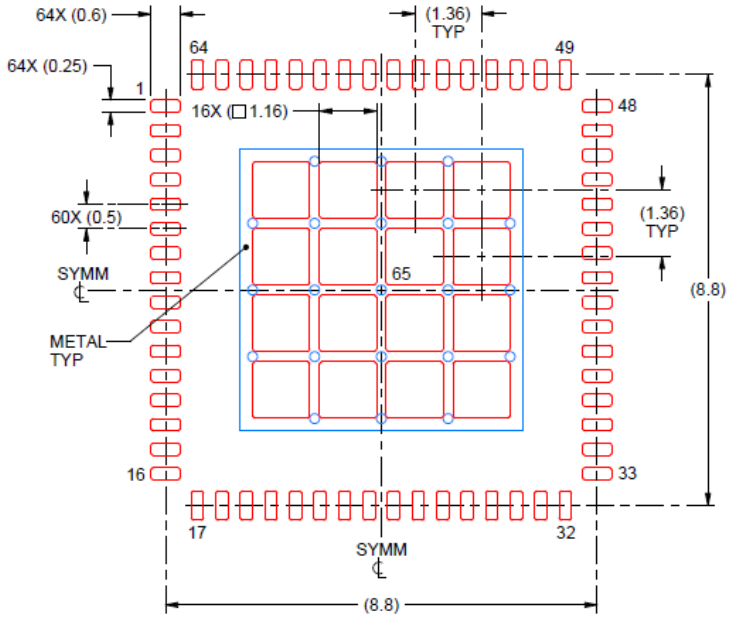


960 EVM Example for AC Capacitor Placement

Irregular via placement

- Recommend following provided landing pattern for thermal requirements





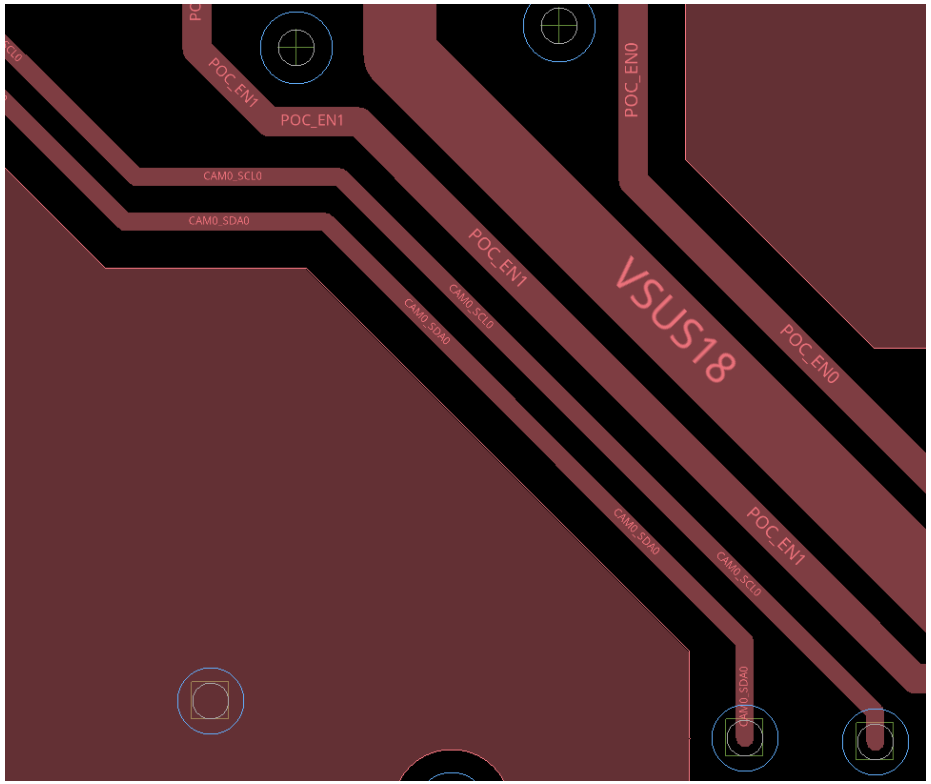
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
65% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:8X

Recommended landing pattern

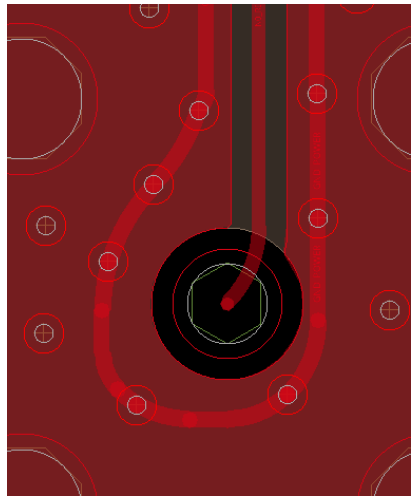
I2C Routing

- Consider limiting length of I2C sections routed closely to each other to prevent coupling and noise between traces

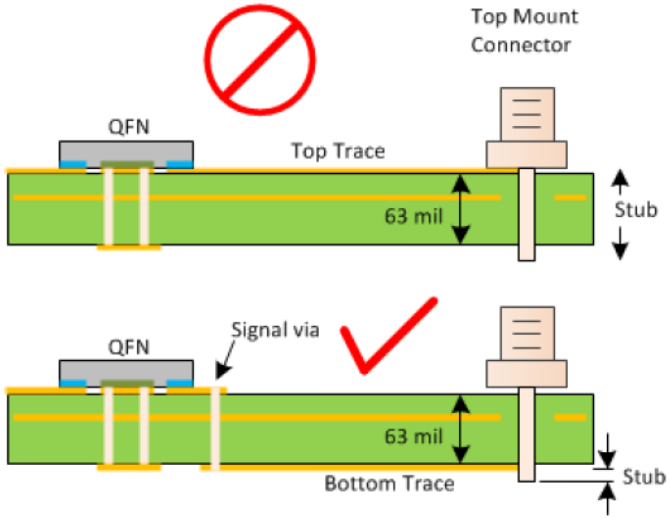


FPD-Link routing

- Consult connector vendor for optimal connector footprint. If the connector is a through-hole component, TI recommends placing the connector on the opposite side of the board to the RIN traces to avoid stubs. This is critical for ensuring good signal integrity.
- Recommend to use simulation to verify the effects of the connector landing pattern on the impedance



Example 960 Connector



CSI-2

- Make sure to double-check that all of the CSI-2 layout guidelines defined in the device datasheet are followed, as well as maintain a continuous ground plane under the traces
- See the next slides for more details.

CSI-2 Layout Guidelines

10.1.1 CSI-2 Guidelines

1. Route CSI0_D*P/N pairs with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
2. Keep away from other high-speed signals.
3. Keep the length difference between a differential pair to 5 mils of each other.
4. Make sure that length matching is near the location of mismatch.
5. Match trace lengths between the clock pair and each data pair to be < 25 mils.
6. Separate each pair by at least 3 times the signal trace width.
7. Keep the use of bends in differential traces to a minimum. When bends are used, the number of left and right bends must be as equal as possible, and the angle of the bend should be ≥ 135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
8. Route all differential pairs on the same layer to help match trace impedance characteristics.
9. Keep the number of VIAS to a minimum—TI recommends keeping the VIA count to two or fewer.
10. Keep traces on layers adjacent to ground plane.
11. Do NOT route differential pairs over any plane split.

Note

Adding test points can cause impedance discontinuity and therefore negatively impacts signal performance. If test points are used, place them in series and symmetrically. Test points must not be placed in a manner that causes a stub on the differential pair.

CSI Trace Length Matching Between Pairs

- CSI trace lengths between pairs should be within 25 mils of each other
  - Current trace lengths have a difference of >50mils between CSI0 D3 and CSI0 D0

CSI0_LCKN-CON	1093.949
CSI0_LCKP-CON	1094.829
CSI0_LDN0-CON	1111.201
CSI0_LDN1-CON	1109.612
CSI0_LDN2-CON	1081.511
CSI0_LDN3-CON	1062.292
CSI0_LDP0-CON	1113.210
CSI0_LDP1-CON	1109.856
CSI0_LDP2-CON	1081.684
CSI0_LDP3_CON	1060.638

Etch length (mils) from Allegro Report

CSI Ground Stitching

- Recommend ground stitching for the between CSI-2 signal pairs