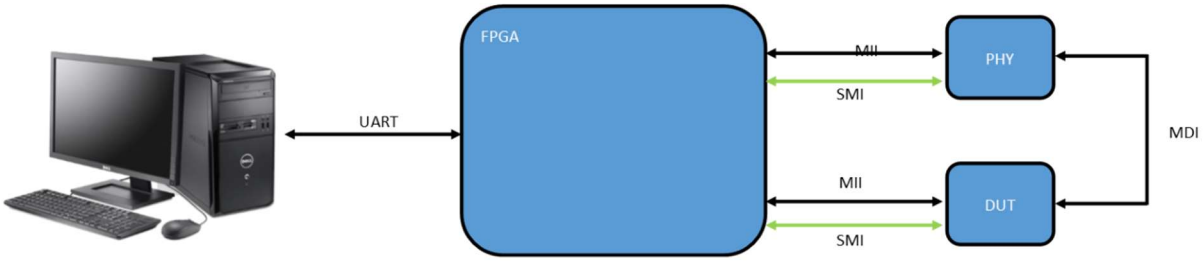
Loopback Explanation and results

Table des matières

Figures

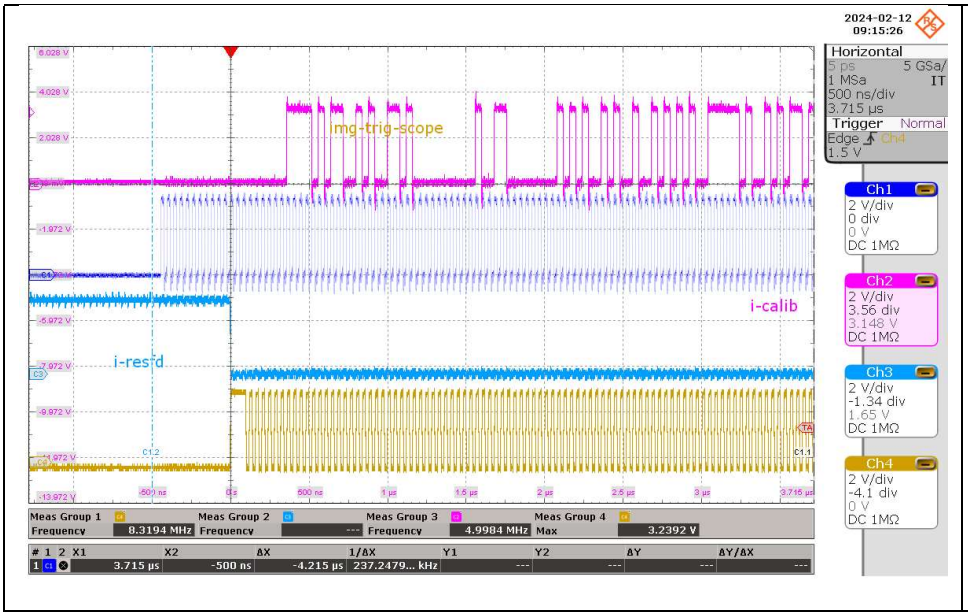
1 Configuration



The two phys (DP83822) are driven by the FPGA and MDI are wired together via RJ45 connectors

2 Without loopback

Data are send by Phy and not received on DUT.



CH1 : TX_CTL
CH2 : TXD1
CH3 : RXD1
CH4 : RX_CTL

Data is send on TXD1 along TX_CTL (‘1’ on rising edge of TX_CLK and ‘0’ on the falling edge of TX_CLK)
The RXD1 is always at ‘0’ and RX_CTL is ‘1’ on rising edge of RX_CLK and ‘0’ on falling edge of RX_CLK. RX_CTL on the two first nibbles is ‘1’ on rising edge of RX_CLK and ‘1’ on falling edge of RX_CLK

3 MII Loopback

Register Configuration on DUT : Set bit 14 of register 0x0000

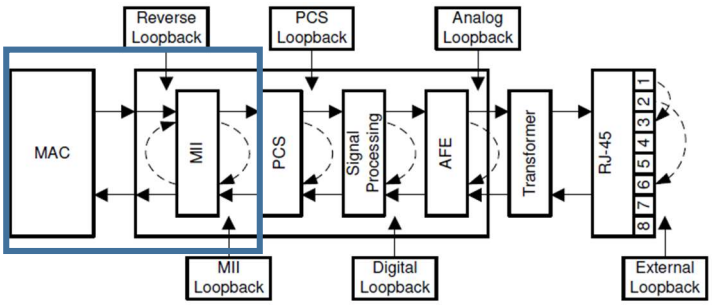


Figure 8-8. Loopback Test Modes

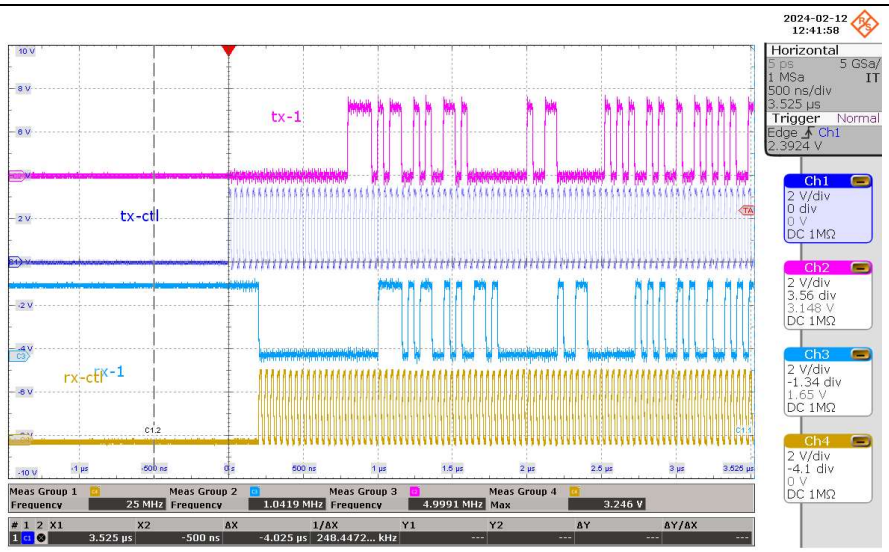


Figure 1 : MII loopback signals

CH1 : RXD1
CH2 : TXD1
CH3 : TX_CTL
CH4 : RX_CTL

Data are sent by MAC and are retreived on MAC.

4 PCS output Loopback

Loopback mode is set by register 0x16[4 :0] at 0x02 on DUT

```
53  void SetPCSOutloopback(PHYCHIP_instance_t *this){
54      DP83822_Write(this,BISCR,0x0102);
55  }
56
```

Figure 2 : Code for PCS Loopback

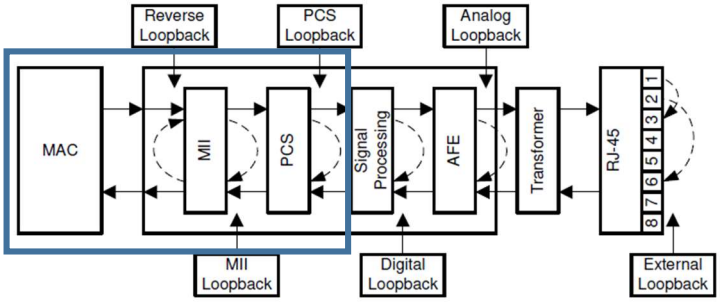


Figure 8-8. Loopback Test Modes

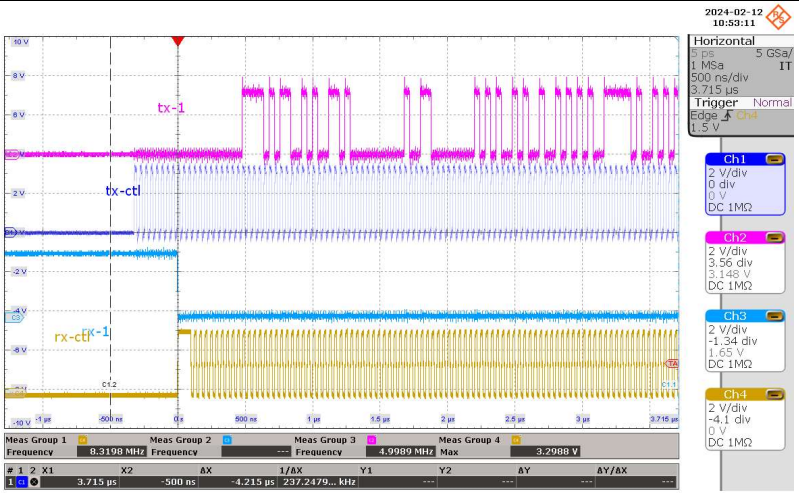


Figure 3 : PCS Loopback signal on MII interface

CH1 : TX_CTL
CH2 : TXD1
CH3 : RXD1
CH4 : RX_CTL

Data are sent on MII TX interface but not retrieved on MII RX interface.

0x0 : 0x3100	0x1 : 0x786d
0x2 : 0x2000	0x3 : 0xa240
0x4 : 0x181	0x5 : 0x4181
0x6 : 0x5	0x7 : 0x2001
0x8 : 0x0	0x9 : 0x80
0xa : 0x121	0xb : 0x1000
0xf : 0x0	0x10 : 0x2615
0x11 : 0x108	0x12 : 0x8000
0x13 : 0xff	0x14 : 0x0
0x15 : 0x3a8	0x16 : 0x102
0x17 : 0x261	0x18 : 0x400
0x19 : 0x8c00	0x1a : 0x0
0x1b : 0x7d	0x1c : 0x5ee
0x1d : 0x0	0x1e : 0x102
0x1f : 0x0	0x25 : 0x1
0x27 : 0x0	0x3e : 0x0
0x3f : 0xb4ff	0x40 : 0xc11d
0x42 : 0x0	0x101 : 0x2002
0x106 : 0xb0bb	0x107 : 0x605
0x10f : 0x300	0x111 : 0x6003
0x114 : 0x400a	0x116 : 0x14a
0x121 : 0x199a	0x122 : 0x1027
0x123 : 0x51c	0x126 : 0x461b
0x129 : 0xf	0x130 : 0x4750
0x155 : 0x1f31	0x170 : 0xe52
0x171 : 0xc85c	0x177 : 0x189b
0x41f : 0x0	0x421 : 0x7
0x428 : 0x0	0x460 : 0x551
0x462 : 0x1	0x467 : 0x78f
0x468 : 0x0	0x469 : 0x40
0x4a0 : 0x1000	0x4a1 : 0x0
0x4d0 : 0x302	0x4d1 : 0x18a
0x3000 : 0x400	0x3001 : 0x40
0x3014 : 0x2	0x3016 : 0x0

Figure 4 : Register for PCS Loopback

5 Reverse Loopback on other Phy with PRBS activated on DUT

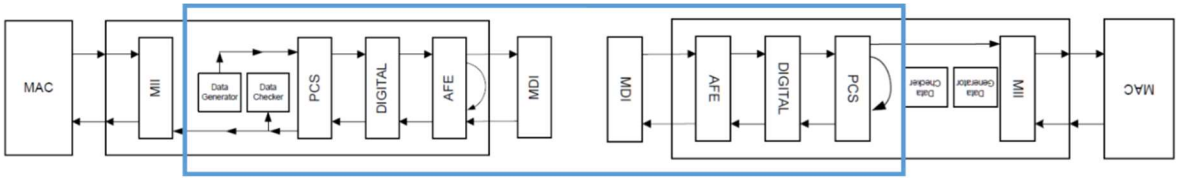


Figure 5 : Reverse Loopback configuration

RJ45 are connected together via ethernet cable. Master is the DUT on left.

DUT send PRBS data and PHY is on reverse loopback mode.

```
void SetReverseLoopback(PHYCHIP_instance_t *this){
        if (this->Master == 1) {
            DP83822_Write(this, 0, 0x2100);    //disable autoneg
            DP83822_Write(this, 0x30B, 0x3380); //helps prbs lock
            DP83822_Write(this, 0x16, 0x3100); //enable PRBS checker and packet generation enable
            DP83822_Write(this, 0x1B, 0x807d); //lock error counter value
        } else {
            DP83822_Write(this, 0, 0x2100); //disable autoneg
            DP83822_Write(this, 0x16, 0x0110); //Reverse loopback
        }
}
```

Figure 6 : Code for Reverse Loopback

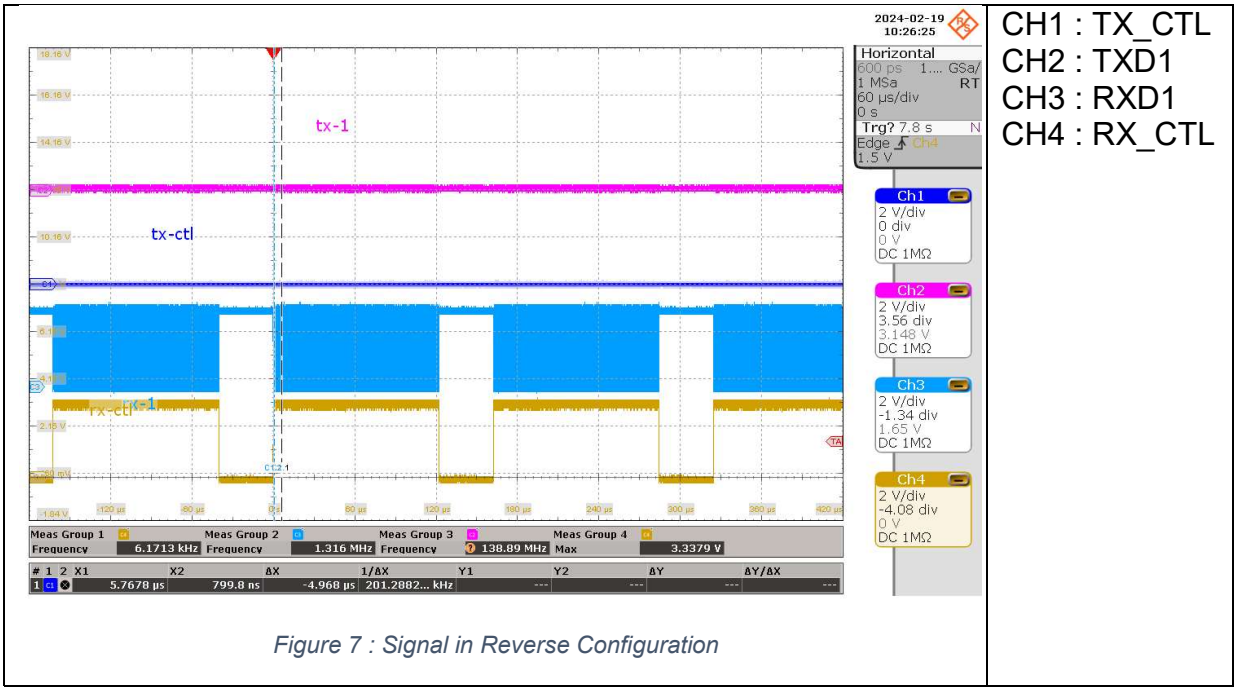


Figure 7 : Signal in Reverse Configuration

There is data on RX_D1 but RX_CTL is at '1' along Data

Register 0x16 : 0x3B00

Bit	Name	Value	Meaning
14	BIST Error Counter Mode	0	Single mode
13	PRBS Checker	1	Enabled
12	Packet Generation Enable	1	Enabled

11	PRBS Checker Lock/Sync	1	Locked
10	PRBS Checker Sync Loss	0	Has not lost sync
9	Packet Generator Status	1	PRBS is active and generating packets

Register 0x001B : 0x007B

Bit	Name	Value	Meaning
15:8	BIST Error Counter	0x00	Error Count
7:0	BIST IPG Length	0x7B	IPG Length

0x0 : 0x2100	0x1 : 0x784d
0x2 : 0x2000	0x3 : 0xa240
0x4 : 0x181	0x5 : 0x0
0x6 : 0x4	0x7 : 0x2001
0x8 : 0x0	0x9 : 0x80
0xa : 0x121	0xb : 0x1000
0xf : 0x0	0x10 : 0x4605
0x11 : 0x108	0x12 : 0x0
0x13 : 0xff	0x14 : 0x0
0x15 : 0x0	0x16 : 0x3b00
0x17 : 0x261	0x18 : 0x400
0x19 : 0x8400	0x1a : 0x0
0x1b : 0x7d	0x1c : 0x5ee
0x1d : 0x0	0x1e : 0x102
0x1f : 0x0	0x25 : 0x1
0x27 : 0x0	0x3e : 0x0
0x3f : 0xb4ff	0x40 : 0xc11d
0x42 : 0x0	0x101 : 0x2002
0x106 : 0xb0bb	0x107 : 0x605
0x10f : 0x300	0x111 : 0x6003
0x114 : 0x400a	0x116 : 0x14a
0x121 : 0x199a	0x122 : 0x1027
0x123 : 0x51c	0x126 : 0x461b
0x129 : 0xf	0x130 : 0x4750
0x155 : 0x1f41	0x170 : 0xe52
0x171 : 0xc85c	0x177 : 0x189b
0x41f : 0x0	0x421 : 0x7
0x428 : 0x0	0x460 : 0x551
0x462 : 0x1	0x467 : 0x78f
0x468 : 0x0	0x469 : 0x40
0x4a0 : 0x1000	0x4a1 : 0x0
0x4d0 : 0x302	0x4d1 : 0x18a
0x3000 : 0x400	0x3001 : 0x40
0x3014 : 0x2	0x3016 : 0x0

Figure 8 : Registers on DUT for Reverse Loopback

6 PCS Loopback with PRBS

Same result when PCS loopback is run with PRBS (except register 0x16 : 0x3B02) as Reverse loopback.