1. 问题描述（Problem description）
2. 单板原采用PHY芯片AR8033，改版更换为TI的芯片DP83869之后，PHY芯片RJ45口和光口： 无论百兆、千兆在快ping包时，有明显丢包，丢包概率为30~200ppm左右；

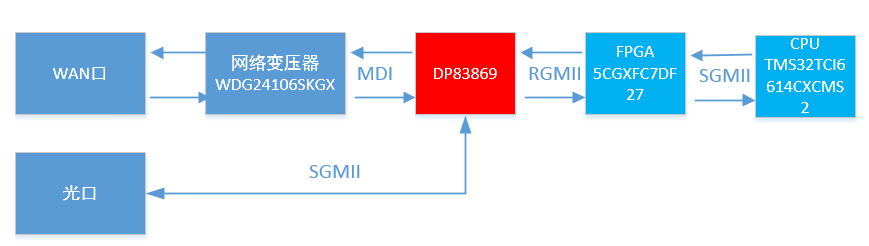
The board originally used the AR8033 PHY chip, which was later replaced by TI's DP83869 chip. When we test the PHY chip as RJ45 port or optical port: No matter 100M or 1000M, there is obvious packet loss when using fast ping packets, and the packet loss probability is around 30~200ppm.

1. 测试工具(test equipment)

万用表、示波器、频谱仪、光转网模块

（Multimeter, oscilloscope, spectrum analyzer, optical switch module）

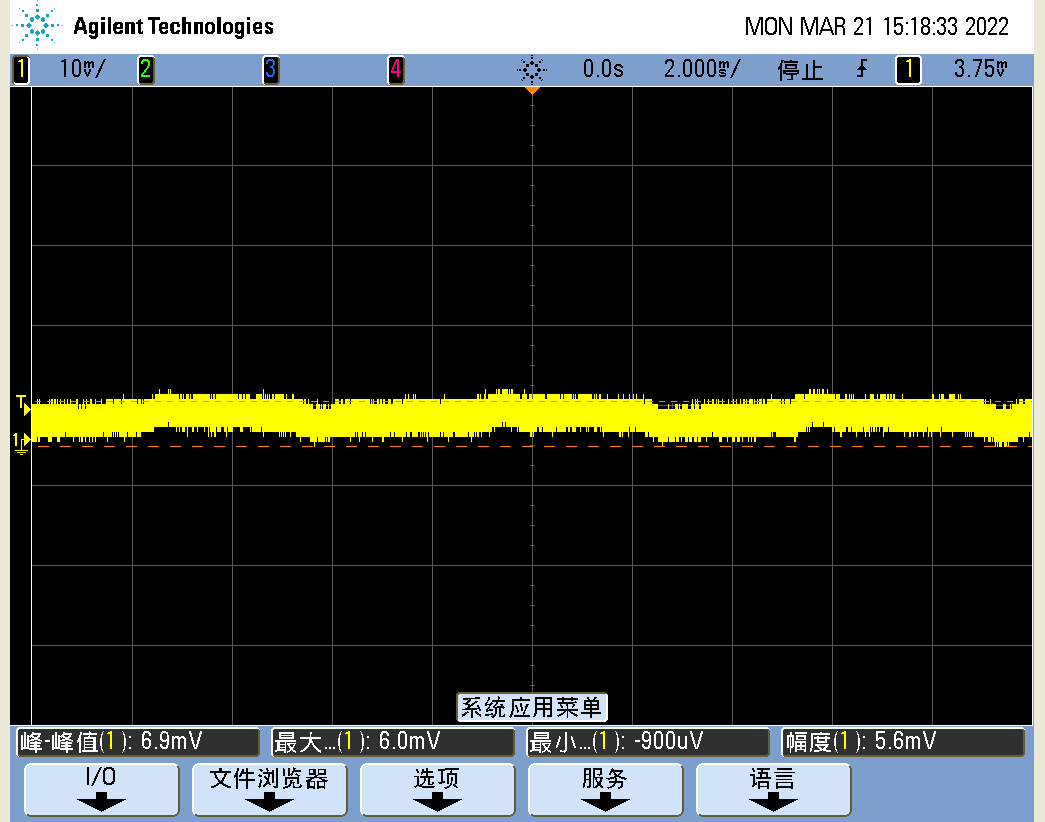
1. 系统框图（System block diagram）



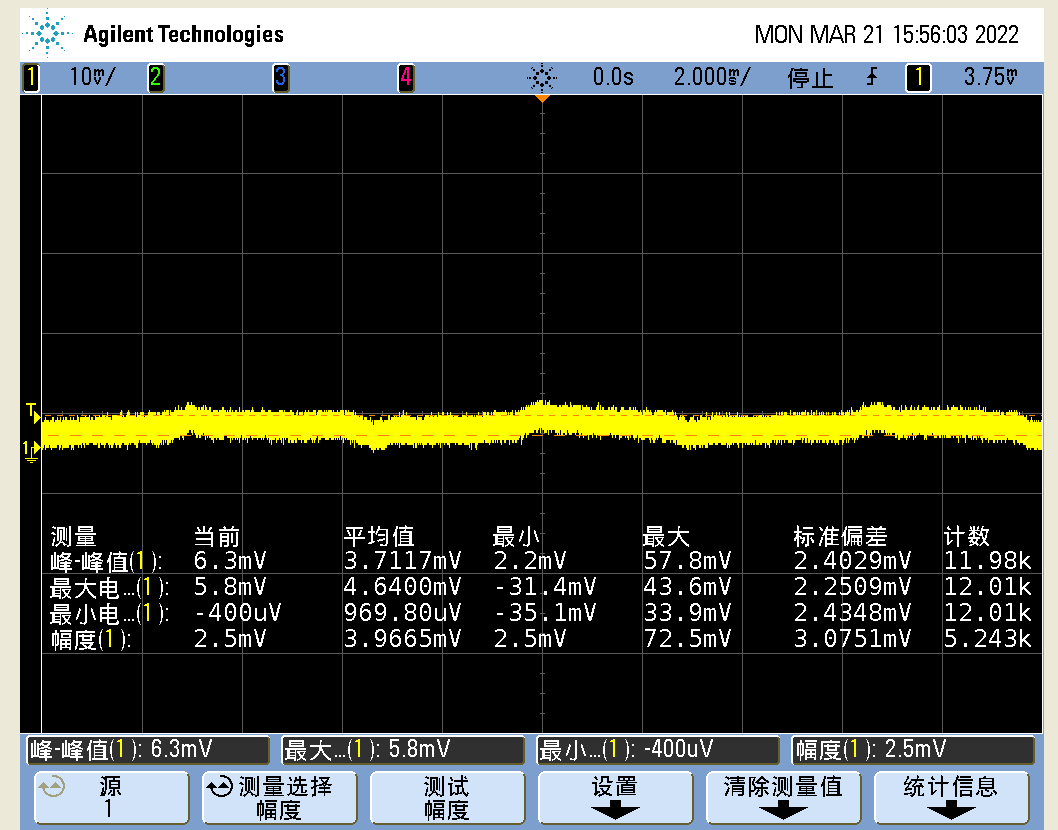
1. 排查记录：（Check record:）

1）Power supply：VDDA2P5=2.51；VDD1P1=1.14；VDDIO=3.32V；

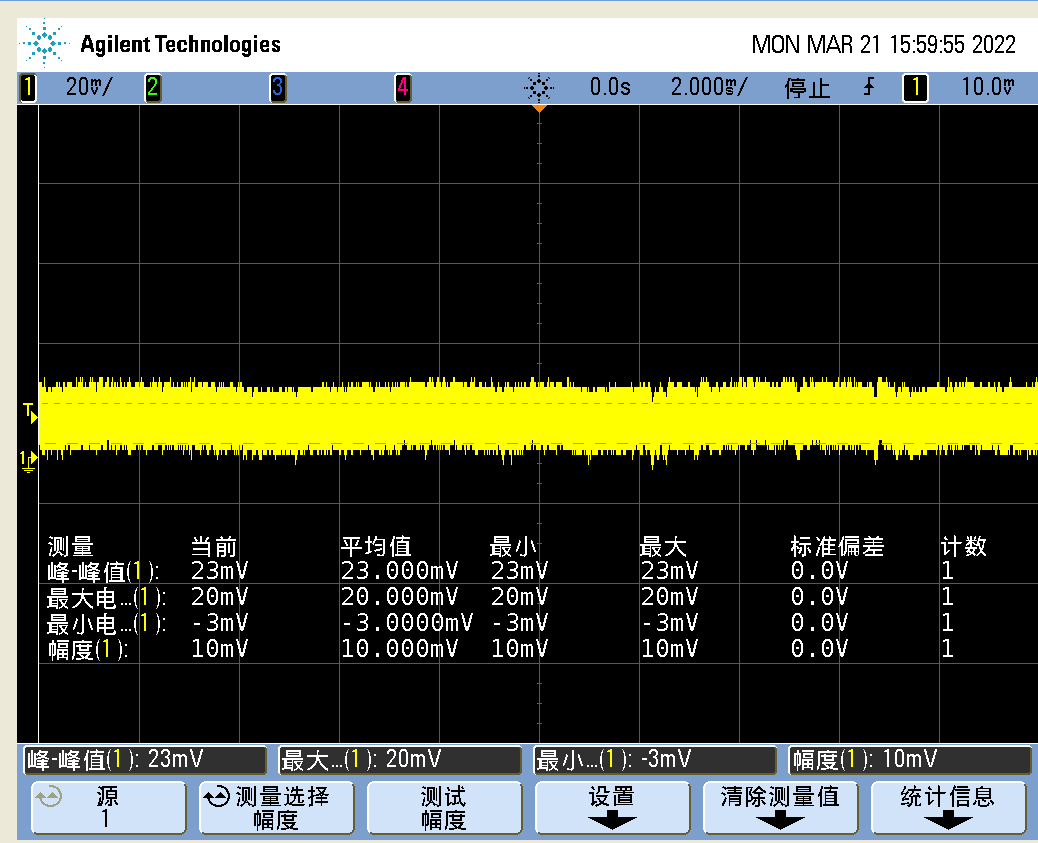
2）power ripple：VDD1P1：6.9mV



VDDA2P5：6.3mV



VDDIO：23mV



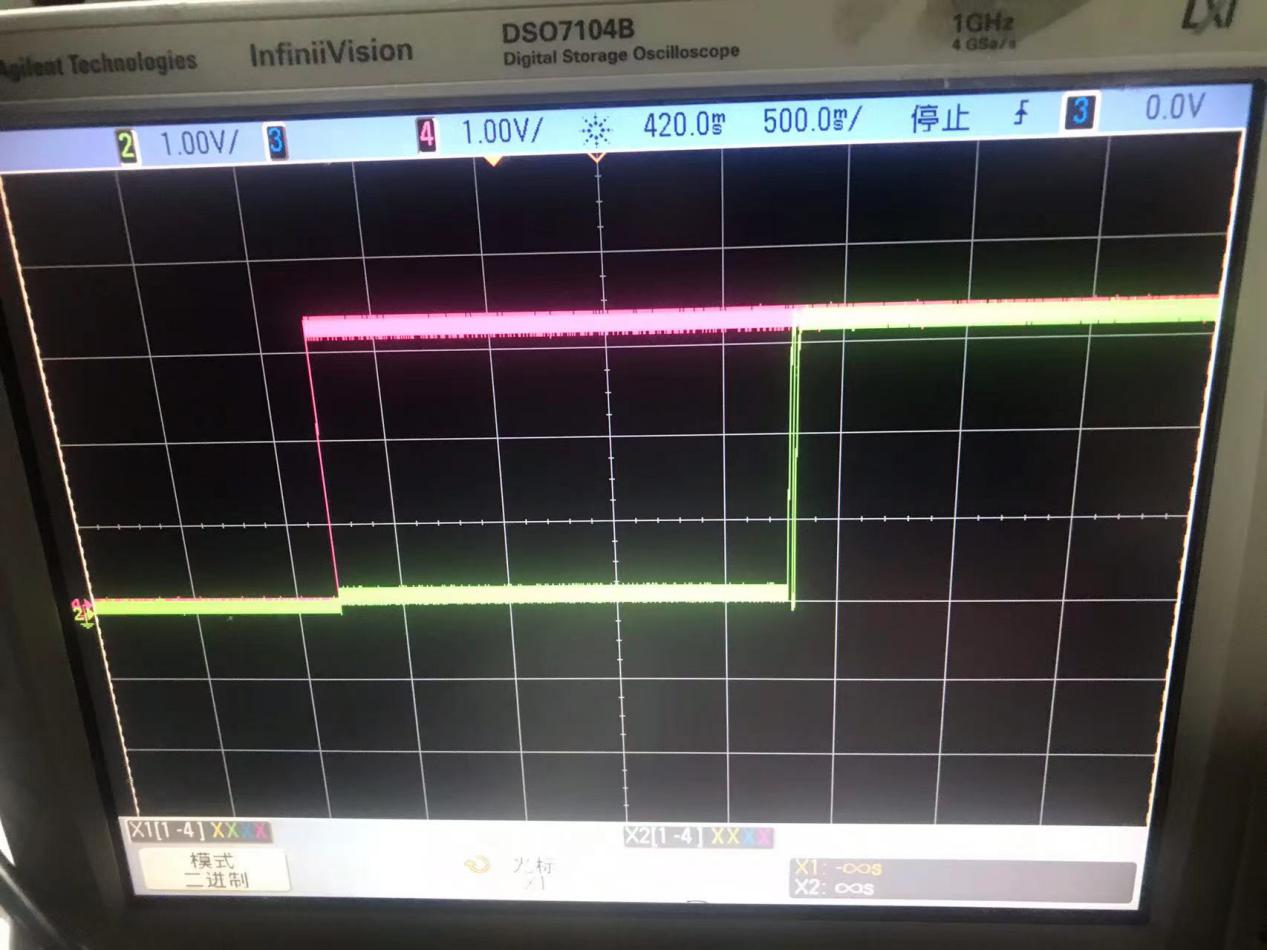
3）电源上电时序：(power on timing)

3.3V&RESET上电复位时序：粉色信号为VDDIO 3.3V, 绿色信号为复位信号

3.3V&RESET power-on reset sequence: pink signal is VDDIO 3.3V, green signal is reset signal

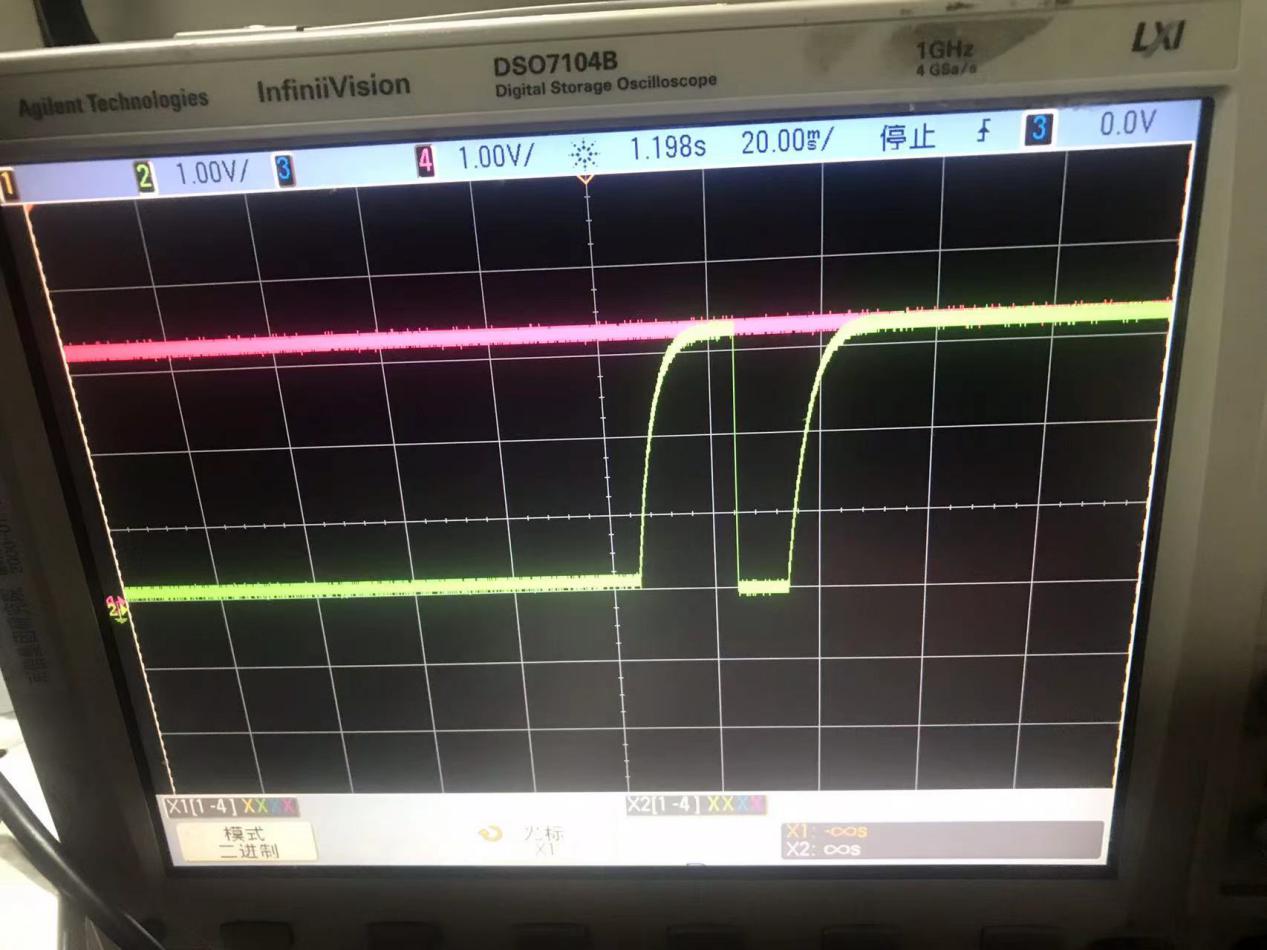
复位信号在电源准备好之后实施了释放动作，释放复位后，单片机还对PHY进行了热复位操作。

The reset signal implements a release action after the power supply is ready, and after releasing the reset, the microcontroller also performs a warm reset operation on the PHY.



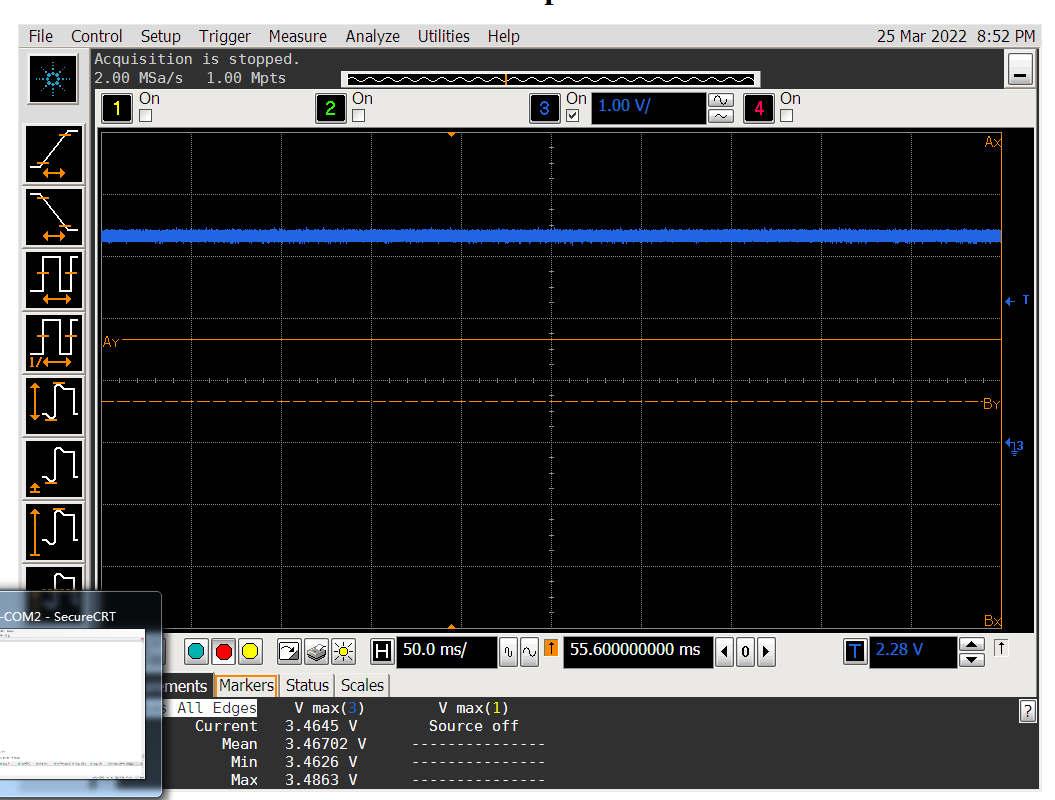
复位时间：下图中绿色线的第一个上升沿为上电复位释放，第一个下降沿到单片机热复位PHY，时间约为10ms

Reset time: The first rising edge of the green line in below photo is the power-on reset release, and the first falling edge to the microcontroller warm reset PHY, the time is about 10ms



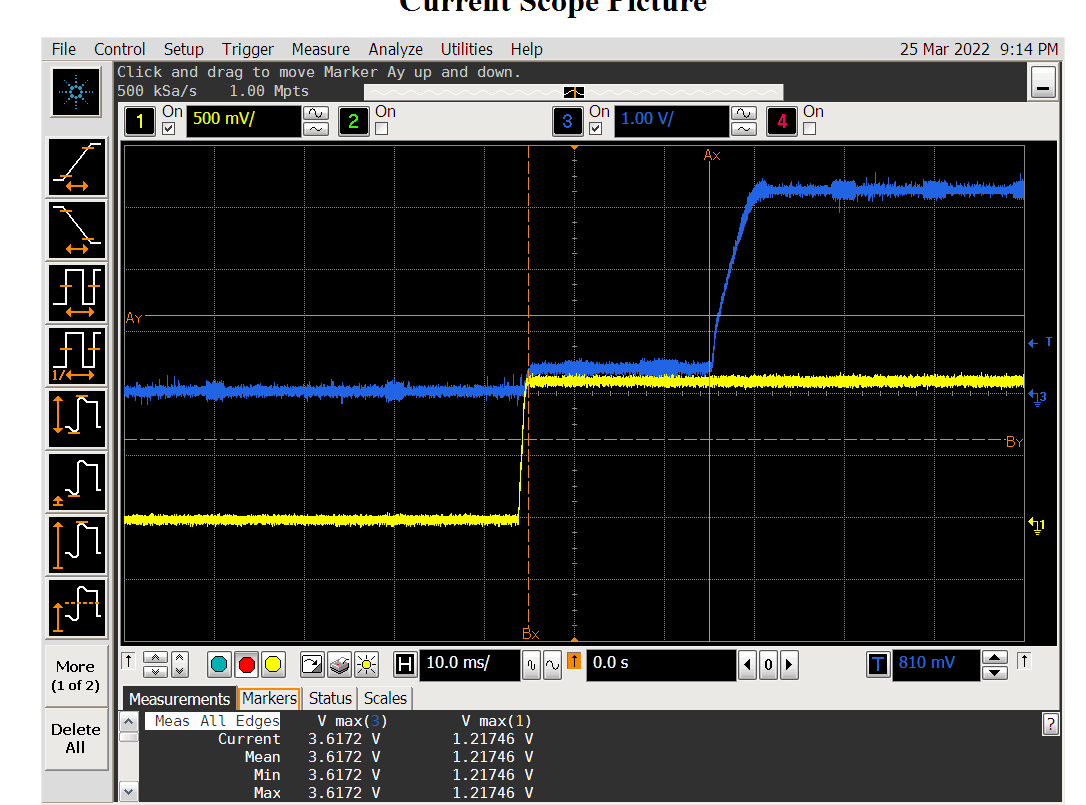
VDDIO3.3V电源：（下降沿触发，在丢包的情况下，电源没有跌落）

VDDIO3.3V power supply: (triggered by falling edge, in the case of packet loss, the power supply does not drop)



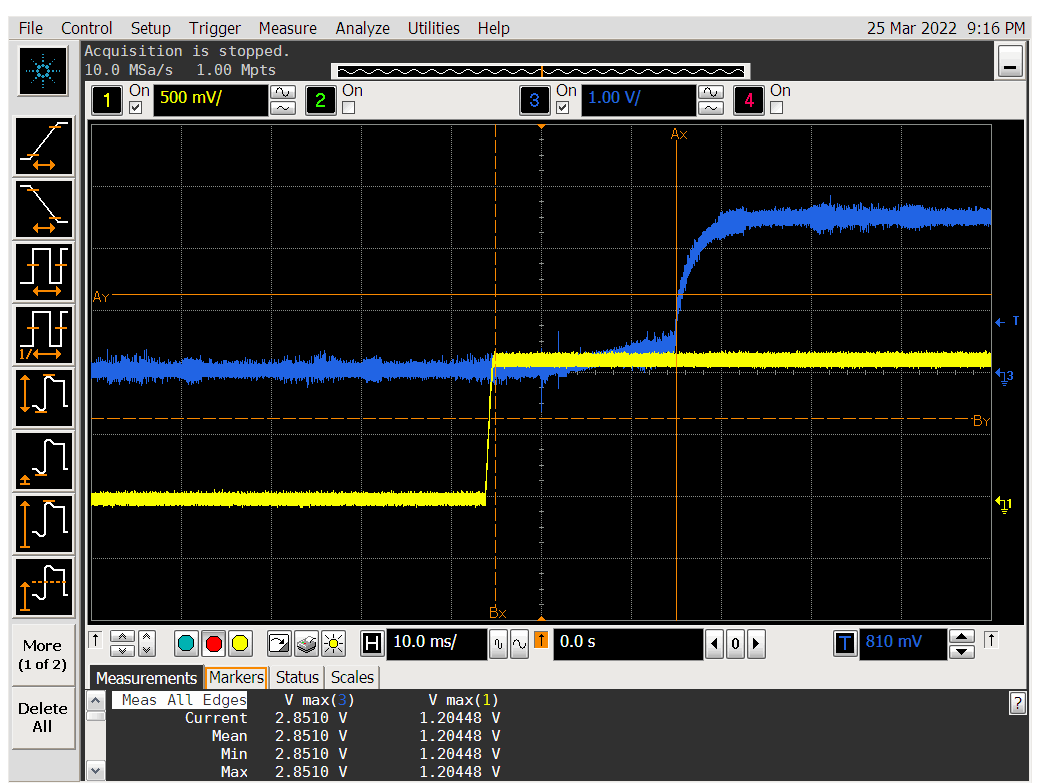
1.15V&3.3V上电时序：（万用表测试VDD=1.15V）

1.15V&3.3V power-on sequence: (multimeter test VDD=1.15V)



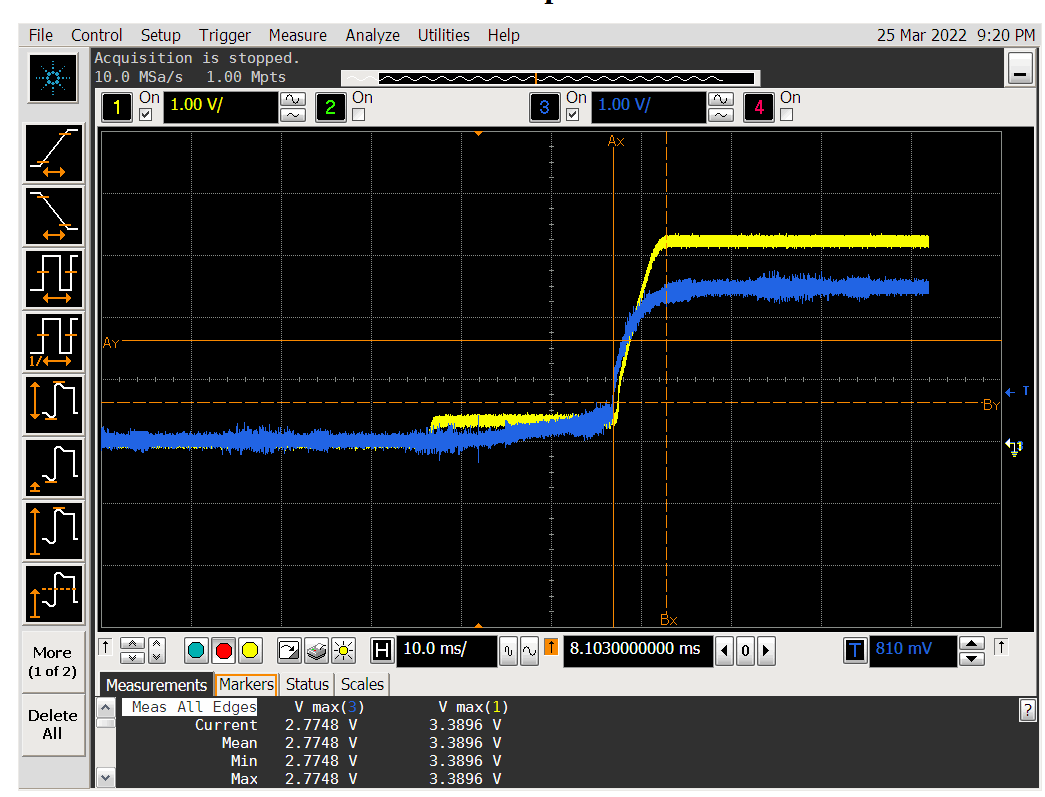
1.15V&2.5V上电时序：（万用表测试VDDA=2.25V）

1.15V&2.5V power-on sequence: (multimeter test VDDA=2.25V)



3.3VV&2.5V上电时序：（万用表测试VDDIO=3.32V）

3.3VV&2.5V power-on sequence: (multimeter test VDDIO=3.32V)



3）RGMII信号测试：(RGMII signal test:)

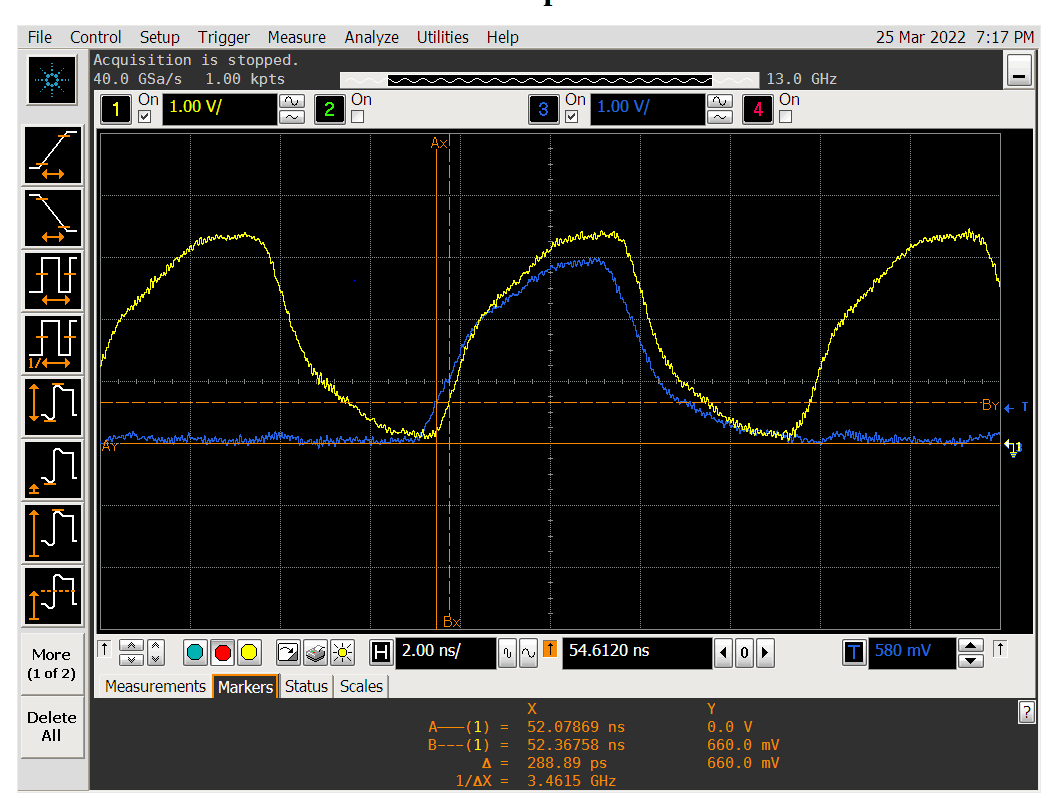
光口强制千兆测试::0x32寄存器：dn wr smi 10e d3；关闭PHY时延；

Optical port forced gigabit test::0x32 register: dn wr smi 10e d3; turn off PHY delay;

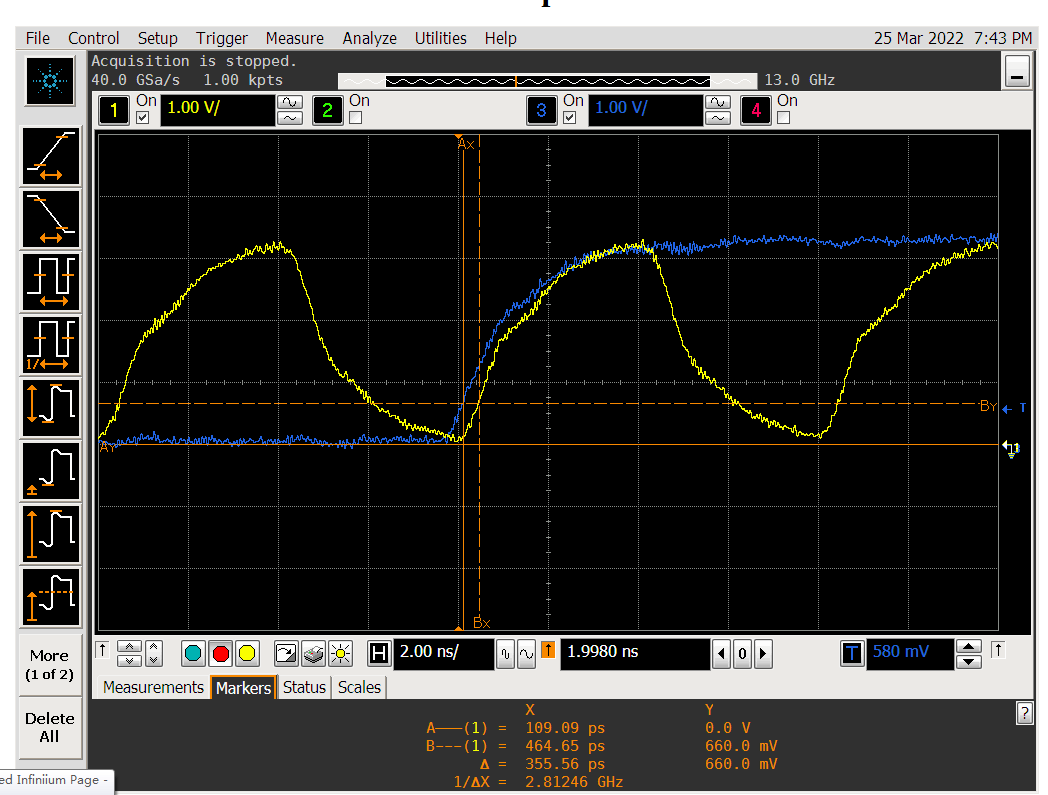
1.时钟余晖测试：（RX\_CLK）没有异常(Clock afterglow test: (RX\_CLK) no exception)



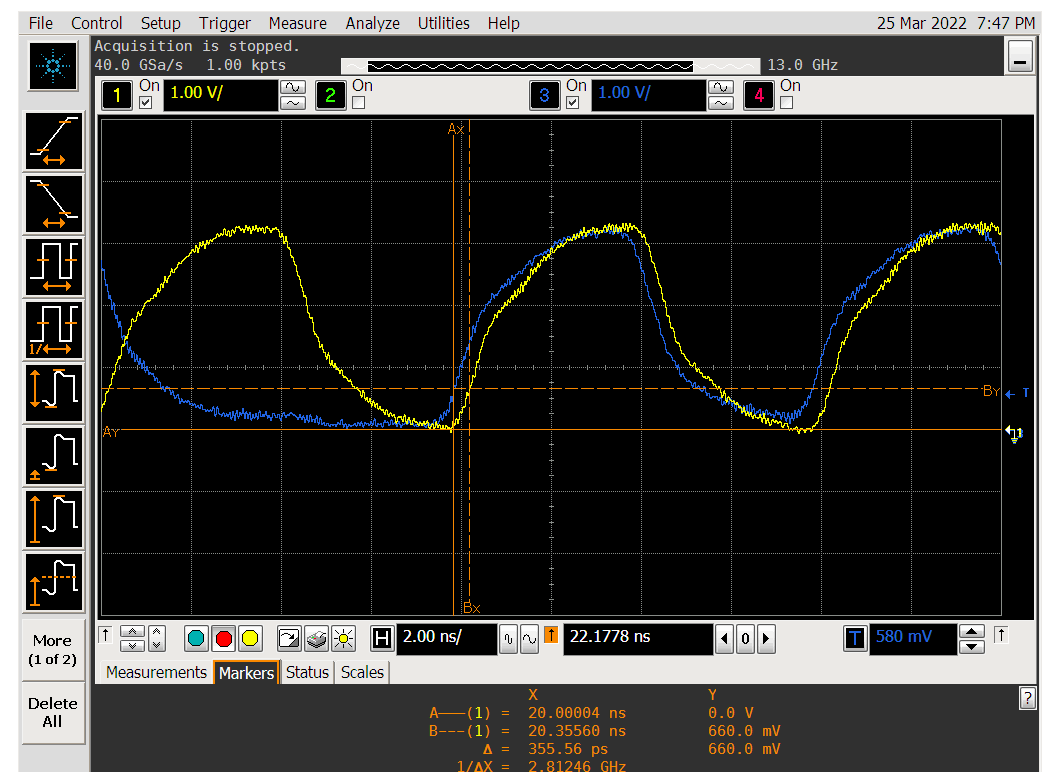
2.RXD0& RX\_CLK：



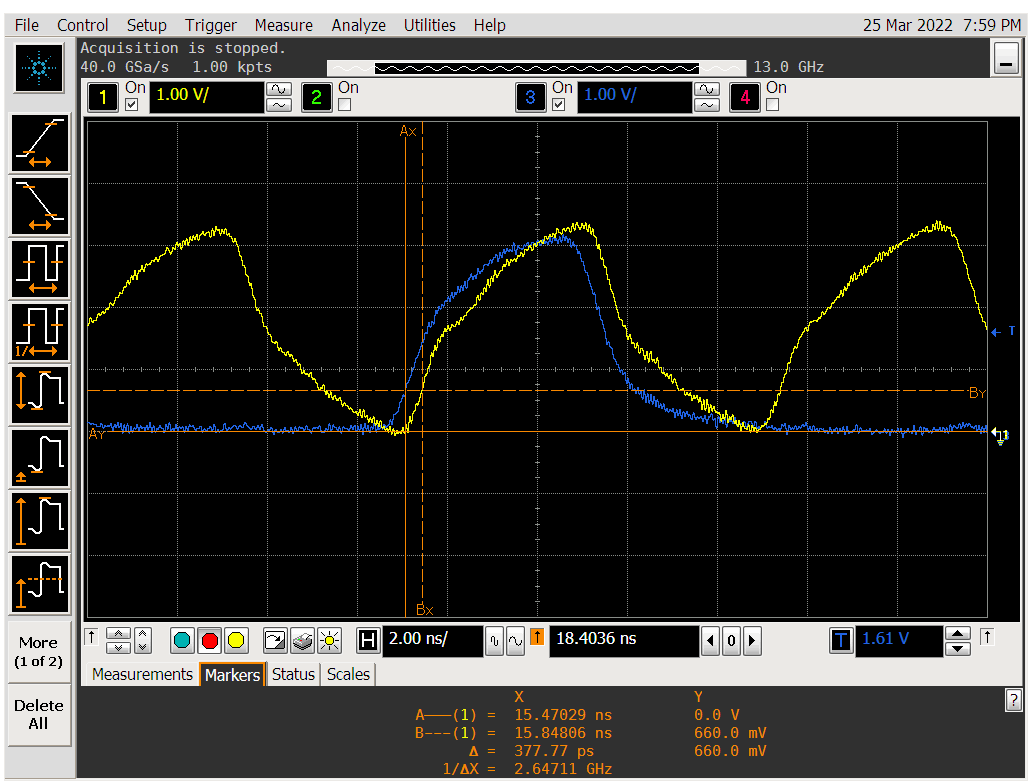
EN&RXCLK:



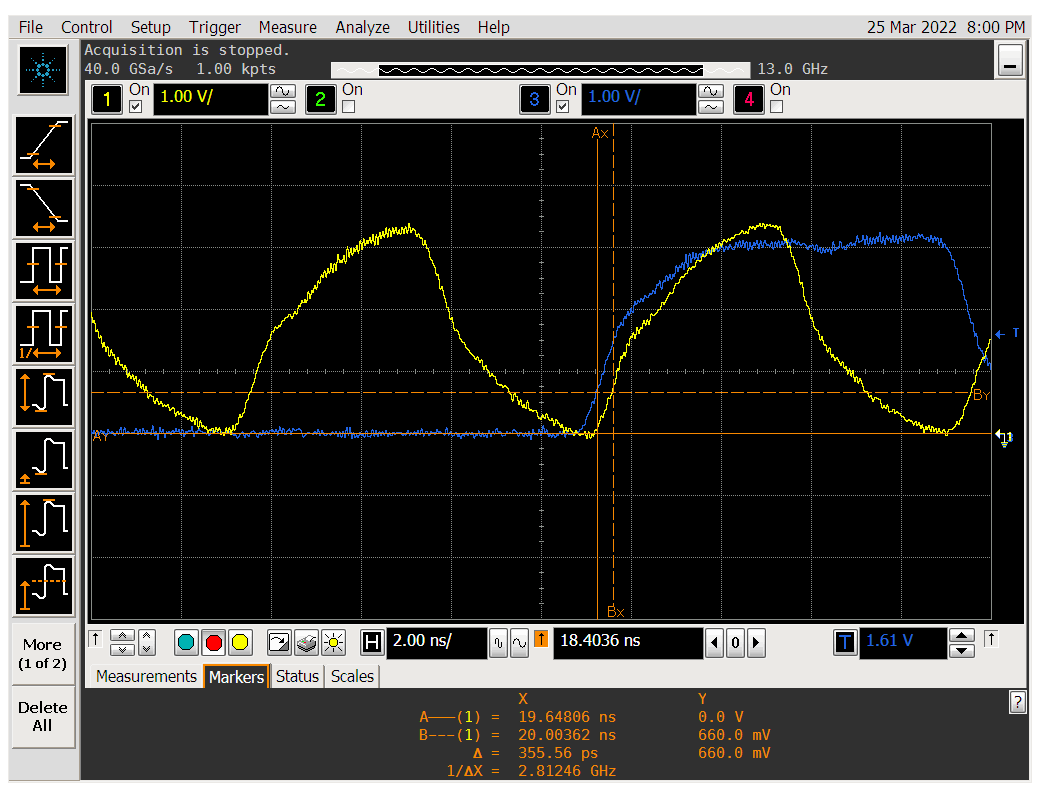
RX1&RXCLK：



RX2&RXCLK:：



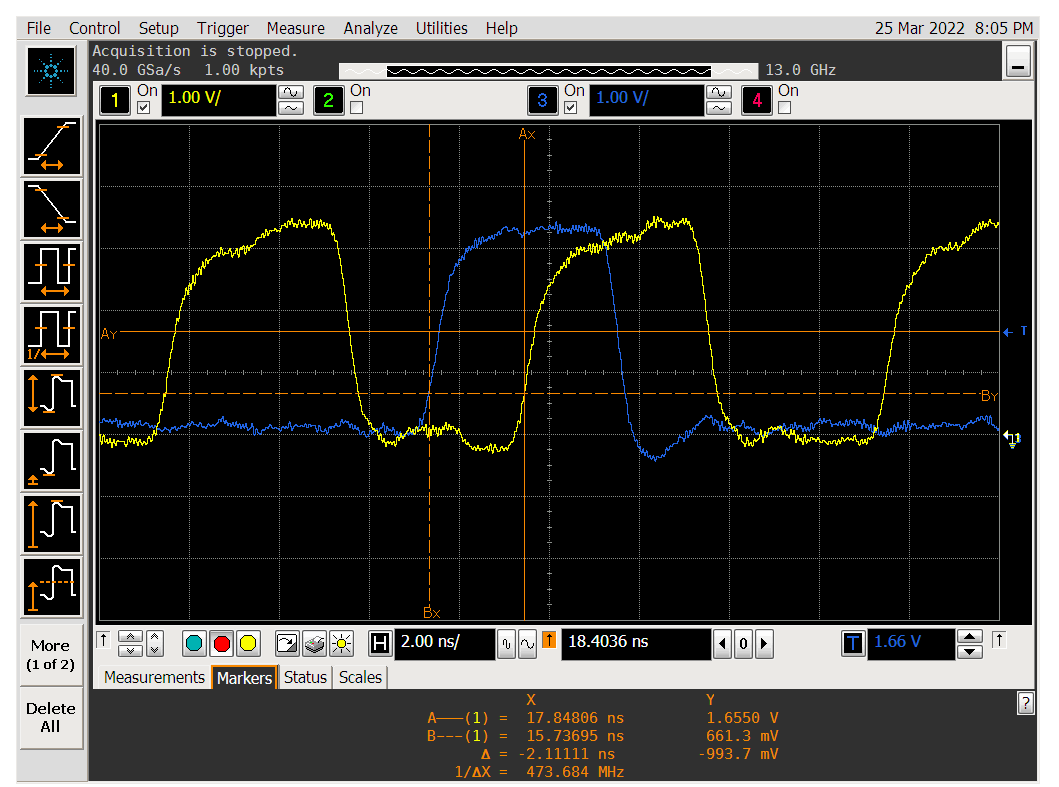
RX3&RXCLK：



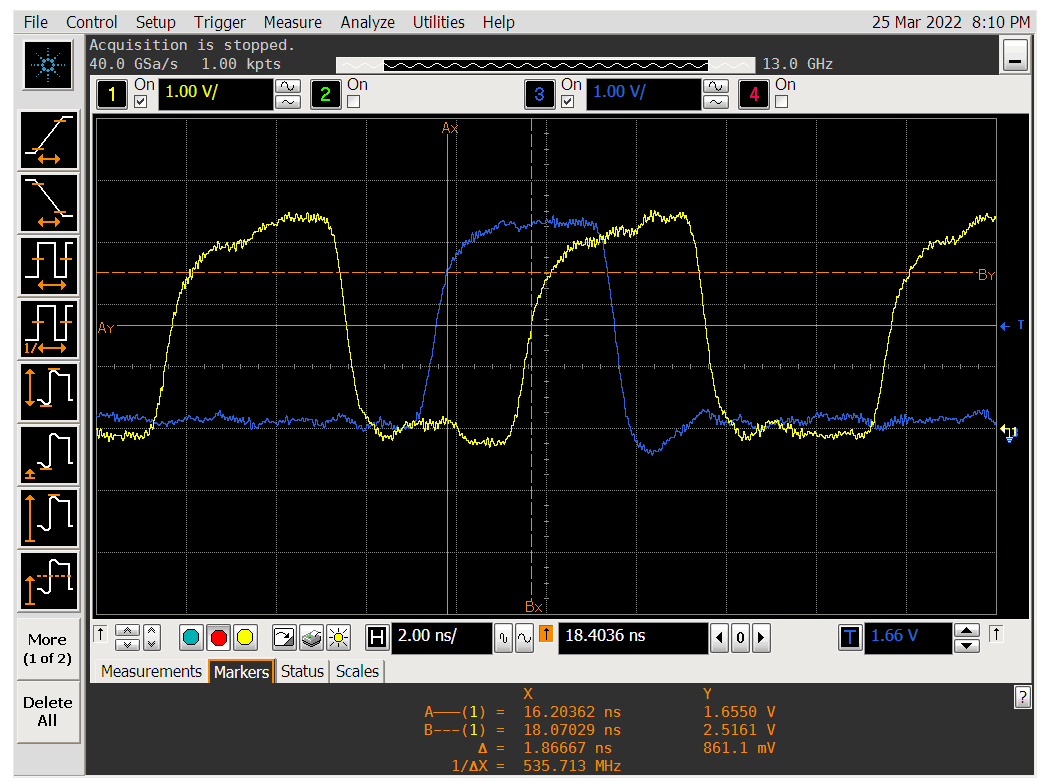
TX方向：(TX direction)

TX0&TXCLK的建立时间：低电平采样

Setup time of TX0 & TXCLK: low level sampling

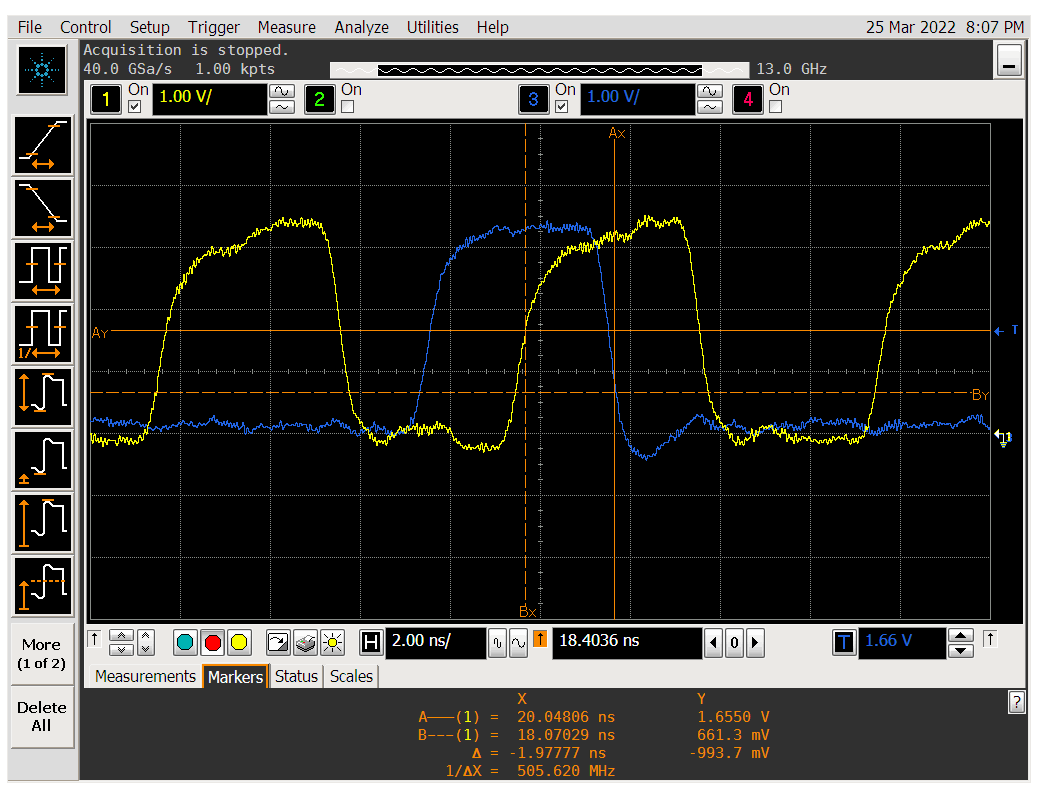


高电平采样High level sampling

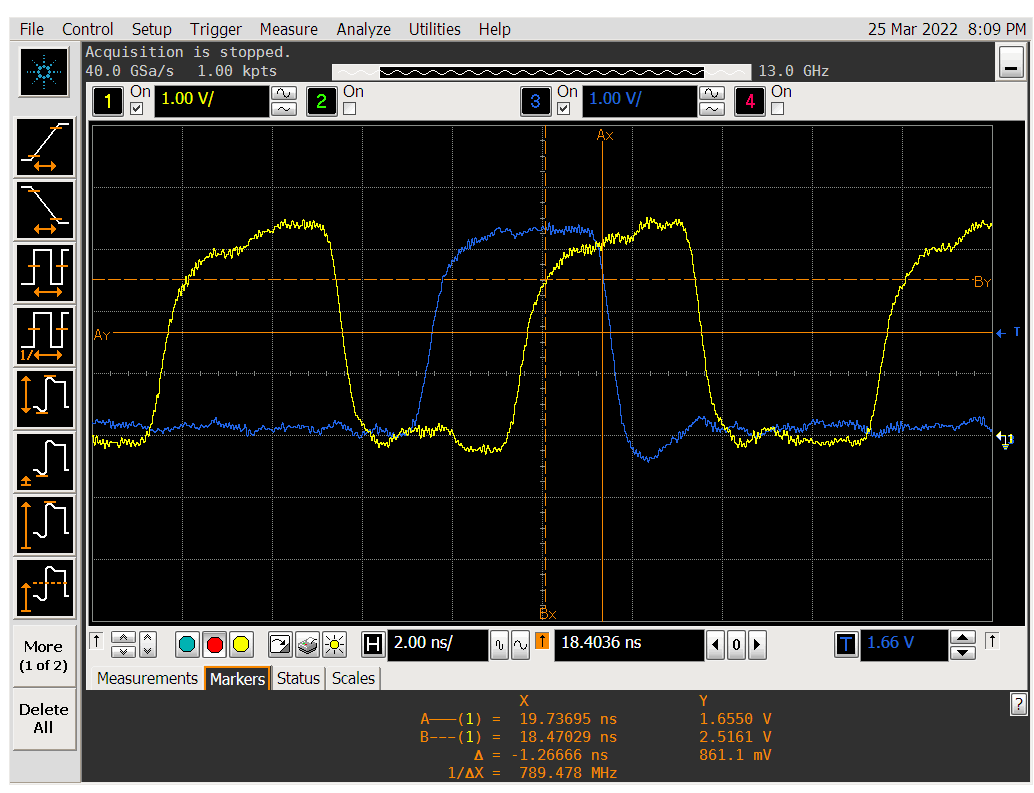


TX0&TXCLK的保持时间：Hold time of TX0&TXCLK:

低电平采样low level sampling

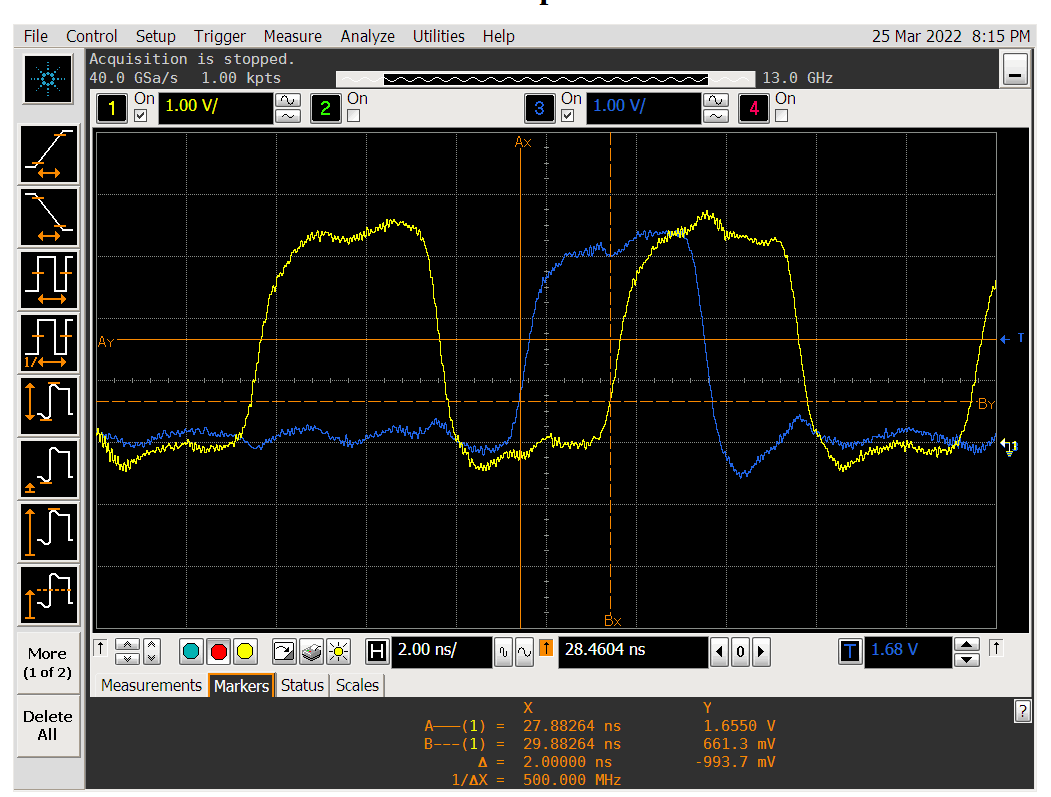


高电平采样：High level sampling:

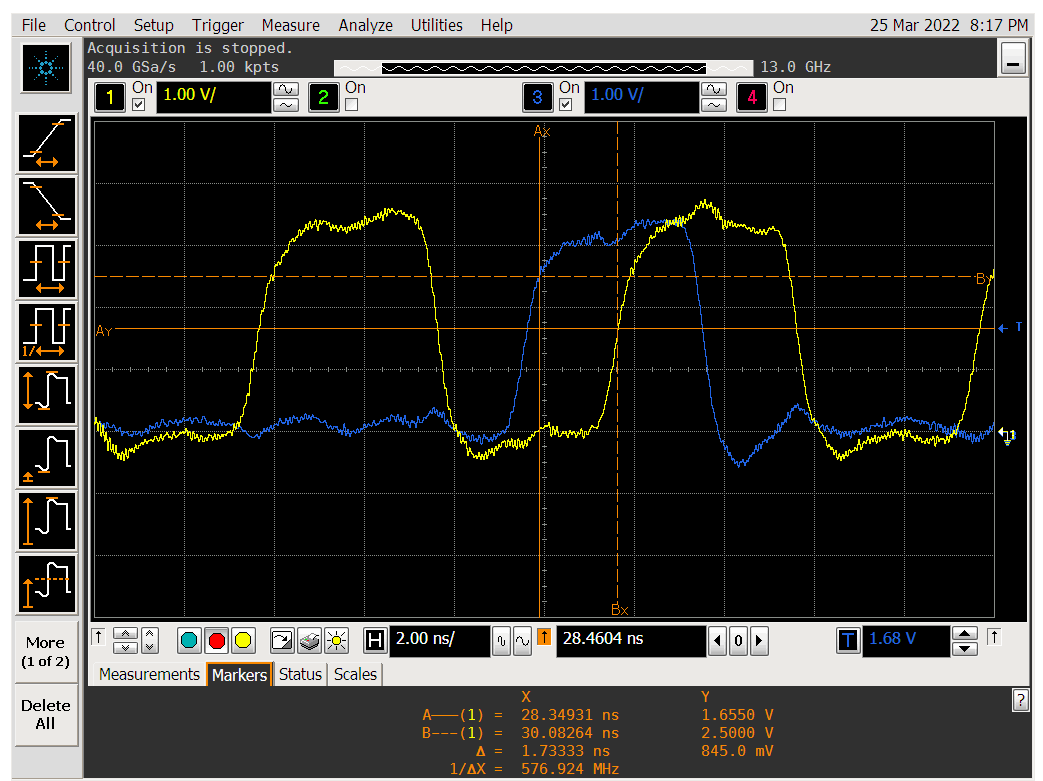


TX1&TXCLK的建立时间：Setup time of TX1 & TXCLK:

低电平采样：Low level sampling:

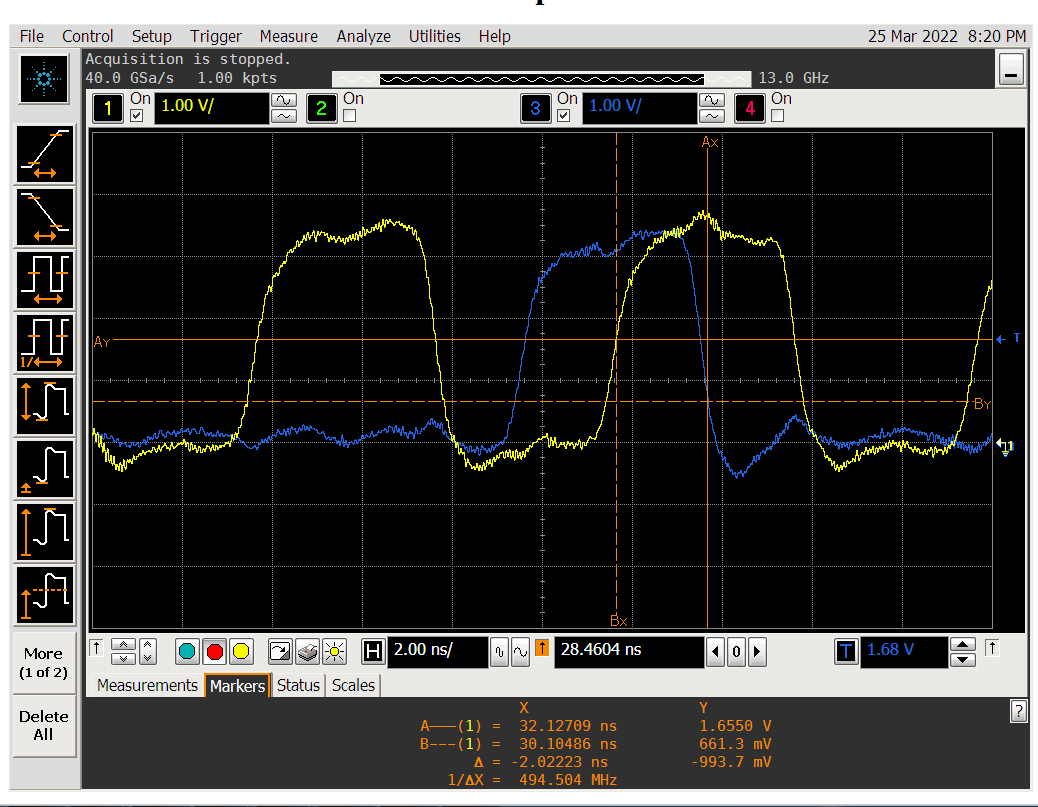


高电平采样：High level sampling:

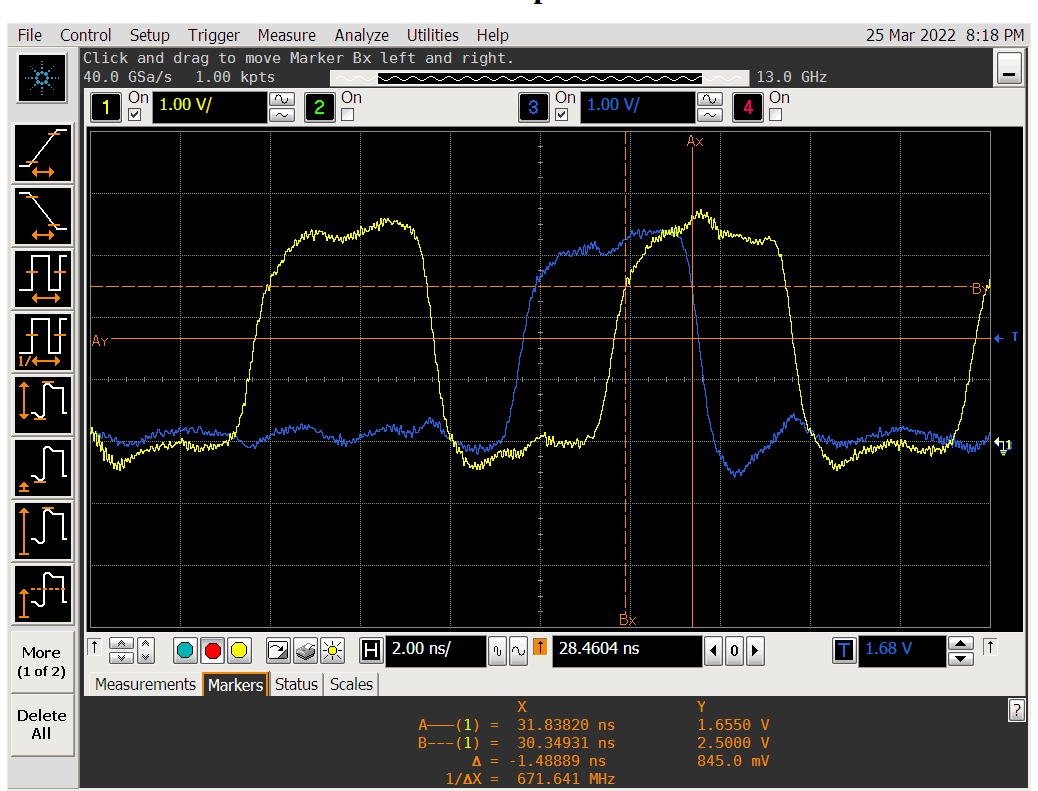


TX1&TXCLK的保持时间：Hold time of TX1&TXCLK:

低电平采样：Low level sampling:

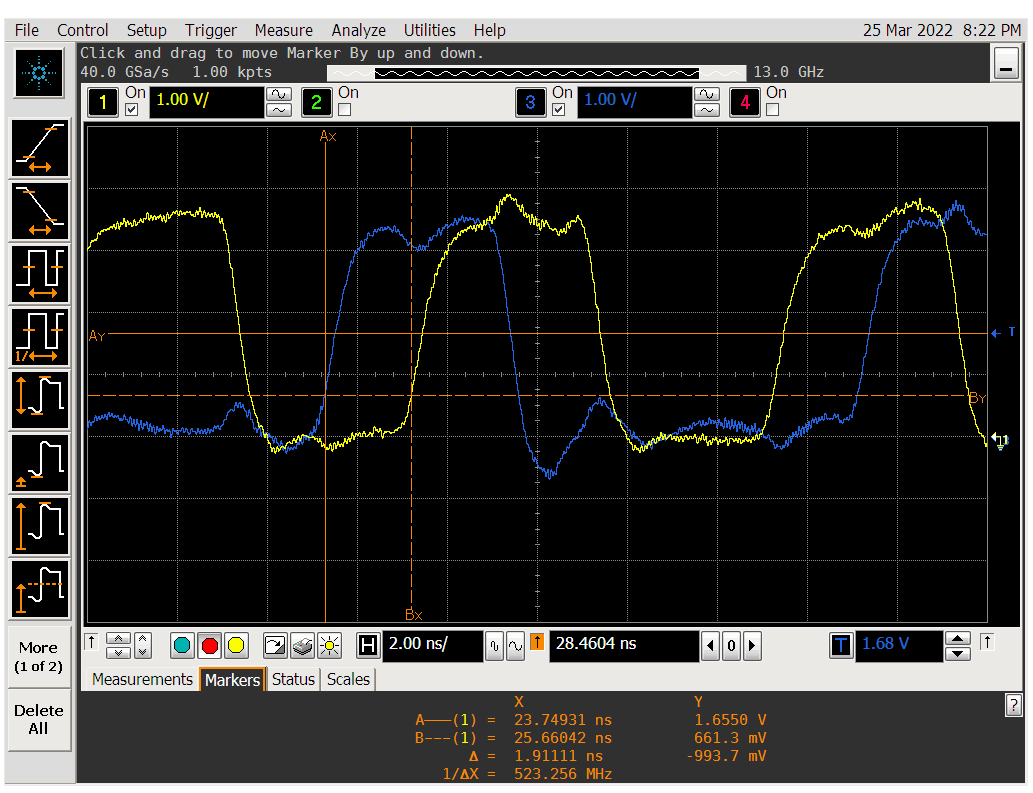


高电平采样：High level sampling:

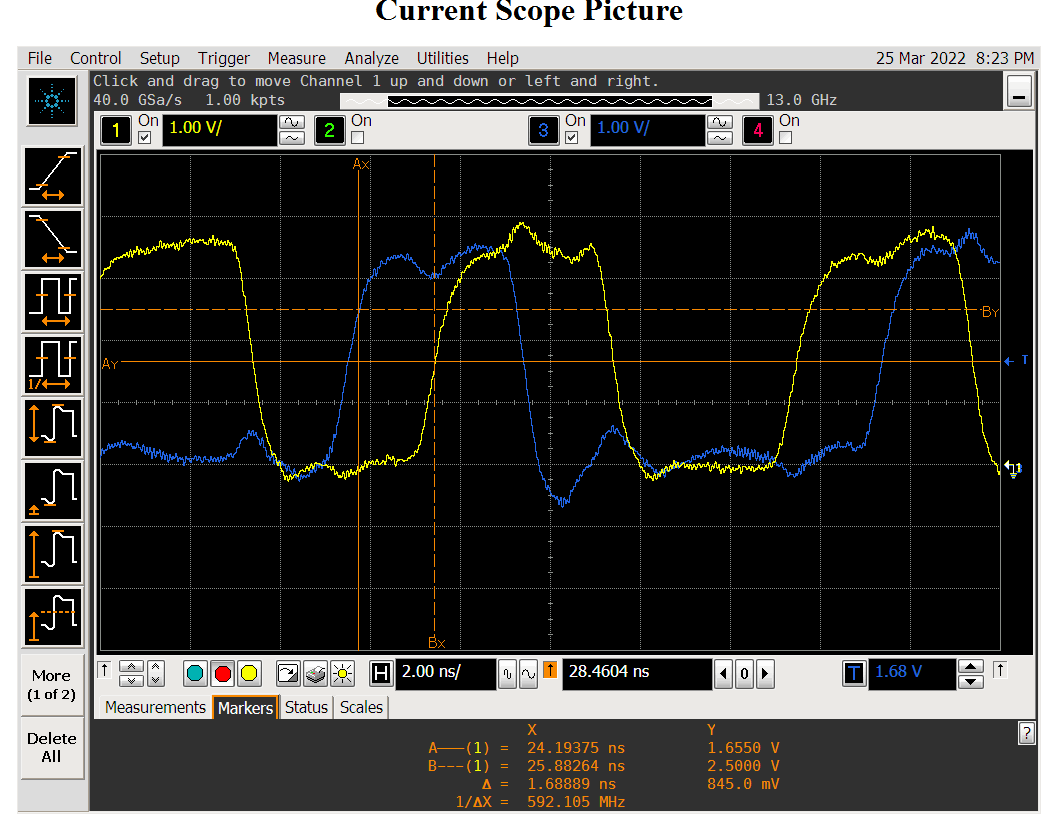


TX2&TXCLK的建立时间：Setup time of TX2 & TXCLK:

低电平采样：Low level sampling:

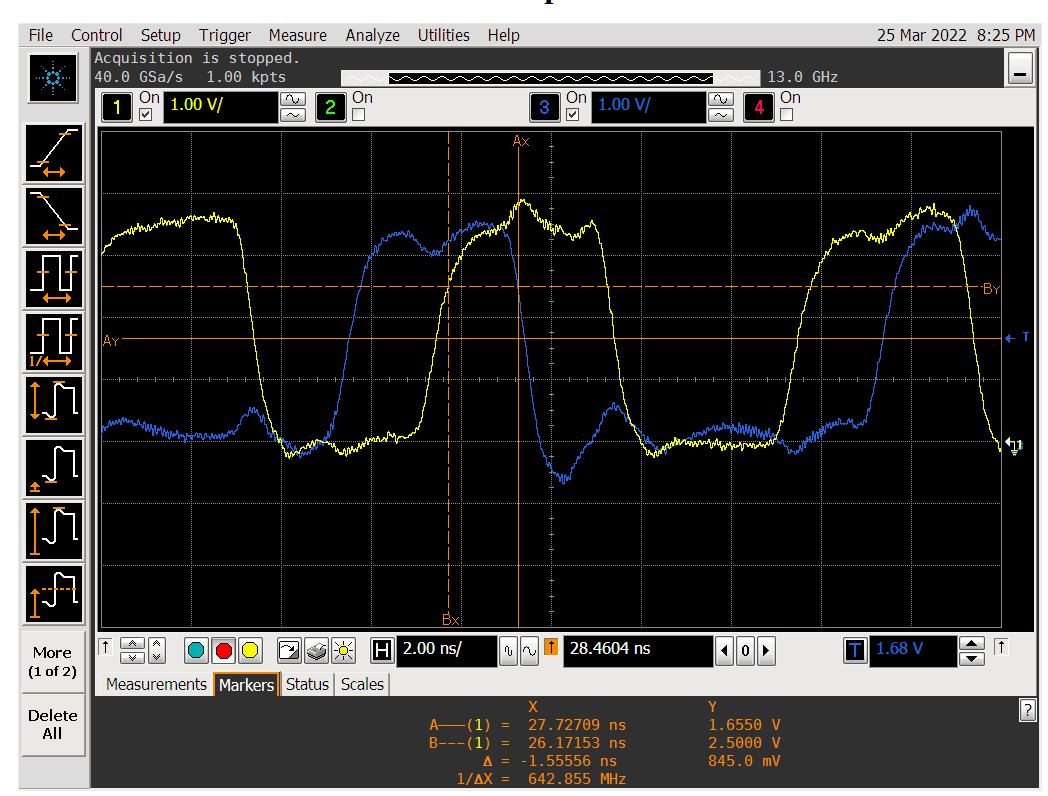


高电平采样：High level sampling:

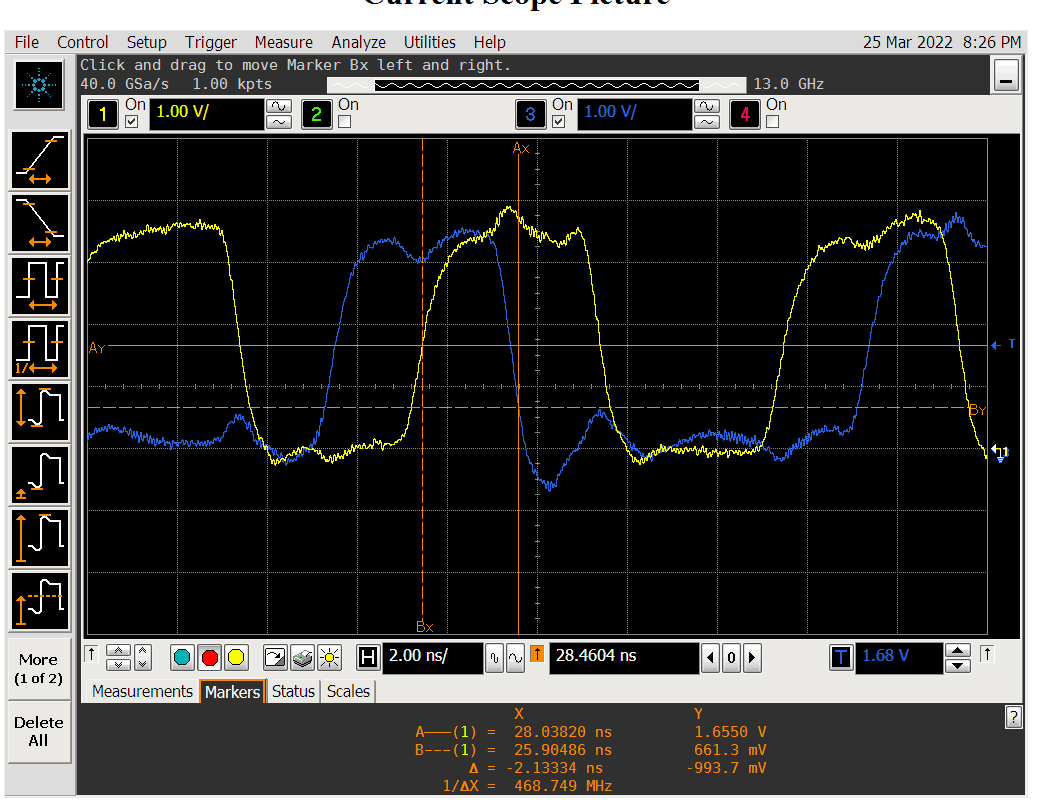


TX2&TXCLK的保持时间：Hold time of TX2&TXCLK:

高电平采样：High level sampling:



低电平采样：Low level sampling:



TX3&TXCLK的建立时间：Setup time of TX3 & TXCLK:

低电平采样：Low level sampling:

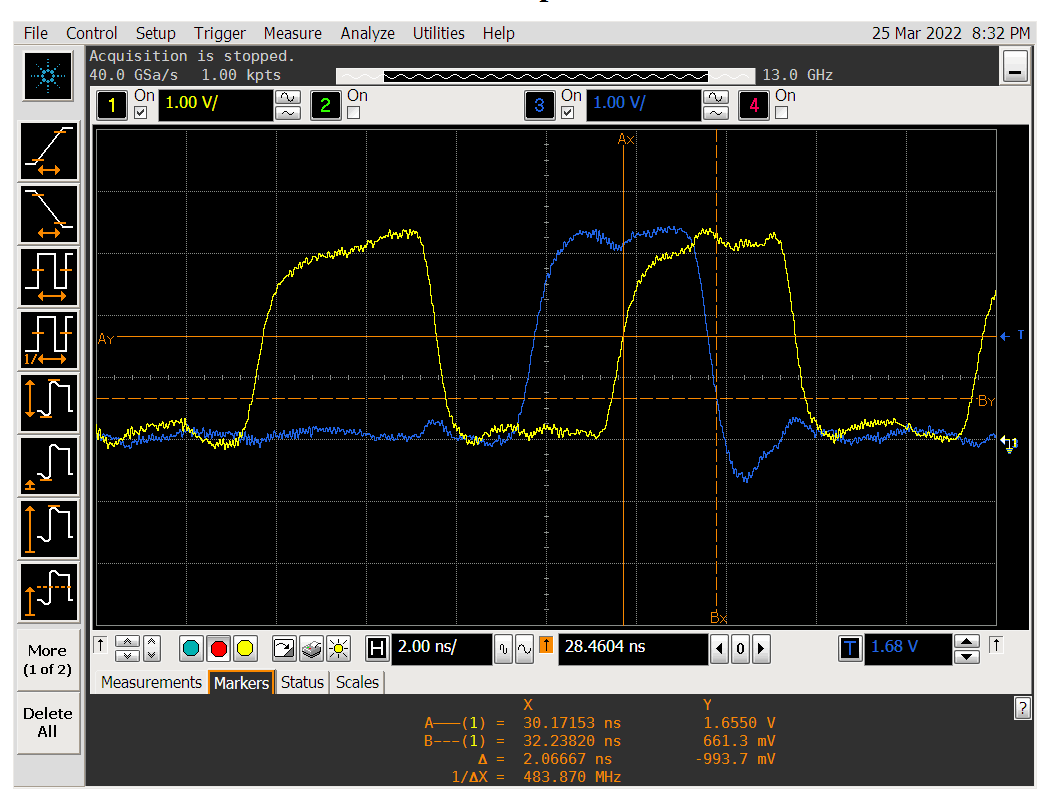


高电平采样：High level sampling:



TX3&TXCLK的保持时间：Hold time of TX3&TXCLK:

低电平采样：Low level sampling:



高电平采样：High level sampling:

