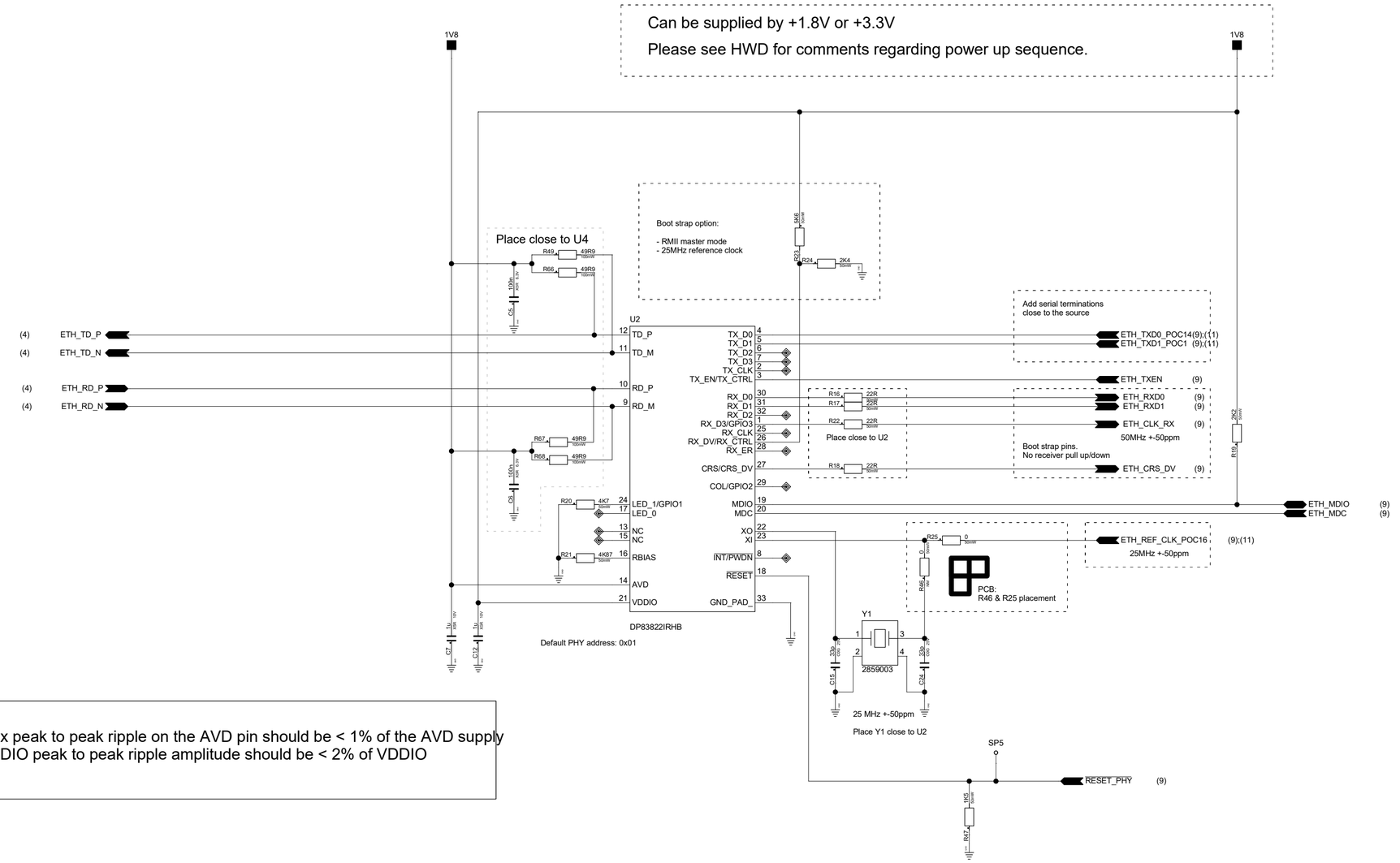
CONFIDENTIAL

RMII MASTER 0201 VERSION



TI:
Max peak to peak ripple on the AVD pin should be < 1% of the AVD supply
VDDIO peak to peak ripple amplitude should be < 2% of VDDIO

TAG106

If changes are made to the original reference design list them here

1. Used RMII 0201 version Master
2. Remove RJ45 con and Transformer / Caps to the power board

HWREF Rev: Mx.xx Copy Date: YYYY-MM-DD

3005036 HWREF PHY DP83822 MII RMII E2

AXIS COMMUNICATIONS

BOARD NAME: PCB ASS M3925-R MAIN	
SCHEMATIC: PHY	SHEET: 3 of 15
PART NO: 3177324	REV: M1
DESIGNER: Ted Sun	DATE: 2025/03/04

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3005036 HWREF PHY DP83822 MII RMI E2
(RMII Master mode, +1.8V I/O voltage)

PCB:
Place R2000
close to U1000

1.8V push-pull
Connect to CV75 pin L4

U1000

Default GPIO state during and after POR: No pull input
GPIO0-8 state after POR: Boot mode dependent
GPIO79-85 state after POR: Boot mode depedent

Gate 4 (7)
I/O
CV75

Default power region: (VDD18_A)

ETHERNET (VDD18_B)

K4	ENET_GTX_CLK	POC16			
M1	ENET_EXT_OSC_CLK				
H5	ENET_2ND_REF	POC6	GPIO78		
L6	ENET_TXD_0	POC14			
K5	ENET_TXD_1	POC1			
L5	ENET_TXD_2	POC2			
M4	ENET_TXD_3	POC3			
P3	ENET_TXEN				
N2	ENET_RXD_0				
N1	ENET_RXD_1				
P1	ENET_RXD_2				
N3	ENET_RXD_3				
L1	ENET_CLK_RX	(See the datasheet for complete mux options)			
K6	ENET_RXDV				
M3	ENET_MDC				
L2	ENET_MDIO				
J6	ENET_PTP_PPS	POC10			

VIDEO

	SSI3_SCLK	PWM4	TCC_WAVE_OUT[0]	SSI0_EN2	GPIO32	VSYNC0_OUT_0	B2
	SSI3_RXD	PWM5	TCC_WAVE_OUT[1]	SSI0_EN3	GPIO33	VSYNC0_OUT_1	B4
	SSI3_TXD	PWM6	TCC_MC0	SSI0_EN4	GPIO34	VSYNC0_OUT_2	C5
	SSI3_EN0	PWM7	TCC_MC1	SSI0_EN5	GPIO35	VSYNC0_OUT_3	D8
	SSIS_SCLK	PWM8	TCC_MC2	SSI0_EN6	GPIO36	HSYNC0_OUT_0	E7
	SSIS_TXD	PWM9	TCC_MC3	SSI0_EN7	GPIO37	HSYNC0_OUT_1	C11
	SSIS_RXD	PWM10	TCC_EV0	ENET_PHY_INTR	GPIO38	EXT_VSYNC_IN	D7
	SSIS_EN	PWM11	TCC_EV1	WDT_EXT_RST_L	GPIO39	EXT_HSYNC_IN	D10
(VDD18_B)					GPIO90	SENSOR_RST	P2
(VDD18_B)	POC20	VIN0_STRIG0	IDSPV0_IOPAD_VIN5_MASTER_HSYNC		GPIO91	SHSYNC	T4
(VDD18_B)	POC19	VIN0_STRIG1	IDSPV0_IOPAD_VIN5_MASTER_VSYNC		GPIO92	SVSYNC	V3
						CLK_SI	D6

HEATER_CTRL (7)
NETWORK_BOOT (4)
POC20 (11)
POC19 (11)
CLK_SI (6)

1V8 1V8 1V8 1V8
H5 H5 H5 H5
R2106 R2105 R2084 R2085

NOTE
Pull-up values may need
to be changed depending on
the layout.

I2C

			IDCS_CLK	GPIO86	IDC_CLK
			IDCS_DATA	GPIO87	IDC_DATA
		VIN0_STRIG0	TM11_CLK	GPIO88	IDC2_CLK
		VIN0_STRIG1	ENET_PHT_INTR	GPIO89	IDC2_DATA

A14 RTC_SECURE-ELEMENT_SCL (12);(8)
B15 RTC_SECURE-ELEMENT_SDA (12);(8) SECURE ELEMENT & RTC only
A13
B14
I2C2_SCL (6)
I2C2_SDA (6) Image sensor

ADC (AVDD33)

		TCC_EV1	PWM4	IDCS_CLK	GPIO19		
	POC4	TCC_WAVE_OUT[0]	PWM5	WDT_EXT_RST_L	GPIO20	SSI0CLK	T1
		TCC_MC0	PWM6	IDCS_DATA	GPIO21	SSI0MOSI	T2
		TCC_MC1	PWM7	IDC1_DATA	GPIO22	SSI0MISO	N5
		TCC_MC2	PWM8	IDC1_CLK	GPIO23	SSI0EN0	R3
						SSI0EN1	R4
		SSIS_SCLK	PWM9	IDC3_CLK	GPIO24	SSI1CLK	T3
		SSIS_TXD	PWM10	IDC3_DATA	GPIO25	SSI1MOSI	V1
		SSIS_RXD	PWM11	VIN0_STRIG0	GPIO26	SSI1MISO	U1
		SSIS_EN	WDT_EXT_RST_L	VIN0_STRIG1	GPIO27	SSI1EN0	V2
	POC5		UART3_AHB_RTS_N	SSIS_SCLK	GPIO28	SSI2CLK	U2
			UART3_AHB_TX	SSIS_TXD	GPIO29	SSI2MOSI	W2
			UART3_AHB_RX	SSIS_RXD	GPIO30	SSI2MISO	U4
			UART3_AHB_CTS_N	SSIS_EN	GPIO31	SSI2EN0	U3

POC4 (11)
AXIS_CTRL_BTN (4)
SENSOR_RESET_1.8V (6)
POC5 (11)
MIC_EN (4)

REF (AVDD18_A)

SSIO (VDD18_B)

PWM

	POC18	TCC_WAVE_OUT[0]	IDSPV0_IO-PAD_VIN5_MASTER_HSYNC	SSI3_SCLK	GPIO40	PWM0	D14
	POC31	TCC_WAVE_OUT[1]	IDSPV0_IO-PAD_VIN5_MASTER_VSYNC	SSI3_TXD	GPIO41	PWM1	D16
	POC17	TCC_WAVE_OUT[2]		SSI3_EN0	GPIO42	PWM2	E16
	ENET_PHY_INTR	TCC_WAVE_OUT[3]	TM11_CLK	SSI3_RXD	GPIO43	PWM3	D15

POC18 (11)
POC31 (11)
POC17 (11)

SMIO

IDSPV0_IO-PAD_VIN5_MASTER_HSYNC	UART2_AHB_RX	NORSPI_CLK	SNAND_SCK	GPIO79	SMIO_0	C10
IDSPV0_IO-PAD_VIN5_MASTER_VSYNC	UART2_AHB_TX	NORSPI_EN	SNAND_CS_N	GPIO80	SMIO_1	C9
SSIS_CLK	UART2_AHB_CTS_N	NORSPI_DQ[0]	SNAND_SI[0]	GPIO81	SMIO_2	B5
SSIS_TXD	UART2_AHB_RTS_N	NORSPI_DQ[1]	SNAND_SI[1]	GPIO82	SMIO_3	B12
SSIS_RXD	WDT_EXT_RST_L	NORSPI_DQ[2]	SNAND_SI[2]	GPIO83	SMIO_4	A10
SSIS_EN	ENET_PHY_INTR	NORSPI_DQ[3]	SNAND_SI[3]	GPIO84	SMIO_5	D12
WDT_EXT_RST_L	VPP_EN	NORSPI_DQS	TM11_CLK	GPIO85	SMIO_6	D13

LED0_GREEN (4)
LED0_RED (4)

UART

			VIN0_STRIG0	GPIO44	UART_APB_RX	M6	
			VIN0_STRIG1	GPIO45	UART_APB_TX	N4	
(VDD18_B)	POC15			GPIO46	UART0_AHB_RX	R2	
	POC13	IDSPV0_IO-PADD_VIN5_MASTER_HSYNC	UART1_AHB_RX	GPIO47	UART0_AHB_TX	M5	
	TCC_MC0	IDSPV0_IO-PADD_VIN5_MASTER_VSYNC	UART1_AHB_TX	GPIO48	UART0_AHB_CTS_N	R1	
	TCC_MC1	IDC3_CLK	UART1_AHB_CTS_N	GPIO49	UART0_AHB_RTS_N	P4	
		IDC3_DATA	UART1_AHB_RTS_N				
	TCC_MC2	SSIS_SCLK	UART1_AHB_RX	GPIO50	CAN0_RX	D4	
	TCC_MC3	SSIS_TXD	UART1_AHB_TX	GPIO51	CAN0_TX	D5	
(VDD18_A)	TCC_EV0	SSIS_RXD	VIN0_STRIG0	GPIO52	CAN1_RX	E6	
	TCC_EV1	SSIS_EN	VIN0_STRIG1	GPIO53	CAN1_TX	D3	

UART_APB_RX (4)
UART_APB_TX_POC15 (11);(4)
POC13 (11)

AUDIO

			DMIC_CLK	GPIO54	I2S_CLK	A4	
			DMIC_DAT	GPIO55	I2S_SI_0	A12	
			DMIC_DAT_OUT	GPIO56	I2S_SO_0	C13	
				GPIO57	I2S_WS	C14	
	TCC_MC0	IDC3_CLK	SSI3_SCLK	GPIO58	I2S1_CLK	A5	
	TCC_MC1	IDC3_DATA	SSI3_RXD	GPIO59	I2S1_SI_0	B11	
	TCC_EV0	IDCS_CLK	SSI3_TXD	GPIO60	I2S1_SO_0	A3	
	TCC_EV1	IDCS_DATA	SSI3_EN0	GPIO61	I2S1_WS	A11	
	POC8	CLK_AU3	CLK_AU2		CLK_AU	B3	

22R R2071
DMIC_CLK (4)
DMIC_DAT (4) PDM microphones

POC8 (11)

Internal PU is 10.4 k to 20.5 k
Internal PD is 34.4 k to 87 k

3142640
CV75S66

(11) POC6
(11) POC2
(11) POC3
(11) POC10
(3);(9);(11) ETH_REF_CLK_POC16
(3);(9);(11) ETH_TXD0_POC14
(3);(9);(11) ETH_TXD1_POC1

(3);(9);(11) ETH_REF_CLK_POC16 — 22R R2000
(3);(9);(11) ETH_TXD0_POC14 — 22R R2055
(3);(9);(11) ETH_TXD1_POC1 — 22R R2056
(3) ETH_TXEN — 22R R2057
(3) ETH_RXD0
(3) ETH_RXD1
(3) ETH_CLK_RX
(3) ETH_CRS_DV
(3) ETH_MDC — 22R R2059
(3) ETH_MDIO — 22R R2058
(3) RESET_PHY

(12) RESET_SECURE-ELEMENT — IR_IN GPIO18 VPP_EN TM11_CLK TCC_EV0 ENET_PHY_INTR IR

(7) NTC_MAIN — C2 ADC_CH_1
(6) NTC_SENSOR — C1 ADC_CH_2

PCB:
SP10 close to CV75

SP10
R2070 10K
D2 BG0_REXT

SD (SD_DVDD)

(11)	EMMC_DATA_0	22R R2051	H6	SD_D0	GPIO0	
(11)	EMMC_DATA_1	22R R2052	K3	SD_D1	GPIO1	
(11)	EMMC_DATA_2	22R R2053	J4	SD_D2	GPIO2	
(11)	EMMC_DATA_3	22R R2054	G5	SD_D3	GPIO3	
(11)	EMMC_CLK	22R R2066	G4	SD_CLK	GPIO4	
(11)	EMMC_CMD	22R R2067	G6	SD_CMD	GPIO5	
(11)	EMMC_DS		E3	SD_CD	GPIO6	
		SP11	F5	SD_WP	GPIO7	
(11)	EMMC_RST_N		E4	SD_RESET	GPIO8	
			L4	SD_HS_SEL	GPIO93	(VDD18_B)

State after POR:
Boot mode dependent

NOTE:
- If CV75 internal pull-ups are enabled the external may be removed.
- SDIO0_WP could be configured as GPIO input mode with default low in SD when using a uSD-card holder.

SDIO (SDIO0_DVDD)

(5)	SDIO1_0	22R R2060	K1	SDIO0_D0	GPIO9	
(5)	SDIO1_1	22R R2061	K2	SDIO0_D1	GPIO10	
(5)	SDIO1_2	22R R2062	J3	SDIO0_D2	GPIO11	
(5)	SDIO1_3	22R R2063	J5	SDIO0_D3	GPIO12	
(5)	SDIO1_CLK	22R R2064	H4	SDIO0_CLK	GPIO13	
(5)	SDIO1_CMD	22R R2065	H3	SDIO0_CMD	GPIO14	
(5)	SDIO1_CD		F3	SDIO0_CD	GPIO15	
			F4	SDIO0_WP	GPIO16	
(5)	SDCARD_PWR_OFF		F6	SDIO0_RESET	CPIO17	
			L3	SDIO0_HS_SEL	GPIO94	(VDD18_B)

1907821 HWREF SD-CARD NORM HIGH WT48 E2

USB

(11)	USB_DP	A9	USB_DP0		
(11)	USB_DM	B9	USB_DM0		
(11)	DETECT_VBUS	C12	DETECT_VBUS_0		
		B10	USB_REXT0		
		A6	USB32P0_CMN_REFCLK_M		
		B6	USB32P0_CMN_REFCLK_P		
		B7	USB32P0_TX_M_LN_0		
		A7	USB32P0_TX_P_LN_0		
		B8	USB32P0_RX_M_LN_0		
		A8	USB32P0_RX_P_LN_0		
		D11	USB32_OVERC_0		
		C4	USB32_DRIVE_BUS_0		
		C6	USB32P0_CMN_REXT		

200R R2072

Part of layout reference

X-TAL (AVDD18_A)

C3	XIN	
D1	XOUT	

R2068 1M
R2069 0
Y2000 2098794 24MHz 10PF
ST2000 NM
C2000 15p C0G 50V
C2001 15p C0G 50V

U1000

Default GPIO state during and after POR: No pull input
*check system HW doc

Gate 6 (7)
MCU
CV75

Default power region:
(VDD18_CMVI)

(13);(7) CV75_RESET — T15 VI_PI_POR_L
U14 VI_CMVI_POR_L

			GPIO8	VI_WIFI_WAKEUP	U13
	VI_IDC_CLK		GPIO0	VI_SSI_CLK	R5
	-		GPIO1	VI_SSI_TX	P6
	VI_IDC_DATA		GPIO2	VI_SSI_RX	R6
	-		GPIO3	VI_SSI_EN0	N6
	VI_WDT_EXT_RST_L		GPIO4	VI_SSI_EN1	L7
			GPIO9	VI_VBUS	P5
			GPIO10	VI_IMU_TRIGGER	U7
	PWR_SEQ0		GPIO5	* VI_PMU_ENABLE	T6
	PWR_SEQ1		GPIO6	VI_PMU_WAKEUP	M7
	PWR_SEQ2		GPIO7	VI_PMU_IRQ	T5

(12) JTAG_TCK — T13 VI_JTAG_CLK
(12) JTAG_RST — T12 VI_JTAG_RST_L
(12) JTAG_TDI — T11 VI_JTAG_TDI
(12) JTAG_TDO — T10 VI_JTAG_TDO
(12) JTAG_TMS — T9 VI_JTAG_TMS

V15 VI_XI_RTC
V14 VI_XO_RTC
U10 VI_TEST_MODE

Internal PU is 10.4 k to 20.5 k
Internal PD is 34.4 k to 87 k

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CV75S66

TAG2000

If changes are made to the original reference design list them here

1. Reserve PU/PD on POC
2. S2000 change to right angle
3. X2000 change to right angle
4. JATG con change to TP
5. Netboot button/ Debug con move to power board
6. Using PMOS to control 3V3 because exist of 3V3_PRE for heater
7. Add anti-leakage for 1V8 as singoalla.
8. U2007 input change to 3V3_PRE for higher efficiency
9. U2005 input link to 3V3_PRE and EN to EN3
10. For secure boot
S2000 deleted and reserved TP205 as limited space

HWREF Rev: M1.11 Copy Date: 2025-01-01

3125964 HWREF CV75 BASIC COMP E1

AXIS COMMUNICATIONS

BOARD NAME: PCB ASS M3925-R MAIN

SCHEMATIC: HWREF CV75 BASIC COMP - GPIO	SHEET: 9 of 15
PART NO: 3177324	REV: M1
DESIGNER: Ted Sun	DATE: 2025/03/04