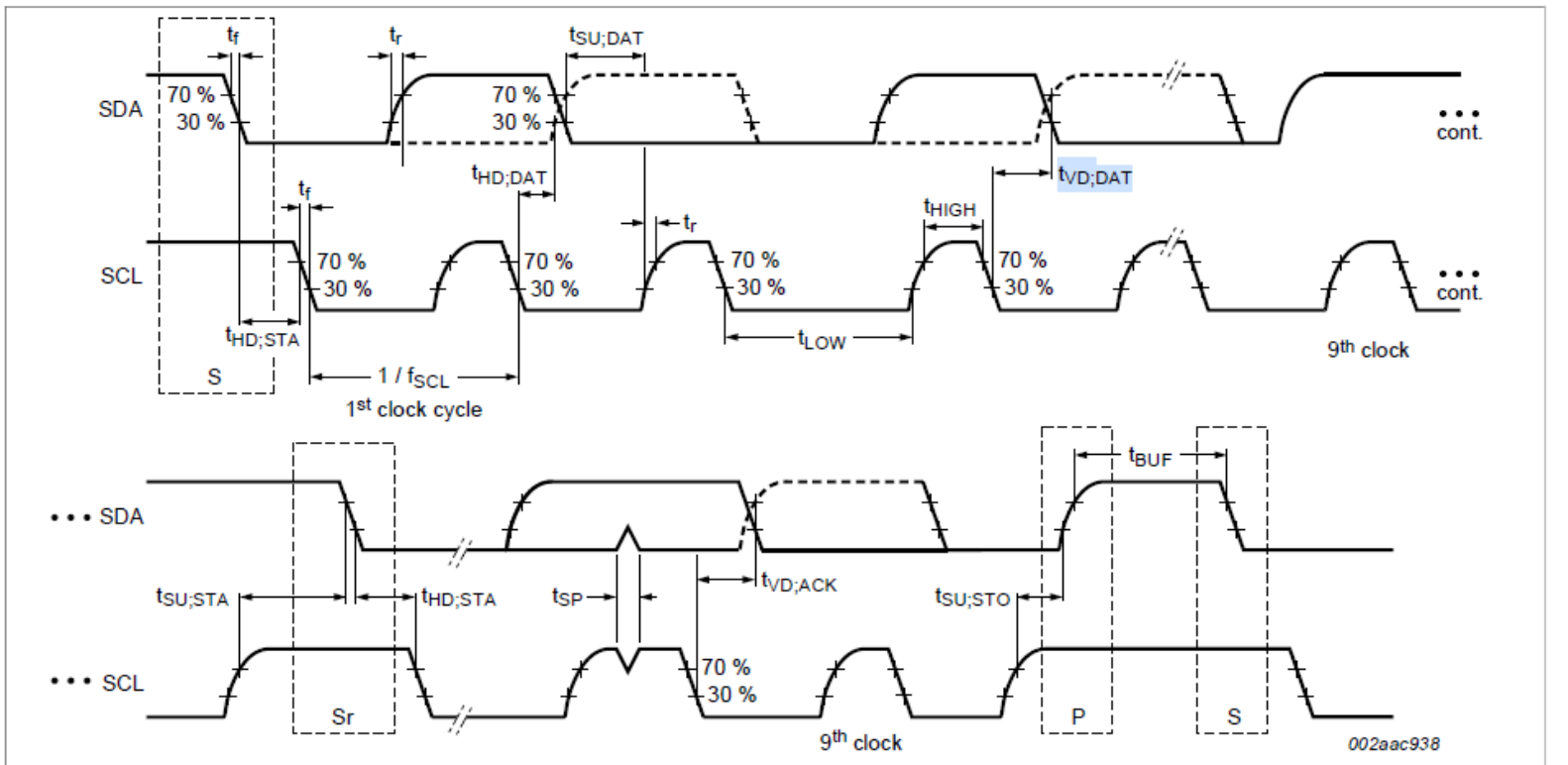
MCU-TCAL6416_I2C_Timing Spec

[8] Necessary to be backwards compatible to Fast-mode.
[9] The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application. Section 7.2 discusses techniques for coping with higher bus capacitances.
[10] $t_{VD;DAT}$ = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
[11] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).



$V_{IL} = 0.3V_{DD}$
$V_{IH} = 0.7V_{DD}$

Figure 38. Definition of timing for F/S-mode devices on the I^2C-bus

Symbol	Parameter	Conditions	Standard-mode		Fast-mode		Fast-mode Plus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency		0	100	0	400	0	1000	kHz
$t_{HD;STA}$	hold time (repeated) START condition	After this period, the first clock pulse is generated.	4.0	-	0.6	-	0.26	-	µs
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time [1]	CBUS compatible controllers (see Remark in Section 4.1)	5.0	-	-	-	-	-	µs
		I^2C-bus devices	0 [2]	- [3]	0 [2]	- [3]	0	-	µs
$t_{SU;DAT}$	data set-up time		250	-	100 [4]	-	50	-	ns
t_r	rise time of both SDA and SCL signals		-	1000	20	300	-	120	ns
t_f	fall time of both SDA and SCL signals [2] [5] [6] [7]		-	300	20 × (V_{DD} / 5.5 V)	300	20 × (V_{DD} / 5.5 V) [8]	120 [7]	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
C_b	capacitive load for each bus line [9]		-	400	-	400	-	550	pF
$t_{VD;DAT}$	data valid time [10]		-	3.45 [3]	-	0.9 [3]	-	0.45 [3]	µs
$t_{VD;ACK}$	data valid acknowledge time [11]		-	3.45 [3]	-	0.9 [3]	-	0.45 [3]	µs
V_{nL}	noise margin at the LOW level	for each connected device (including hysteresis)	0.1V_{DD}	-	0.1V_{DD}	-	0.1V_{DD}	-	V
V_{nH}	noise margin at the HIGH level	for each connected device (including hysteresis)	0.2V_{DD}	-	0.2V_{DD}	-	0.2V_{DD}	-	V

[1] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
[2] Ensure SCL drops below 0.3V_{DD} on falling edge before SDA crosses into the indeterminate range of 0.3 V_{DD} to 0.7 V_{DD}.
NOTE: For controllers that cannot observe the SCL falling edge then independent measurement of the time for the SCL transition from static high (V_{DD}) to 0.3 V_{DD} should be used to insert a delay of the SDA transition with respect to SCL.
[3] The maximum $t_{HD;DAT}$ could be 3.45 µs and 0.9 µs for Standard-mode and Fast-mode, but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.

[4] A Fast-mode I^2C-bus device can be used in a Standard-mode I^2C-bus system, but the requirement $t_{SU;DAT}$ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I^2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

[5] If mixed with Hs-mode devices, faster fall times according to Table 10 are allowed.

Question

1）According to the UM10204,

the case of writing from MCU --> TCAL6416, tVD;DAT is the maximum delay of the data from the falling edge of the clock signal.

And the tVD;DAT must be less than the half period of the clock period for adhereing the set-up time before it releases the data.

My understanding is correctly?

2）Is the I2C of the TCAL6461 designed follow the UM10204.pdf ?