MDIO interface Access Issue Debug

Version 0.1

18 Nov 2022

Overview

We are facing inconsistency in the 1GE local management port with 4 Radio boards.
The issue is not seen with other Radio boards (more than 30 boards)

On testing on these boards we are finding intermittent failures in the MDIO read access on these boards.
We suspect that MDIO access failures is causing the 1GE Ethernet link to fail.

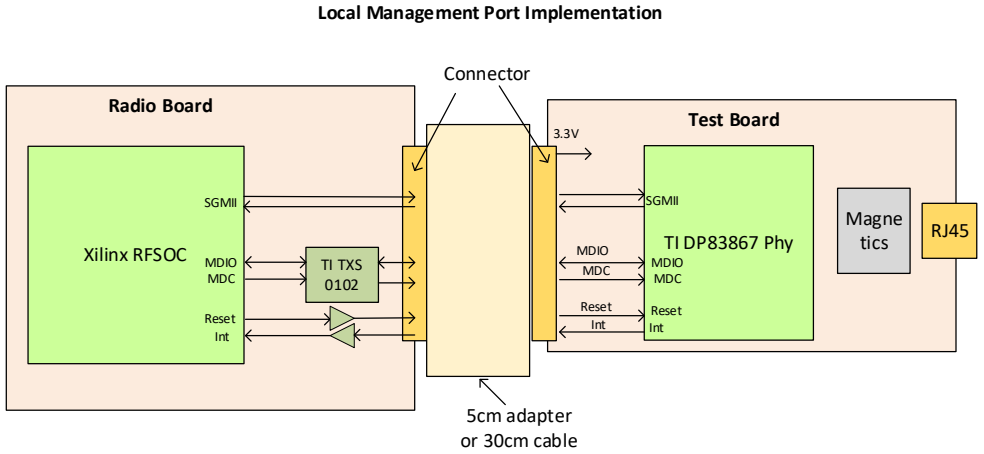
On comparing the MDIO read access waveform in Pass and Fail case, we find that during the turnaround time (duration between RFSOC driving and TI Phy there is a difference. [Details in subsequent slides]

The TI phy device seems to have started driving seems to have started driving the Read register value one clock cycle early

We require specifications of Xilinx ZU67 RFSIC and Phy device during turn around time for MDIO read access.

Overview

The 1GE Local Management port is implemented as shown to the right



The MDIO read access waveform from TI DP83867 Phy datasheet is shown to the right.

Note that there are two clock cycles for turn around time before the Phy starts driving the Read Register daa on the MDIO line

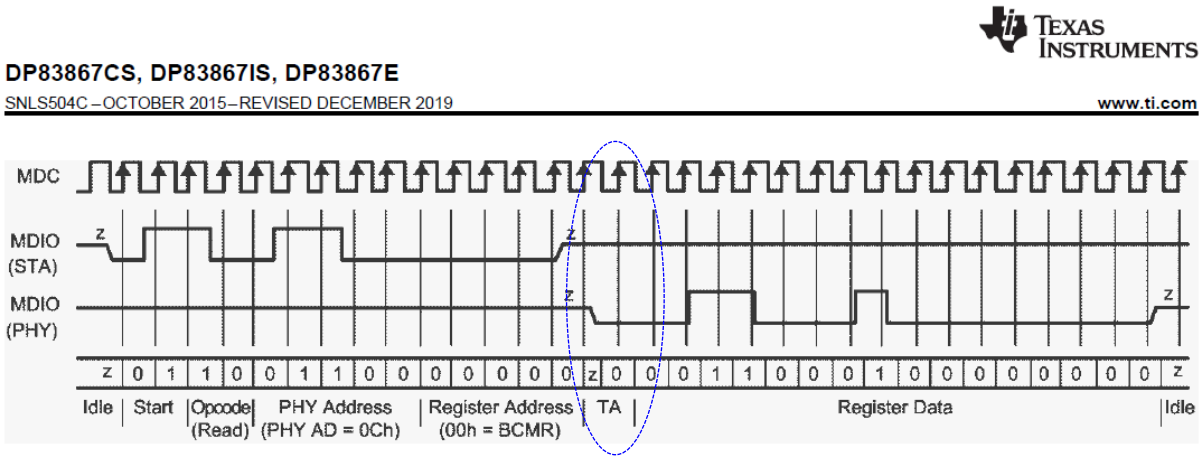
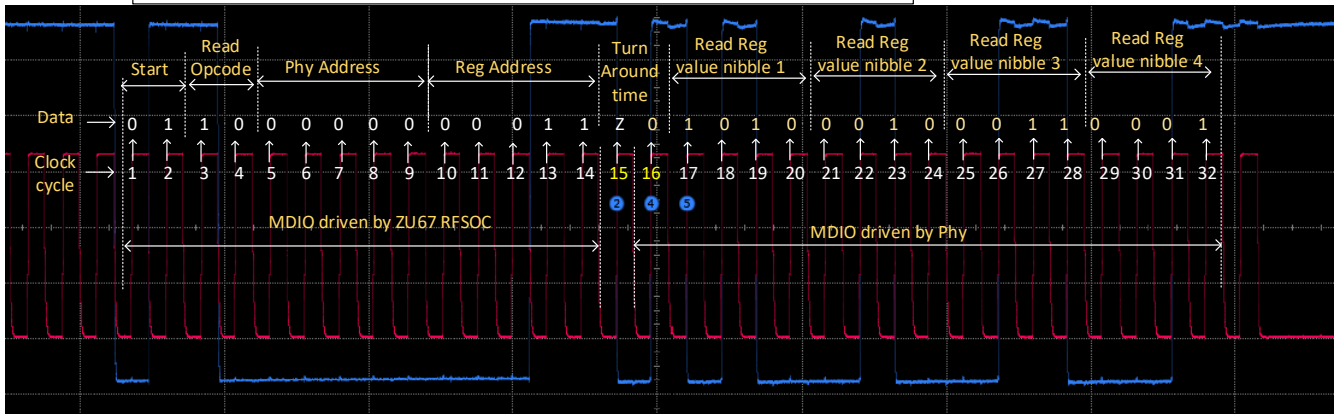


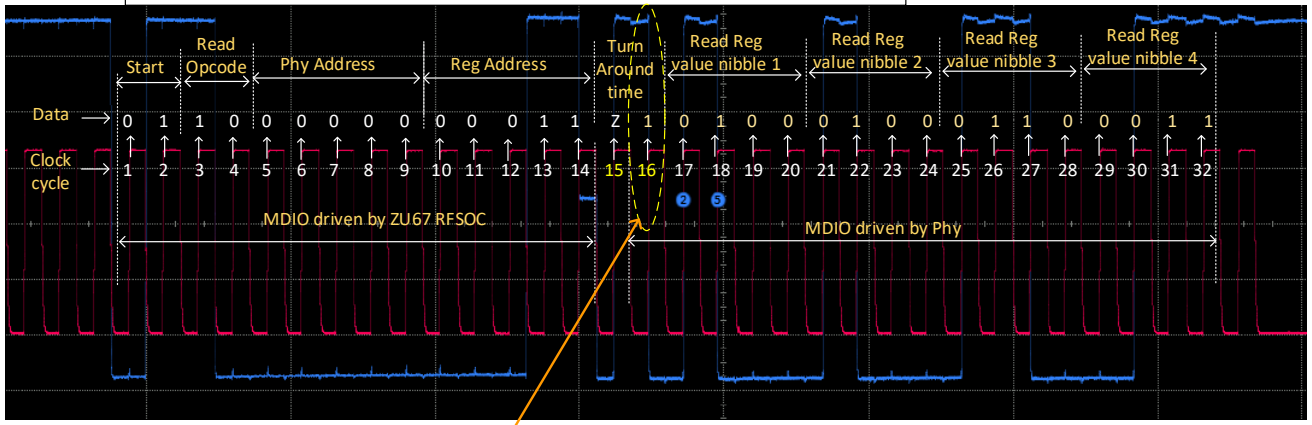
Figure 17. Typical MDC/MDIO Read Operation

MDIO access PHYID2 read waveform for Passing vs Failing case

Pass Case: Phy ID2: 9Nov: MDIO_PHYID2 read_JP178_30cm HDMI CABLE_@ uBOOT_2.pdf



Fail Case: Phy ID2: 9Nov: MDIO_PHYID2_ZU67 READ FAIL_JP178_HDMI ADAPTER.pdf



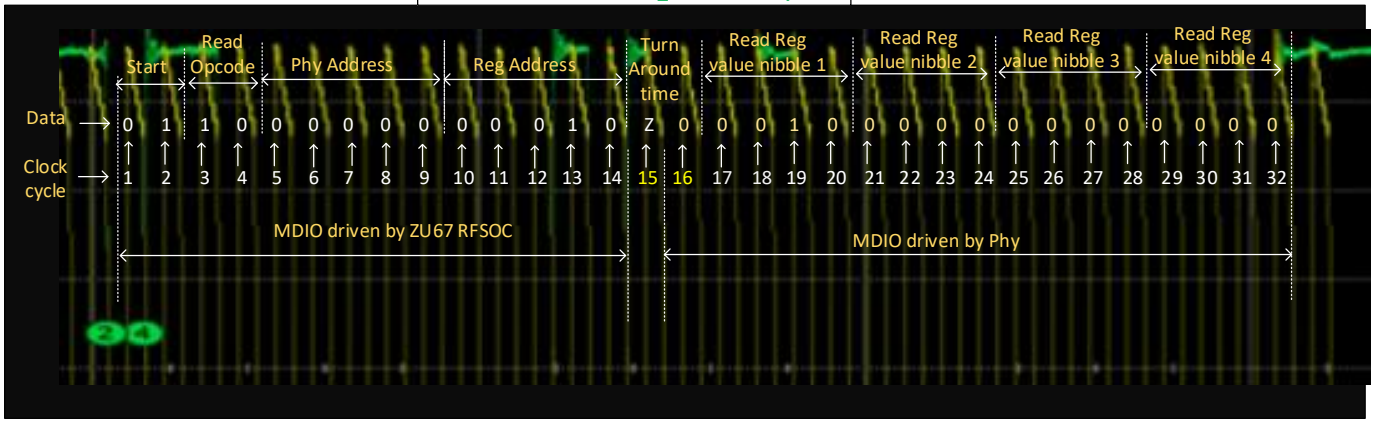
<u>MDIO read access to PHYID2 register</u>
Register address: 0x3
Register data: 0xA231

In fail case value read is 0x4463
(bits shifted to left by 1)

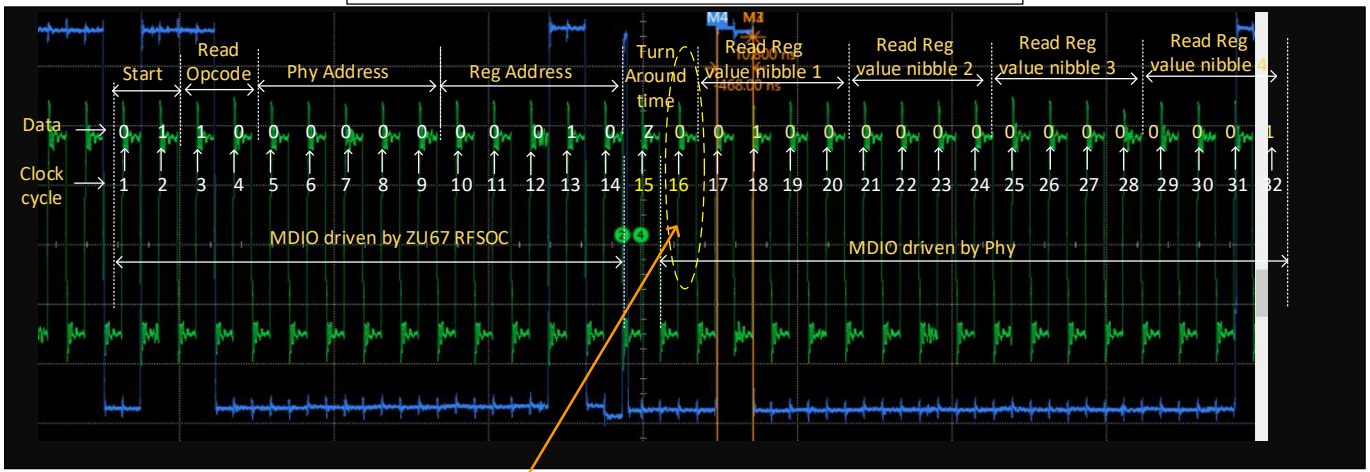
Observation: At the 16th Clock cycle, Phy device is expected to drive 0. However in the Fail case, the Phy device is driving 1 (seems to have started driving the Read register value 1 clock cycle early)
Need to check on specification of ZU67 and Phy device during turn around time.

MDIO access PHYID1 read waveform for Passing vs Failing case

Pass Case: Nov 7: MDIO_PHYID1 Read.pdf



Fail Case: Nov 8: MDIO_PHYID1 READ_JP178_ERROR_1.pdf



<u>MDIO read access to PHYID2 register</u>
Register address: 0x2
Register data: 0x2000

In fail case value read is 0x4001
(bits shifted to left by 1)

Observation: At the 16th Clock cycle, Phy device seems to have started driving the Read register value 1 clock cycle early.
Need to check on specification of ZU67 and Phy device during turn around time.

MDIO access waveform analysis

The Previous two slides capture the MDIO read waveform for Pass and Failing case for two different register reads (PHYID1 (Phy register address :0x02) and PHYID2 (Phy register address :0x02)). Phy Address is 0x0

On comparing the MDIO read access waveform in Pass and Fail case, we find that during the turnaround time (duration between RFSOC driving and TI Phy there is a difference.
We are trying to understand reason for this difference and require clarification on the Xilinx and TI turnaround time specifications

In the fail case, the TI phy device seems to have started driving seems to have started driving the Read register value one clock cycle early compared to expected.
Currently we do not have explanation why this is only seen with 4 Radio boards. The same Phy test board works well with other Radio boards (more than 30 boards). If the Phy was misbehaving we would have seen this issue with almost all Radio boards.

Queries

Question for Xilinx:

At the falling edge before the 14th clock cycle rising edge ZU67 drives last MDIO data bit.

1. What is the delay specification for ZU67 to release the MDIO bus(tristate) after the 14th Clock cycle?

[We need this data to verify that the Phy device MDIO hold time requirement of 10ns after the MDC clock rising edge is met]

Question for TI:

2.What is the Delay specification for Phy device to start driving the MDIO bus between 15th and 16th Clock cycle of MDIO register read access?

[We need this data to verify that the RFSOC device MDIO set time requirement of 80ns before the MDC clock rising edge is met]