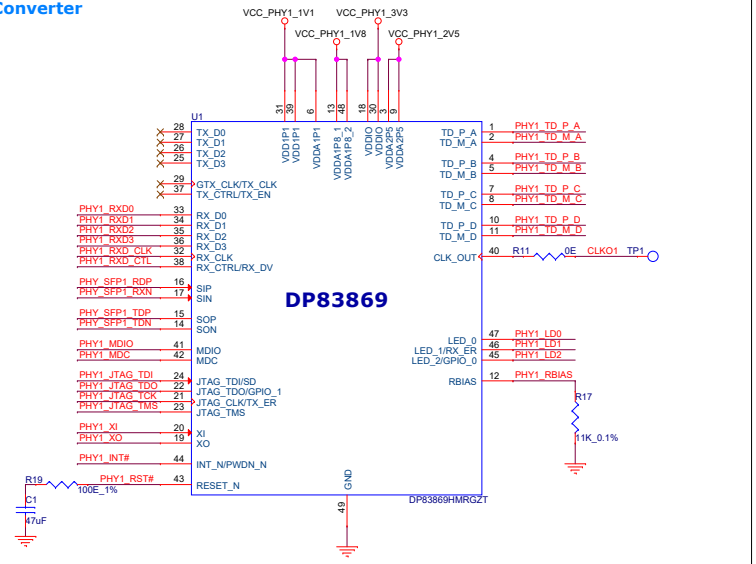
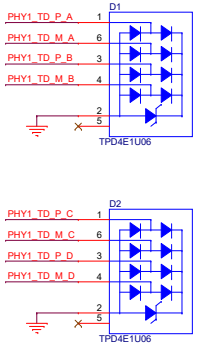
GIGABIT ETHERNET PHY 1

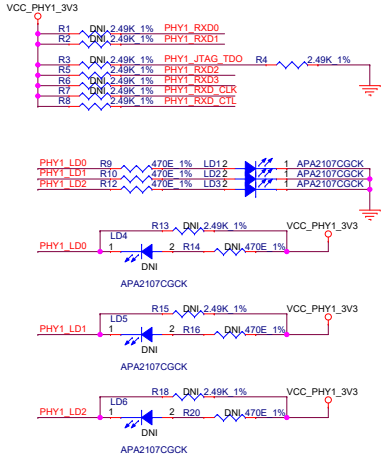
Gb Media Converter



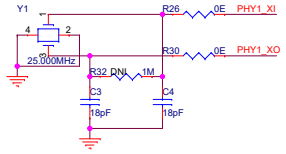
Protection Diodes



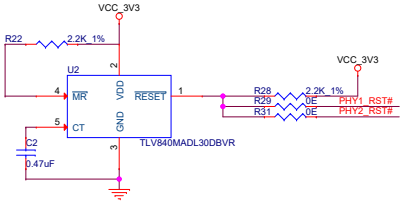
Hardware Strap Configuration



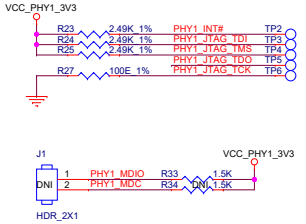
Crystal



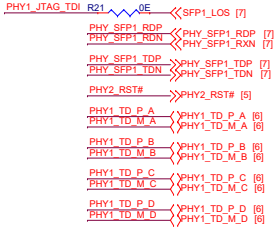
Reset Distribution



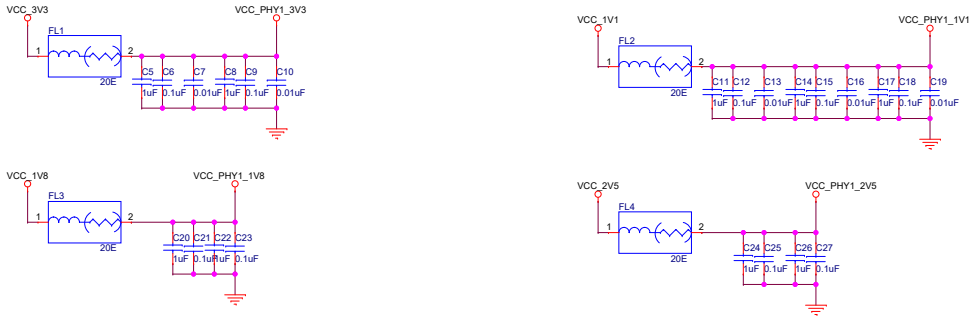
Debug & Test Points



Off-Page Connections



Power Supply Input & Decaps

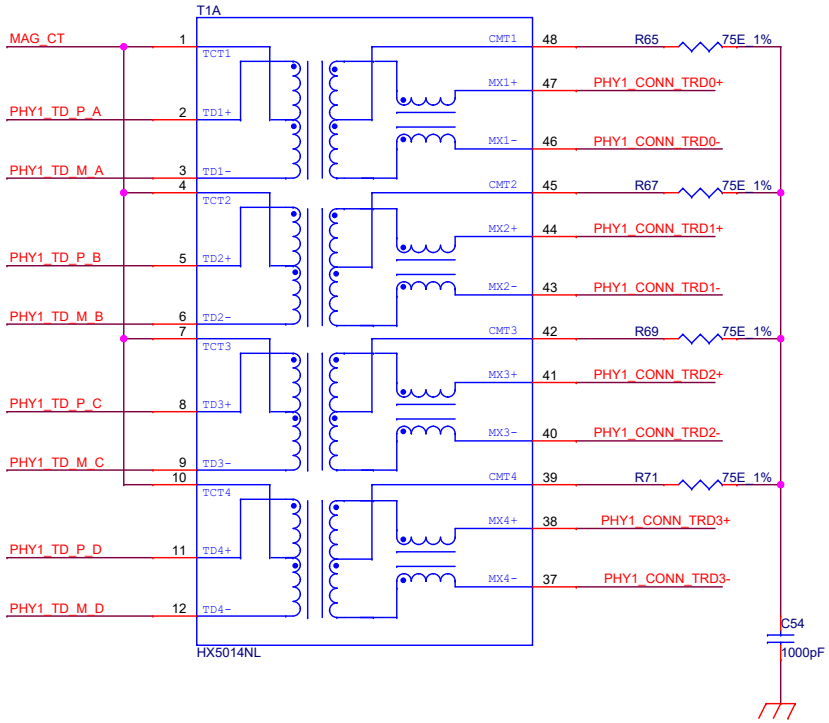


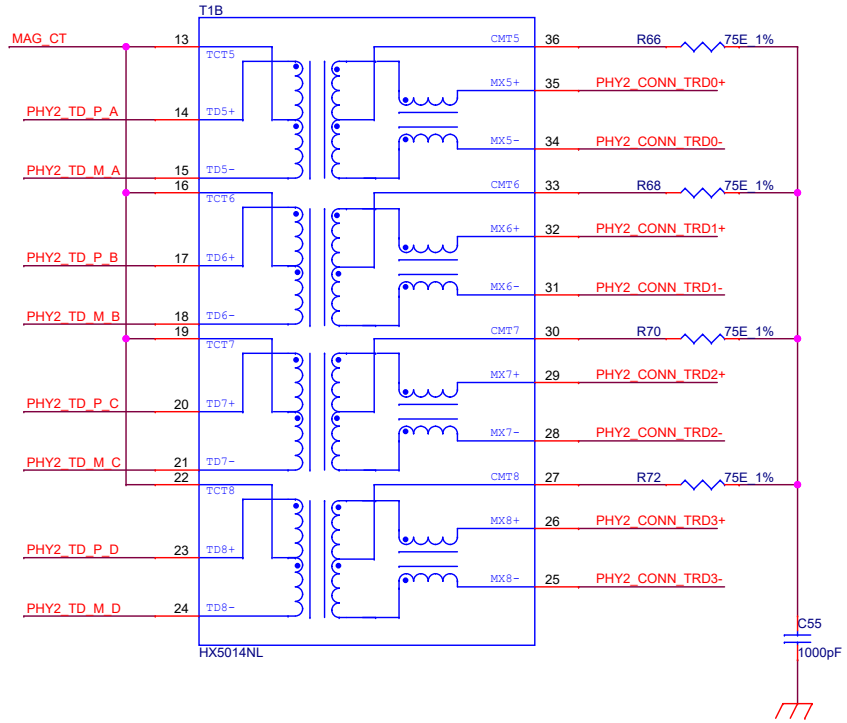
Cad Note: Place the Decaps close to each power pins

Hardware Strap Configuration

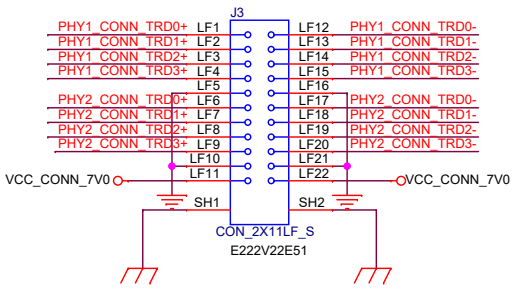
Net Name	Configuration	Summary	
PHYx_RXD0	Open	PHY_ADD[1:0] : 00	
PHYx_RXD1	Open	PHY_ADD[3:2] : 00	
PHYx_JTAG_TDO	PD (0)	OPMODE_0 : 0	OPMODE_[2:0] : 100 1000Base-T to 1000Base-X
PHYx_RXD2	PU (1)	OPMODE_2 : 1	
PHYx_RXD3	PD (0)	OPMODE_1 : 0	
PHYx_RXD_CLK	PD (0)	Link Loss Pass Thru Enabled	
PHYx_RXD_CTL	PU (1)	Copper: Mirror Enable	
PHY1_LD0	PD (0)	Fiber Auto Negotiation	
PHY1_LD1	PD (0)	ANEGSEL_0 : 0	ANEGSEL[1:0] : 00 Copper:Auto-negotiation (1000/100 Advertised), Auto MDIX
PHY1_LD2	PD (0)	ANEGSEL_1 : 0	

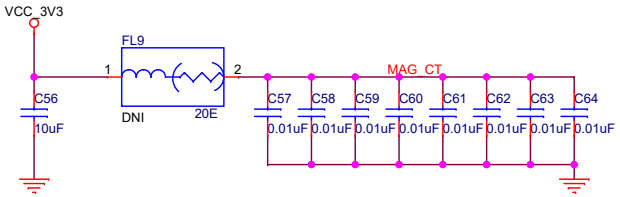
MAGNETICS & I/O CONNECTOR





Input I/O Connector





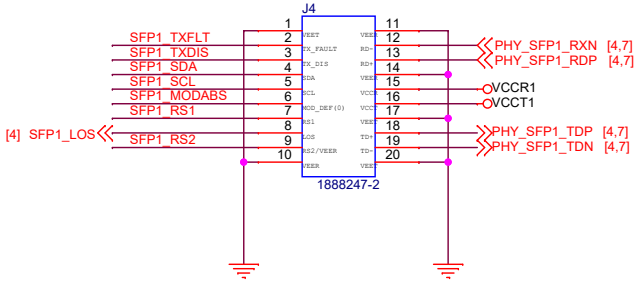
Off-Page Connections

PHY1_TD_P_A
PHY1_TD_M_A
PHY1_TD_P_B
PHY1_TD_M_B
PHY1_TD_P_C
PHY1_TD_M_C
PHY1_TD_P_D
PHY1_TD_M_D

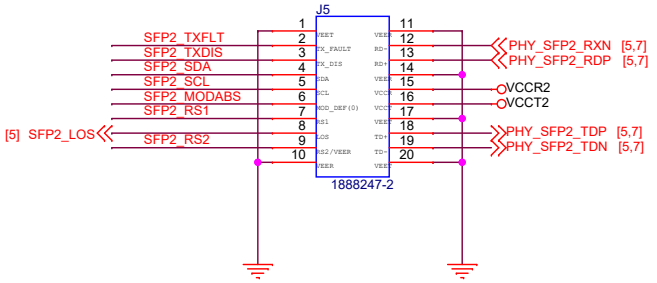
PHY2_TD_P_A
PHY2_TD_M_A
PHY2_TD_P_B
PHY2_TD_M_B
PHY2_TD_P_C
PHY2_TD_M_C
PHY2_TD_P_D
PHY2_TD_M_D

SFP CAGE & CONNECTOR

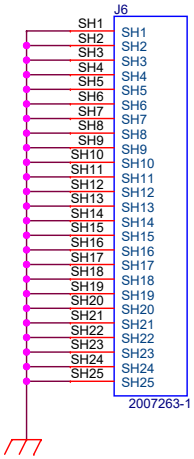
SFP 1 CONNECTOR



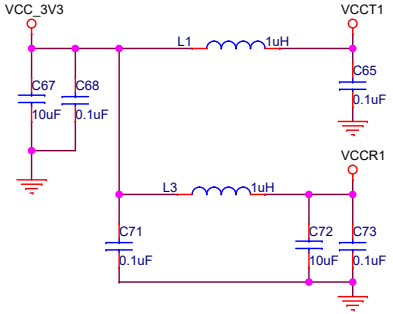
SFP 2 CONNECTOR



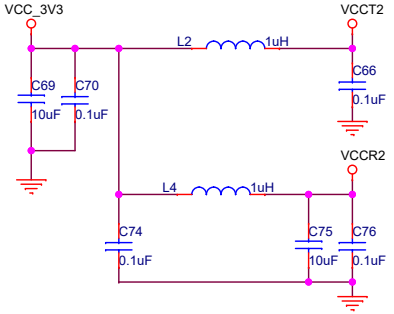
SFP CAGE



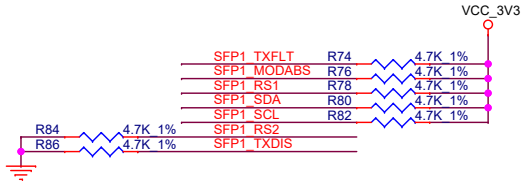
INPUT- POWER FILTERS

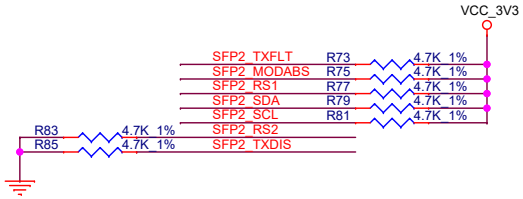


Cad Note: Place the Decaps close to each power pins



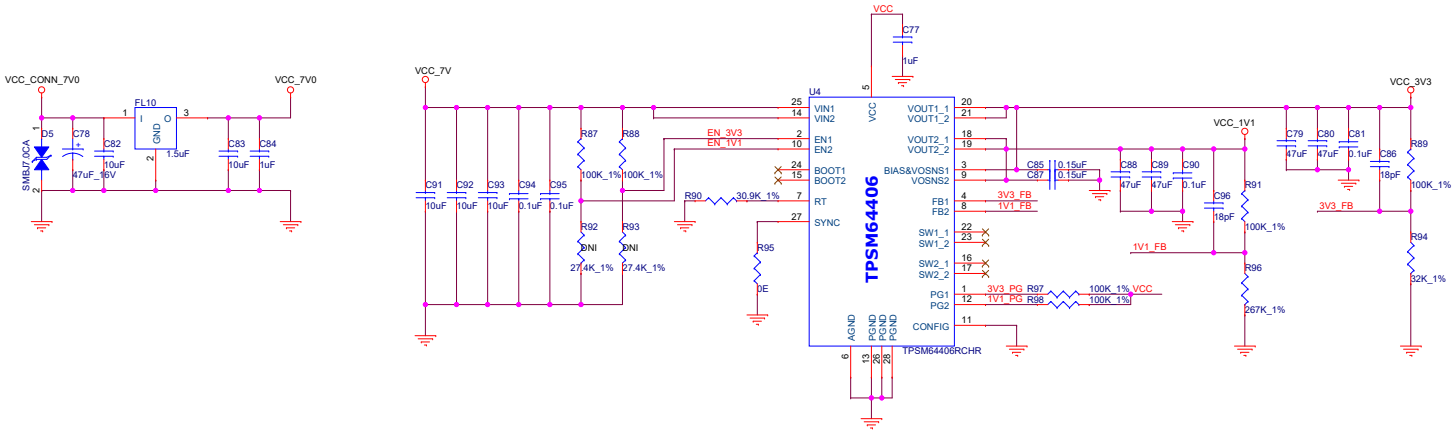
Cad Note: Place the Decaps close to each power pins



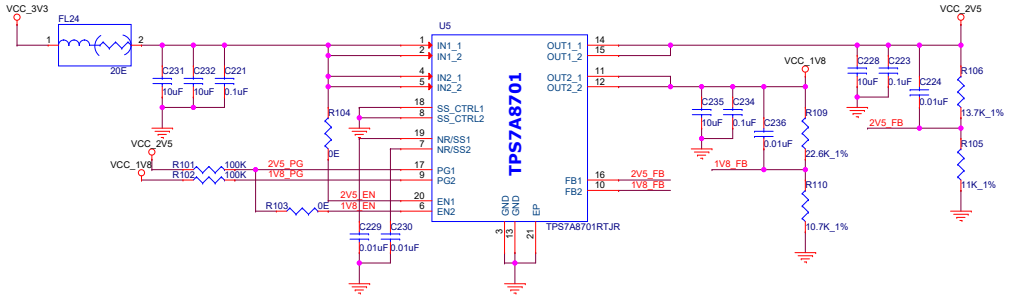


POWER SUPPLY

VCC_3V3 & VCC_1V1



VCC_2V5 & VCC_1V8



MISCELLANEOUS

GROUNDING SCHEME