**MIPI 4 lane waveforms for 954 to ISP SoC**

**Ch1: host to TI954 SCL**, Ch2: host to TI954 SDA, Ch3: host HSYNC, Ch4: host to OV491 MIPI data0

**Normal:**



**HSYNC\_abnormal:**



**no\_MIPI\_output:**



**Serdes setting for 953 and 954:**

TAG:00

7A 01 02 ;reset all

;SL 200

SL 150

7A 0c cf

;7A 10 91

7A 10 90 ;GPIO0 input

7A 11 85

7A 13 89

7A 14 8d

7A 19 15

7A 1a b3

7A 1b c3

7A 1c 4F

;7A 18 01 ;enable FSIN

7A 18 00 ;disable FSIN

7A 4c 01 ;SELECT PORT0

7A 58 5e ;Enable I2C Pass Through

7A 5c 30 ;Serializer Alias

7A 5d 78 ;native I2C ID

7A 65 78 ;Imager alias

7A 6F 00 ;0A ;BCC GPIO2 select frame sync signal

7A 6E 00 ;0A

7A 70 2B ;RAW10 DT + VC0

7A 71 2C ;RAW12 DT + VC1

7A 72 E4 ;VC Mapping default - vc0

7A 4c 12 ;SELECT PORT1

7A 58 5e ;Enable I2C Pass Through

7A 5c 32 ;Serializer Alias

7A 5d 78 ;native I2C ID

7A 65 7C ;Imager alias

7A 6F 00 ;0A ;BCC GPIO2 select frame sync signal

7A 6E 00 ;0A

7A 70 6B ;RAW10 DT + VC0

7A 71 6C ;RAW12 DT + VC1

7A 72 fe ;VC Mapping default - vc1

7A 32 01

7A 33 03 ;CSI Continous clock + 4 Lanes

SL 2

7A 20 00 ;Forward all RX to CSI0

SL 2

30 0e 90 ;[7:4]: enable GPIO0/1/2/3 output

;30 0d 30 ;enable FSIN remote control

30 0d 10 ;20

SL 2

;30 0d 38

30 0d 18 ;28

30 0b 20 ;I2C speed: 390K

30 0c 20

30 02 53 ;MIPI 2lane; 73: 4lane

;30 06 43 ;refclk to sensor:24MHz

;30 07 7D

32 0e 90 ;[7:4]: enable GPIO0/1/2/3 output

;32 0d 30 ;enable FSIN remote control

32 0d 10 ;20

SL 2

;32 0d 38

32 0d 18 ;28

32 0b 20 ;I2C speed: 390K

32 0c 20

32 02 53 ;MIPI 2lane; 73: 4lane

;32 06 43 ;refclk to sensor:24MHz

;32 07 7D