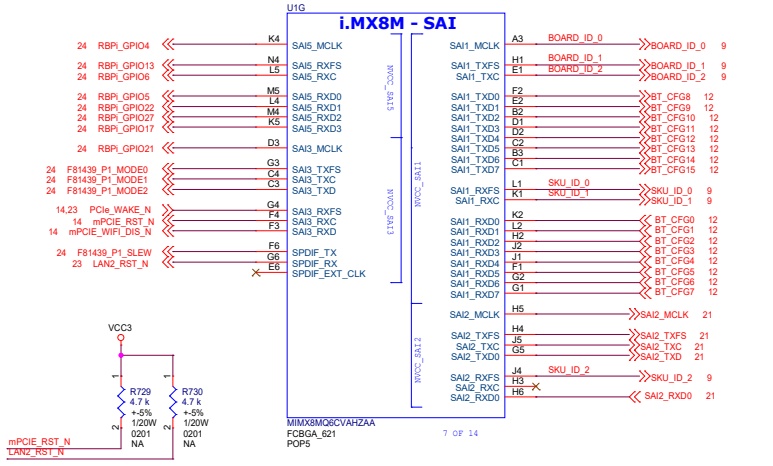
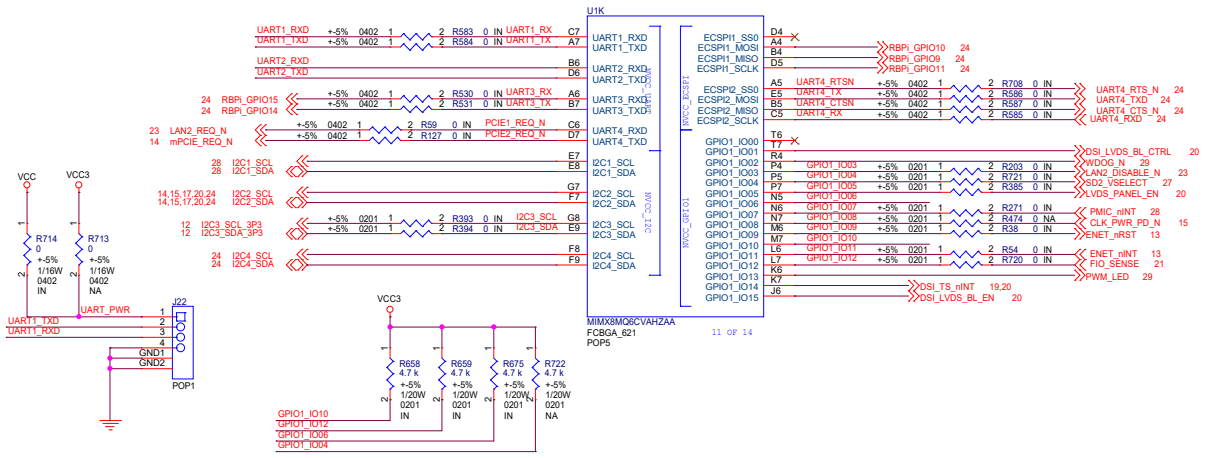
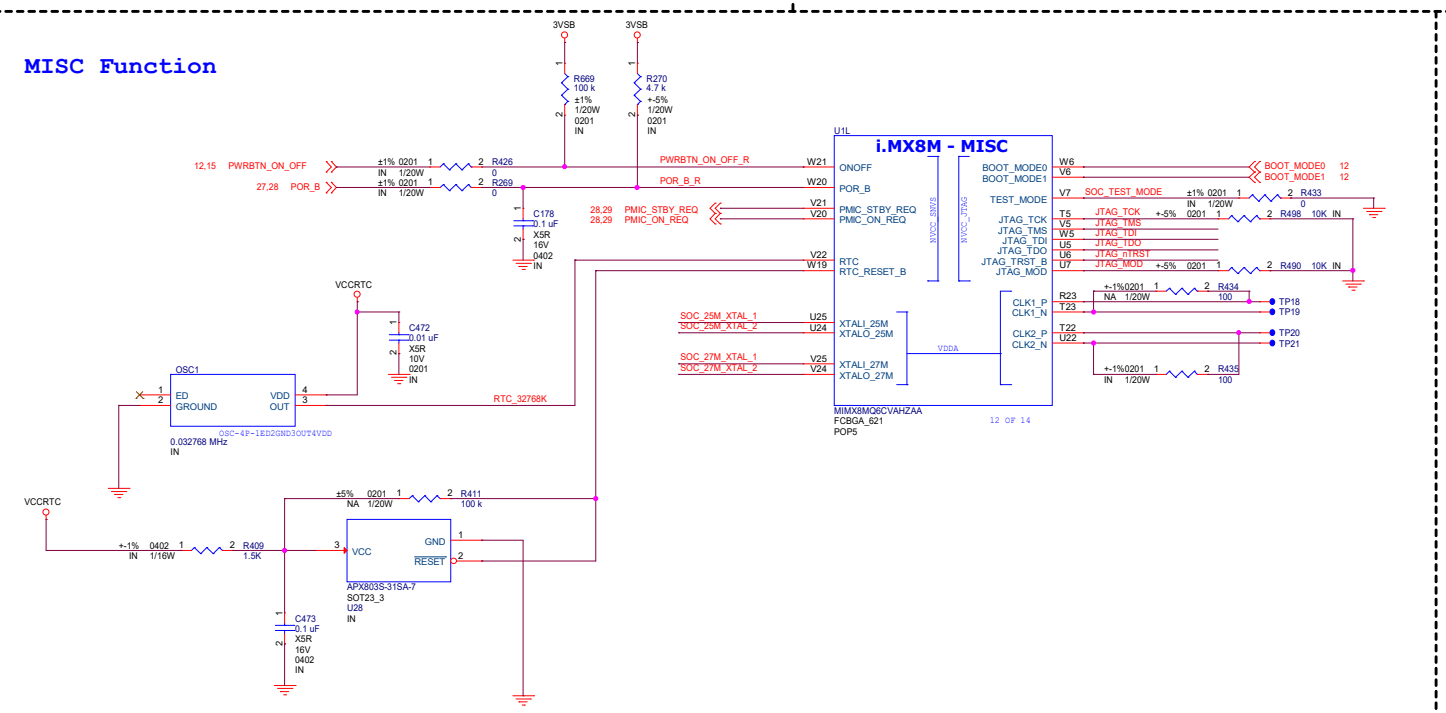
I2S Function

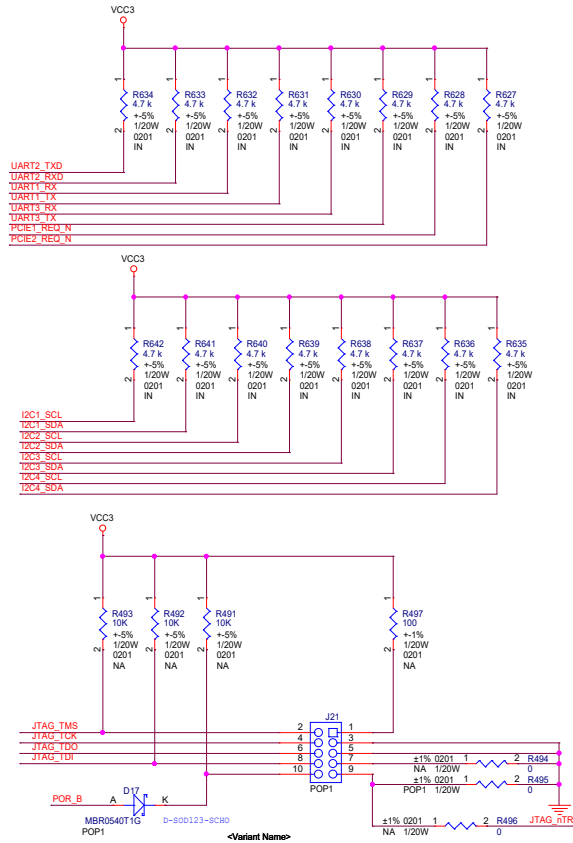


I2C/UART/GPIO Function



MISC Function





Crystal

<Variant Name>

MiTAC Computing Technology Corp.

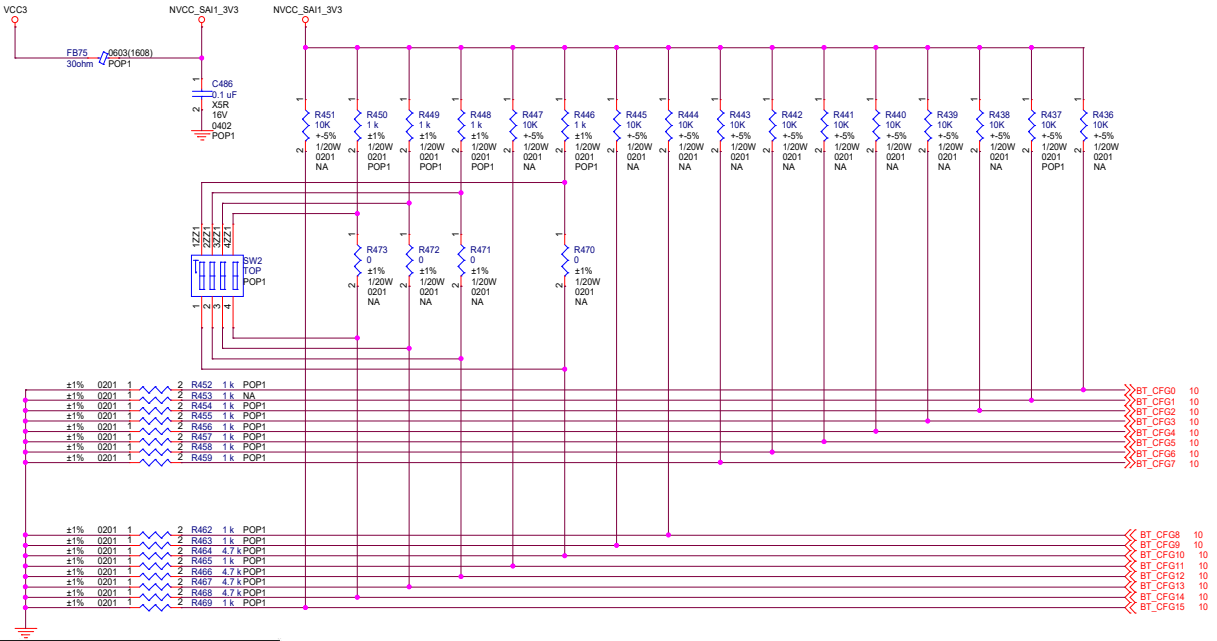
Title	SOC-I2S/UART/MISC/GPIO	
Size: C	Document Number: ND108T	Rev: R0A
Date: Monday, June 15, 2020	Sheet 10 of 30	

Boot ROM Fuse

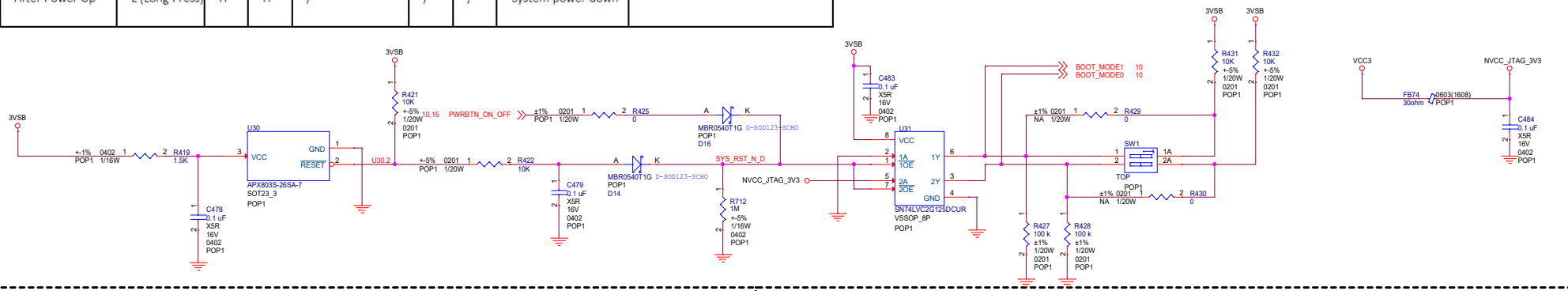
<Default: eMMC BOOT>, QSPI boot is not supported by ROM

	Address	7	6	5	4	3	2	1	0
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]
	0x470[15:8]	(Infinit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - eSDHC1 01 - eSDHC2		Power Cycle Enable '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel. (for SDR50 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			QSPI Instance: 0 - Quad(SPI)0 1 - Reserved	SDR SMP: "000" - Default "001-111"		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed: 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC4.4) 110 - 8-bit DDR (MMC4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC1 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V	USDHC2 IO VOLTAGE SELECTION 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8			Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles.			Reserved
QSPI	0x470[7:0]	HSPHS: Half Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	HSDLY: Half Speed Delay selection 0 : one clock delay 1: two clock delay	FSPHS: Full Speed Phase Selection 0 : select sampling at non-inverted clock 1: select sampling at inverted clock	FSDLY: Full Speed Delay selection 0 : one clock delay 1: two clock delay	Reserved	Reserved	Reserved	Reserved
SPINOR	0x470[7:0]	CS select (SPI only): 00 - CS0 (default) 01 - CS1 10 - CS2 11 - CS3		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

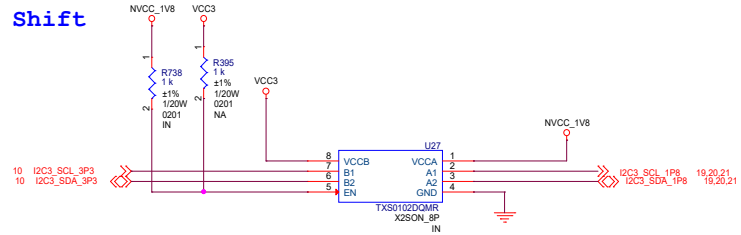
Debug SW



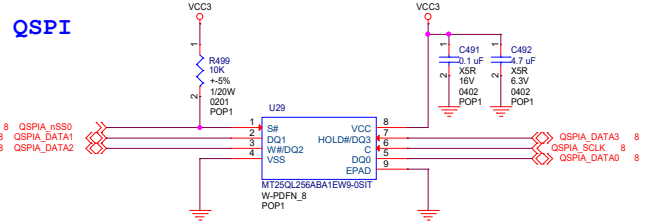
item	Power state	ONOFF	RST	OE	DIP SW	BM1	BM0	Note	Description
1	During Power Up	H (No press)	L	H	1-4 : OFF; 2-3 : ON	0	1	Serial Downloader	item 1/2 for system development item 2/3 for system upgrade Normal power key function
2	During Power Up	H (No press)	L	H	1-4 : ON; 2-3 : OFF	1	0	Internal Boot	
3	During Power Up	L (Press)	L	L	1-4 : ON; 2-3 : OFF	0	1	Serial Downloader	
4	After Power Up	H (No press)	H	H	/	/	/	No power key event	
5	After Power Up	L (Short Press)	H	H	/	/	/	Power key event	
6	After Power Up	L (Long Press)	H	H	/	/	/	System power down	



LEVEL Shift



QSPI

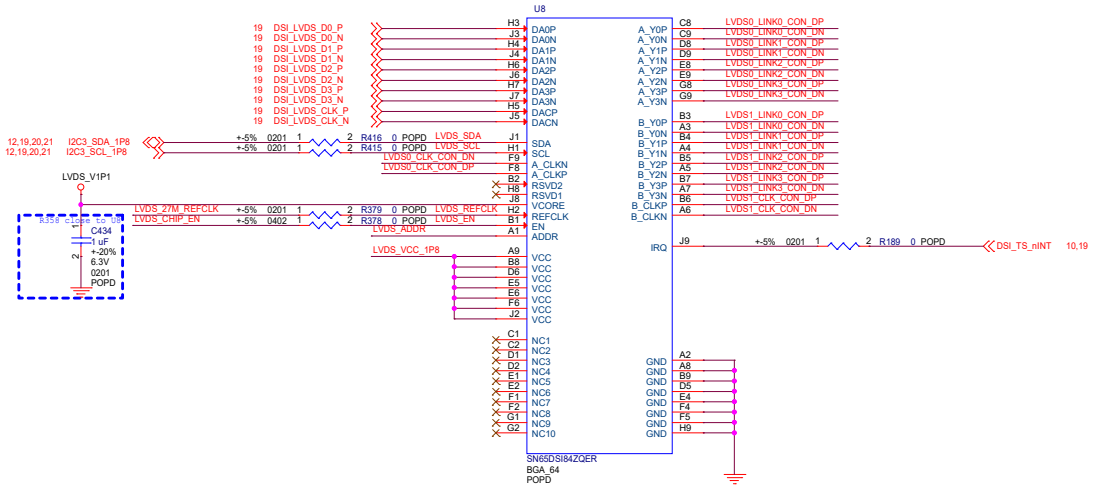


<Variant Name>

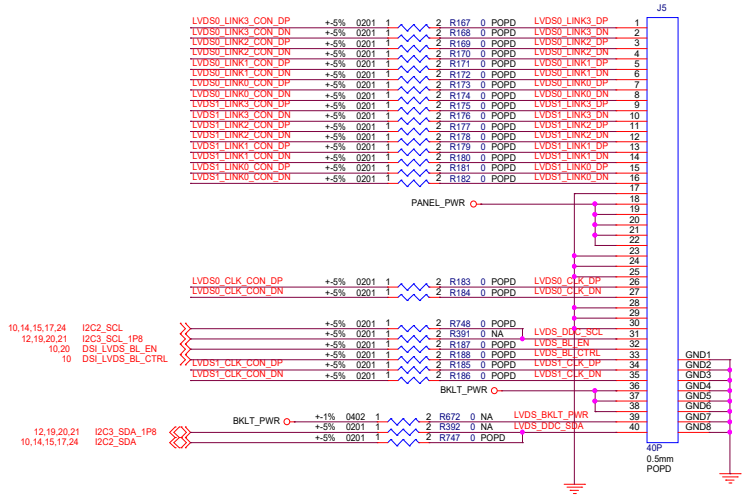
MiTAC Computing Technology Corp.

Title	Debug SW/Level Shift/QSPI	
Size C	Document Number ND108T	Rev R0A
Date: Friday, July 03, 2020	Sheet 12 of 30	

MIPI to LVDS- SN65DSI84ZQER

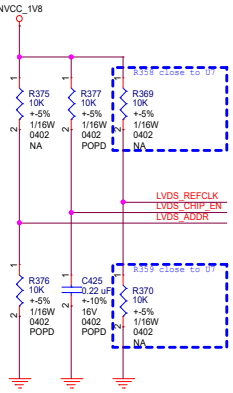


LVDS CONNECTOR

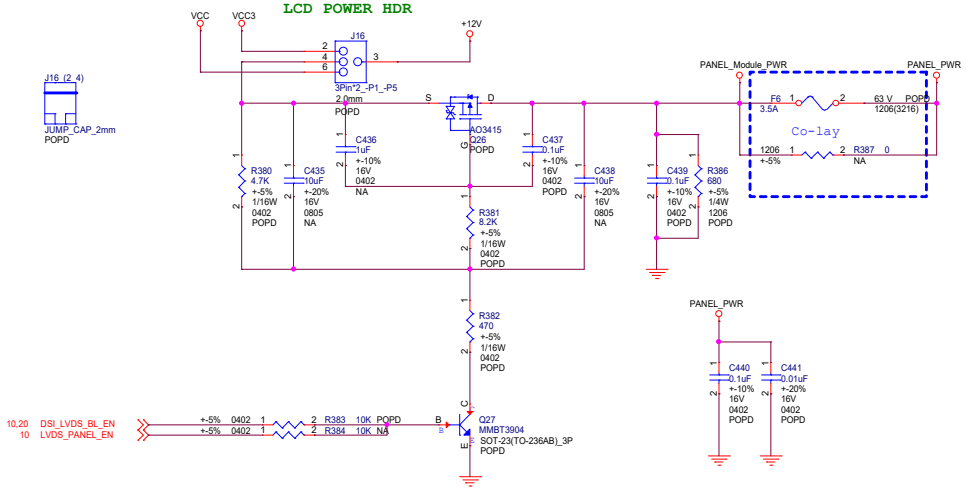


Strapping Setting

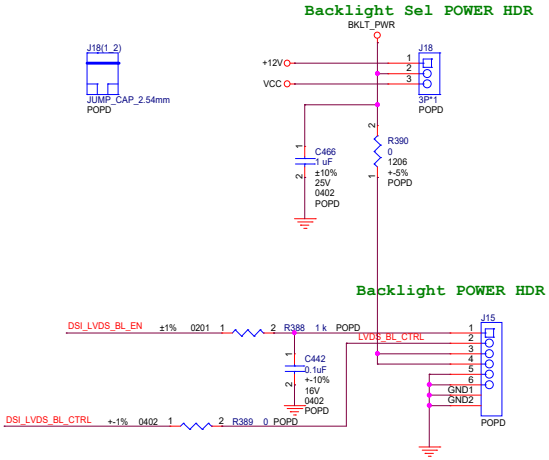
When ADDR=0,
Address Cycle is 0x58 (Write) and 0x59 (Read)



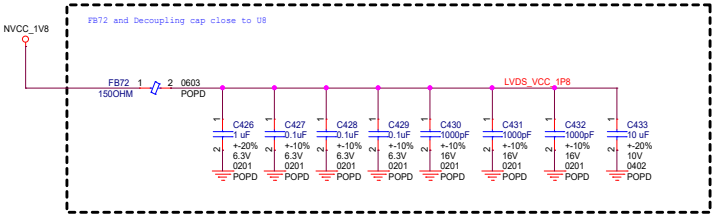
Panel Power



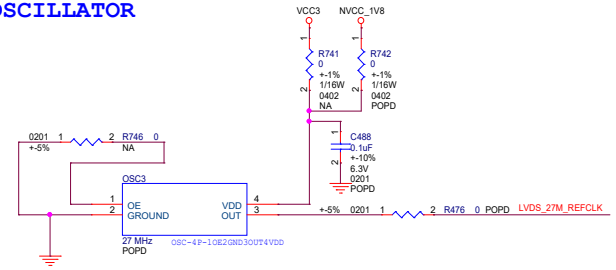
Backlight Power



POWER for CHIP



OSCILLATOR



<Variant Name>

MiTAC Computing Technology Corp.

Title	MIPI to LVDS SNDSI84	
Size: C	Document Number: ND108T	Rev: R0A
Date: Monday, June 15, 2020	Sheet 20 of 30	