



## SERDESUB – 913ROS

DS90UB913Q Serializer and DS90UB914Q Deserializer Evaluation Kit

User's Manual

Rev 2.1

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## **Introduction:**

National Semiconductor's Automotive SERDES DS90UB913/914Q FPD-Link III evaluation kit contains one (1) DS90UB913Q Serializer board and one (1) DS90UB914Q Deserializer board. The boards are mounted with the Rosenberger connectors for connectivity using the Leoni-Dacar cables (not sent along with the kits). The boards also have the option of being populated with single ended coaxial cables.

The DS90UB913Q/914Q chipset supports a variety of automotive mega-pixel camera systems over a two (2) wire serial stream. The single differential pair (FPD-Link III) is well-suited for direct connections between an imager and Host Controller/Electronic Control Unit (ECU)/FPGA. The bidirectional control channel of the DS90UB913Q/914Q provides seamless communication between the ECU/FPGA and the display module.

This kit will demonstrate the functionality and operation of the DS90UB913Q and DS90UB914Q chipset. The chipset enables transmission of a high-speed video data along with a low latency bi-directional control bus over a single twisted pair cable. The integrated control channel transfers data bi-directionally over the same serial video link. The transport delivers 10/12 bits of parallel data, two SYNC bits and PCLK together with a bidirectional control channel that supports an I<sup>2</sup>C bus. Additionally, there are four unidirectional general purpose (GPI and GPO) signal lines for sending control data. This interface allows transparent full-duplex communication over a single high-speed differential pair, carrying asymmetrical bi-directional control information without the dependency of video blanking intervals. The Serializer and Deserializer chipset is designed to transmit data at PCLK clocks speeds ranging from 10 to 100 MHz and I<sup>2</sup>C bus rates up to 400 kbps at up to 10 meters cable length over -40 to +105 Deg C.

The user needs to supply only a single 5V supply to the Deserializer boards as these kits have power transfer over coax/ power transfer over differential pair capabilities.

**The demo boards can be used for EMI testing.**

### **System Requirements:**

In order to demonstrate, the following are required:

- 1) Mega-pixel imager modules such as the Omnivision OV10630 or Aptina MT9M023.
- 2) Microcontroller (MCU) or FPGA with I<sup>2</sup>C interface bus (I<sup>2</sup>C master)
  - a. slave clock stretching must be supported by the I<sup>2</sup>C master controller/MCU.
- 3) External peripheral device that supports I<sup>2</sup>C (slave mode)
- 4) 5V power supply.

### **Contents of the Demo Evaluation Kit:**

- 1) One Serializer board with the DS90UB913Q
- 2) One Deserializer board with the DS90UB914Q
- 3) Evaluation Kit Documentation (this manual)

4) DS90UB913Q/914Q Datasheet

## DS90UB913Q/914Q SerDes Typical Application

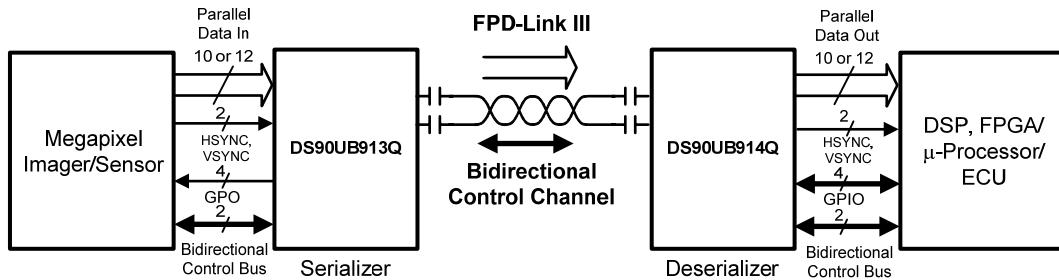


Figure 1. Typical Application of DS90UB913Q/914Q Chipset

The diagram above illustrates a typical application of DS90UB913Q/914Q chipset. The ECU/FPGA can program device registers on the DS90UB913Q, DS90UB914Q, and remote peripheral device, such as a display module.

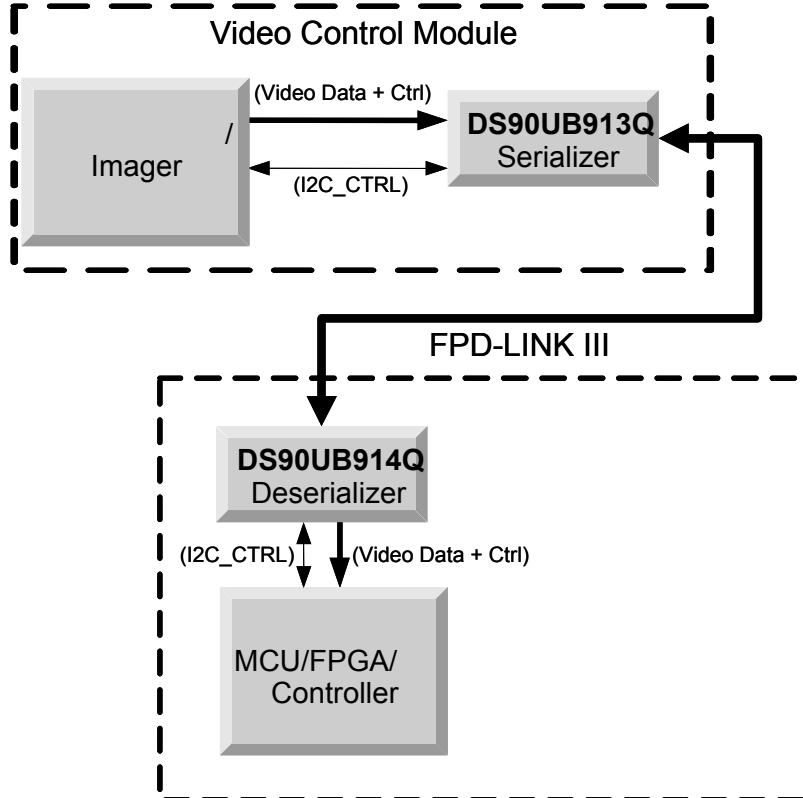


Figure 2. Typical DS90UB913/914Q Imager System Diagram

Refer to the proper datasheet information on Chipsets (Serializer/Deserializer) provided on each board for more detailed information.

## How to set up the Demo Evaluation Kit:

The DS90UB913Q/914Q evaluation boards consist of two sections. The first part of the board provides the point-to-point interface for transmitting parallel video data. The second part of the board allows bi-directional control communication of an I<sup>2</sup>C bus control of using a MCU/FPGA to programming a remote peripheral device via the Serializer.

The PCB routing for the Serializer input pins (DIN) accept incoming parallel video data at 1.8V/3.3V LVCMOS signals from J1 IDC connector. The FPD-Link III interface can use a single twisted pair cable or a single coax cable. The output pins (ROUT) are accessed through a JP1 IDC connector. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

- 1) Connect the DS90UB913/914Q demo boards using a Leoni/Dacar cable or a coaxial cable( not provided)
- 2) Jumpers and switches have been configured at the factory; they should not require any changes for immediate operation of the chipset. See text on Configuration settings and datasheet for more details. The jumpers and connectors are configured in external oscillator mode with the VDDIOs toggling at 3.3V.
- 3) From the imager, connect a flat cable (not supplied) to the Serializer board and connect another flat cable (not supplied) from the Deserializer board to the ECU/FPGA module. *Note: For 50 ohm signal sources, provide 1.8V/3.3V LVCMOS input signal levels into DIN[12:0], HS, VS and PCLK*
- 4) Connect the Deserializer I<sup>2</sup>C ports to the I<sup>2</sup>C of the MCU/FPGA (I<sup>2</sup>C master). Connect the Serializer I<sup>2</sup>C ports to the I<sup>2</sup>C bus of the peripheral slave device.
- 5) Power for the Serializer and Deserializer boards must be supplied externally through JP5 on the Deserializer board and JP4 on the Serializer board.

## Bi-Directional Control Bus And I<sup>2</sup>C Modes:

In order to communicate and synchronize with remote devices on the I<sup>2</sup>C bus through the bi-directional control channel, slave clock stretching must be supported by the I<sup>2</sup>C master controller/ECU. The chipset utilizes bus clock stretching (holding the SCL line low) during data transmission; where the I<sup>2</sup>C slave pulls the SCL line low prior to the 9th clock of every I<sup>2</sup>C data transfer (before the ACK signal).

The bidirectional control bus supports an I<sup>2</sup>C compatible interface that allows programming of the DS90UB913Q, DS90UB914Q, or an external remote device (such as an imager). Register programming transactions to/from the DS90UB913Q/914Q chipset are employed through the clock (SCL) and data (SDA) lines. These two signals have open drain I/Os and must be pulled-up to VDDIO by external resistors. The boards have an option to use the on-board 10KΩ pull-up resistors tied to VDDIO or connected through external pull-ups at the target Host. The appropriate pull-up resistor values will depend upon the total bus capacitance and operating speed. The DS90UB913Q/914Q I<sup>2</sup>C bus data rate supports up to 400 kbps according to I<sup>2</sup>C specification.

## Demo Board Power Connections:

Power should be only applied to the DS90UB914Q Deserializer boards. Power is transferred over the link using either the Differential pair or the coaxial link.

## DS9UB913Q Serializer Board Description:

The 2x15-pin IDC connector JP1 accepts 10/12 bits of 1.8V or 3.3V data, HS, VS and PCLK. VDDIO must be set externally for 1.8V or 3.3V LVCMOS inputs.

The Serializer board can be powered from the Deserializer board. For the Serializer to be operational, the S1-PDB switch on 1 must be set HIGH. S1-RES0 must be set LOW.

The boards can be connected to the Deserializer boards using either Rosenberger connectors or co-axial connectors as shown in Figure 3Figure 3. DS90UB913Q Boards with HSD Connector and Figure 4.

### Configuring the Mode Pin on the Serializer Board

To configure the device in the external oscillator mode, PCLK mode or the AON clock mode, switch S8 has to be configured as shown in Table. 1.

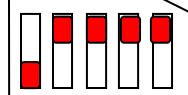
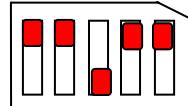
Mode Configuration	Switch S8 Settings
PCLK from imager	
External Oscillator Mode	

Table 1. Mode switch configuration on the Serializer Board

### Serializer LVCMOS Pinout by Connector

The following three tables illustrate how the Deserializer connections are mapped to the IDC connector J1 on the Serializer board.

JP1			
LVC MOS I/O			
pin no.	name	name	pin no.
1	GND	<b>DIN0</b>	2
3	GND	<b>DIN1</b>	4
5	GND	<b>DIN2</b>	6
7	GND	<b>DIN3</b>	8
9	GND	<b>DIN4</b>	10
11	GND	<b>DIN5</b>	12
13	GND	<b>DIN6</b>	14
15	GND	<b>DIN7</b>	16
17	GND	<b>DIN8</b>	18
19	GND	<b>DIN9</b>	20
21	GND	<b>DIN10</b>	22
23	GND	<b>DIN11</b>	24
25	GND	<b>HS</b>	26
27	GND	<b>VS</b>	28
29	GND	<b>PCLK</b>	30

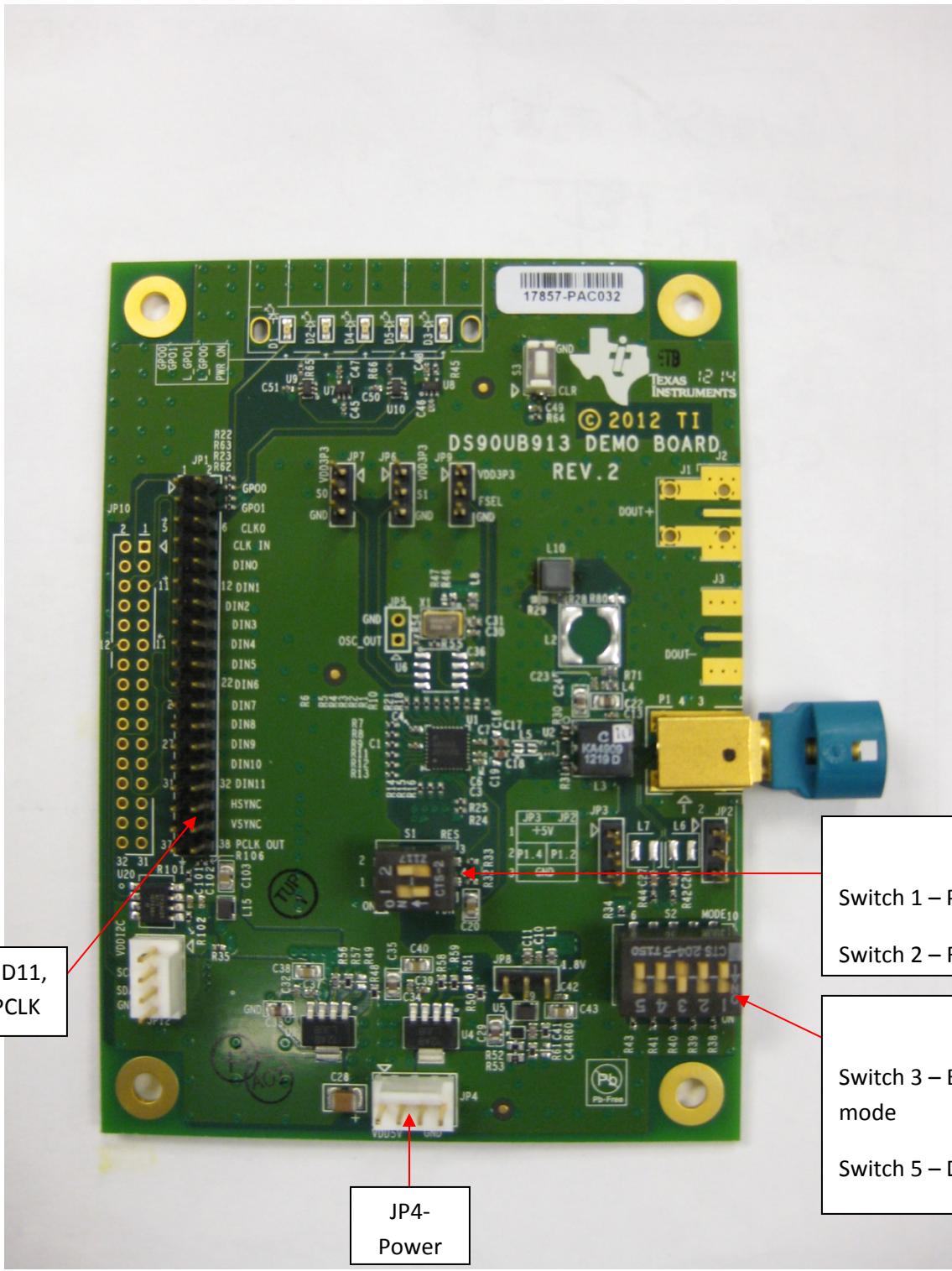


Figure 3. DS90UB913Q Boards with HSD Connector

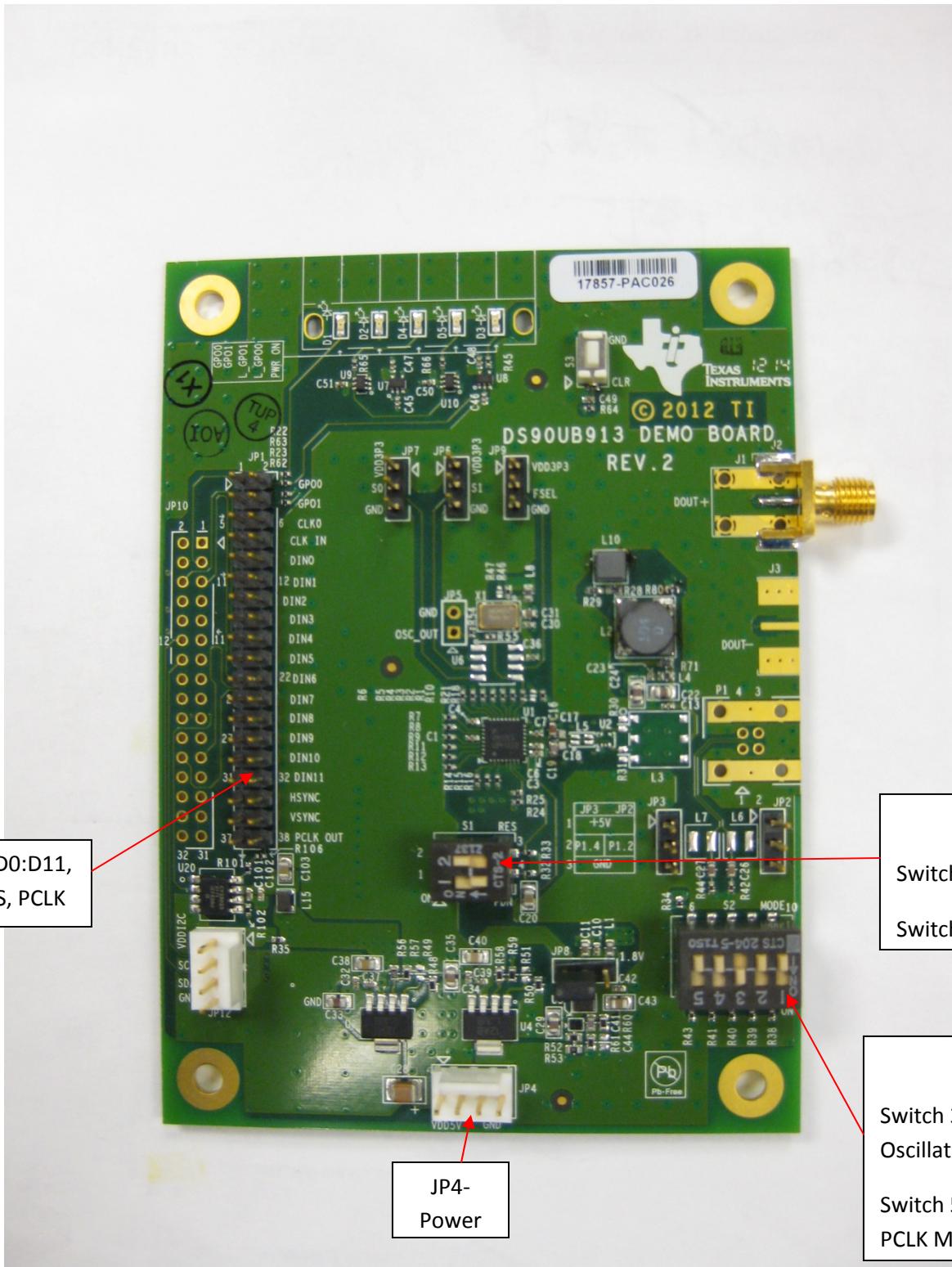


Figure 4. DS90UB913Q Board with Coax connector

## DS9UB914Q Deserializer Board Description:

The Deserializer board can be powered using header JP5. For the Deserializer to be operational, follow the dip switch configuration S1 shown in Table 2 and Table 3. The 2x15 pin IDC Connector JP1 provides access to the 1.8V or 3.3V LVC MOS data, HS, VS and PCLK outputs.

The Deserializer board is by default configured to operate in the 100MHz mode with 1.8V I/O. The default device address of the DS90UB914Q on the Board is C0.

### Dip Switch S2 Configuration on the Deserializer Board

To configure the DS90UB914Q device on the Deserializer board, please follow Table.2.

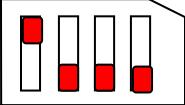
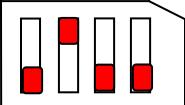
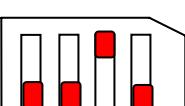
Mode Configuration	Switch S6 Settings
12-bit Low Frequency Mode	
12-bit High Frequency Mode	
10-bit Mode	

Table 2. Mode Switch Configuration on the Deserializer Board

### Dip Switch S1 Configuration on the Deserializer Board

To configure the DS90UB914Q device on the Deserializer board, please follow Table.2.

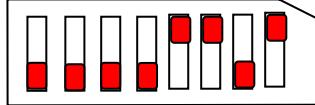
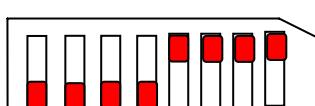
Mode Configuration	Switch S6 Settings
Normal Mode configuration	
BIST Mode configuration	

Table 3. Mode Switch Configuration on the Deserializer Board

## Deserializer LVCMOS Pinout by Connector

The following table illustrates how the Deserializer connections are mapped to the IDC connector J1 on the Serializer board.

J1			
LVCMOS I/O			
pin no.	name	name	pin no.
1	ROUT0	GND	2
3	ROUT1	GND	4
5	ROUT2	GND	6
7	ROUT3	GND	8
9	ROUT4	GND	10
11	ROUT5	GND	12
13	ROUT6	GND	14
15	ROUT7	GND	16
17	ROUT8	GND	18
19	ROUT9	GND	20
21	ROUT10	GND	22
23	ROUT11	GND	24
25	HS	GND	26
27	VS	GND	28
29	PCLK	GND	30

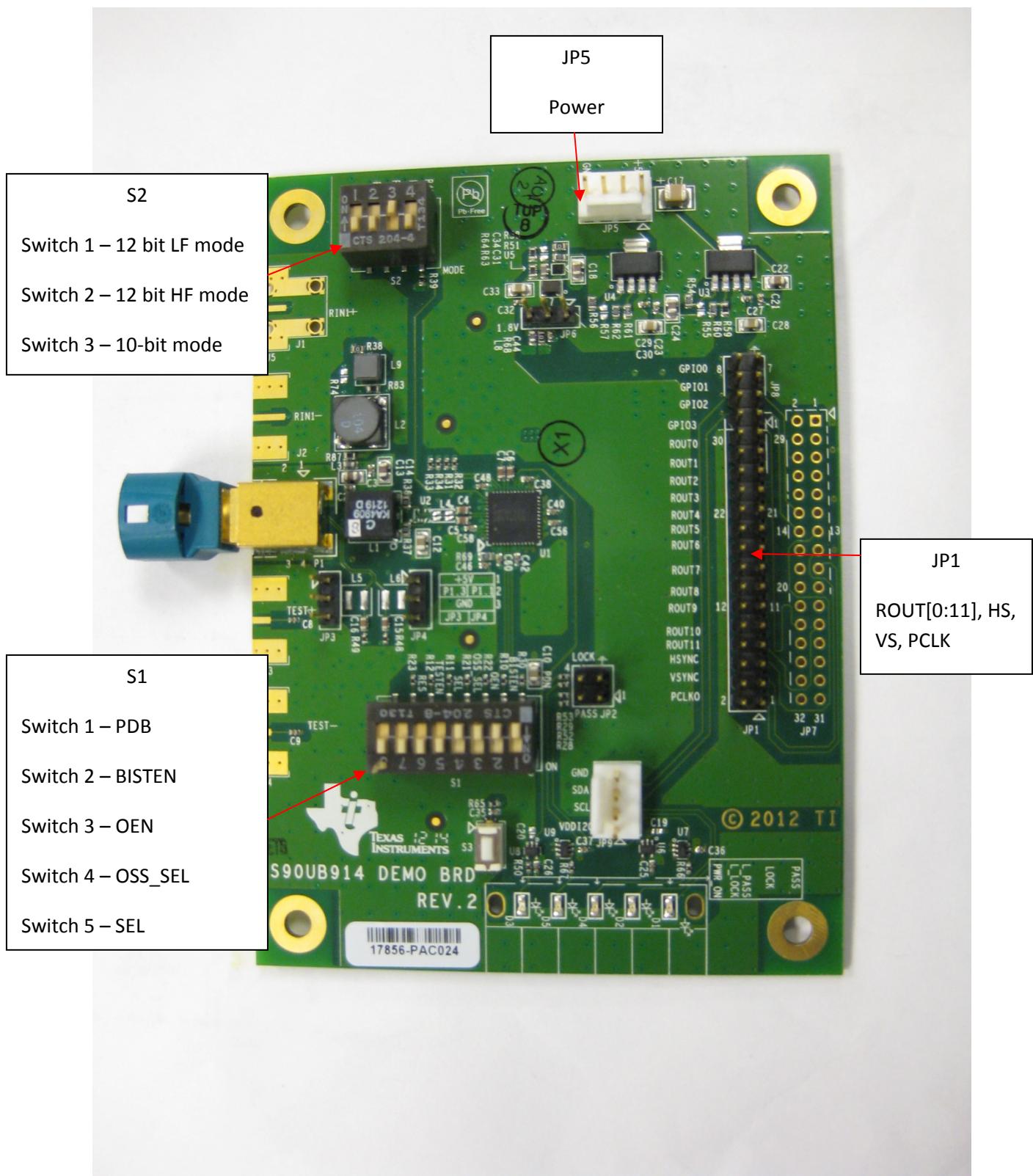


Figure 5. DS90UB914Q Deserializer boards with HSD Connectors

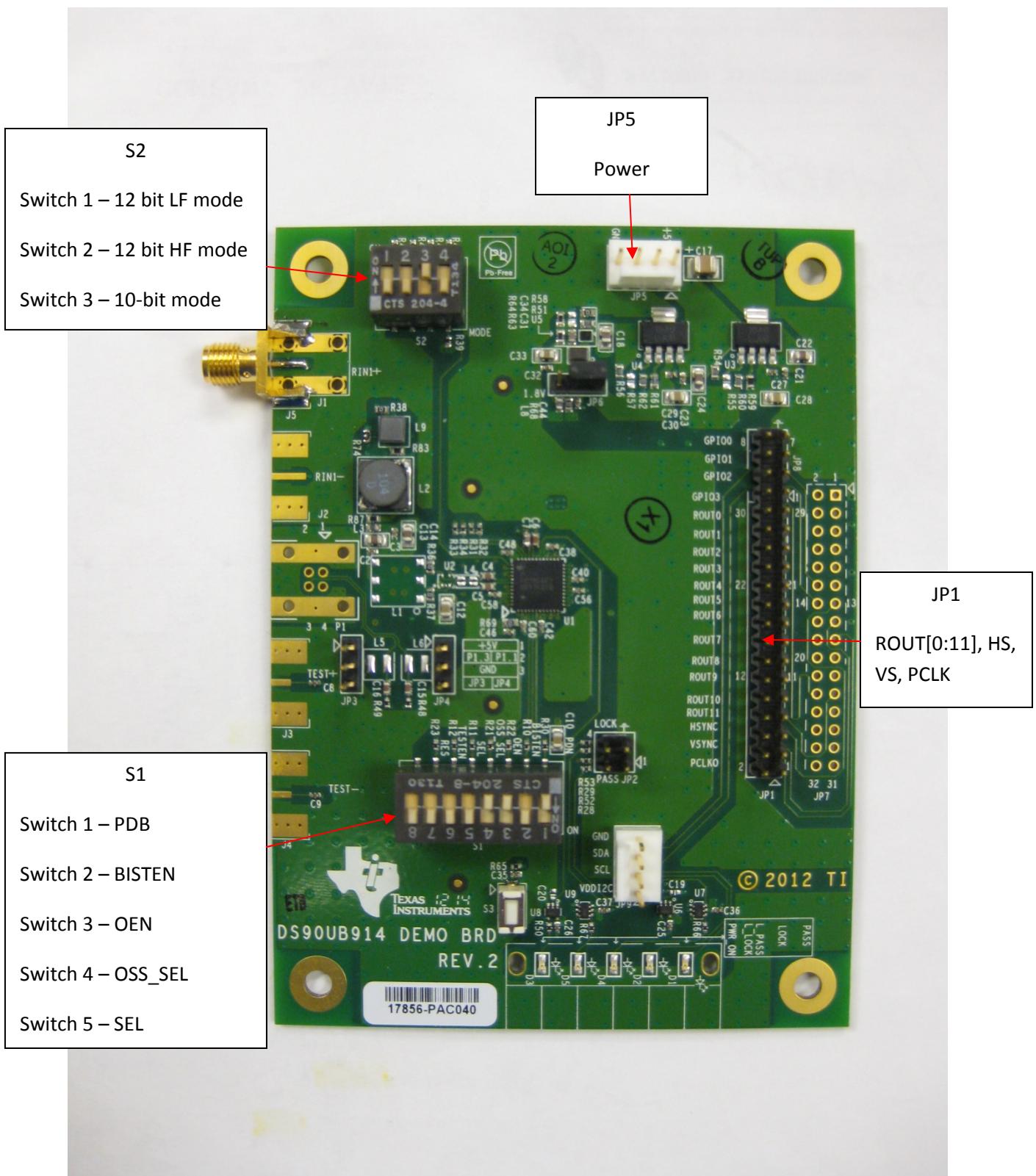


Figure 6. DS90UB914Q Deserializer boards with Coax Option

## Typical Connection and Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the Serializer inputs:

1) Image Sensor such as the OV10630 or MT9M024

2) Any other signal generator / video source that generates the correct input levels.

The following is a list of typical test equipment that may be used to monitor the output signals from the Deserializer:

1) Microcontroller or FPGA with an I<sup>2</sup>C interface

2) Optional – Logic Analyzer or Oscilloscope

3) Any SCOPE with a bandwidth of at least 50MHz for 1.8V/3.3V LVCMOS and/or 1.5GHz for observing differential signals.

## I<sup>2</sup>C Communication over Bi-directional Control Channel in Camera Mode

### Camera Mode:

In Camera mode, I<sup>2</sup>C transactions originate from the Master controller at the Deserializer side. The I<sup>2</sup>C slave core in the Deserializer will detect if a transaction is intended for the Serializer or a slave at the Serializer. Commands are sent over the bi-directional control channel to initiate the transactions. The Serializer will receive the command and generate an I<sup>2</sup>C transaction on its local I<sup>2</sup>C bus. At the same time, the Serializer will capture the response on the I<sup>2</sup>C bus and return the response on the forward channel link. The Deserializer parses the response and passes the appropriate response to the Deserializer I<sup>2</sup>C bus.

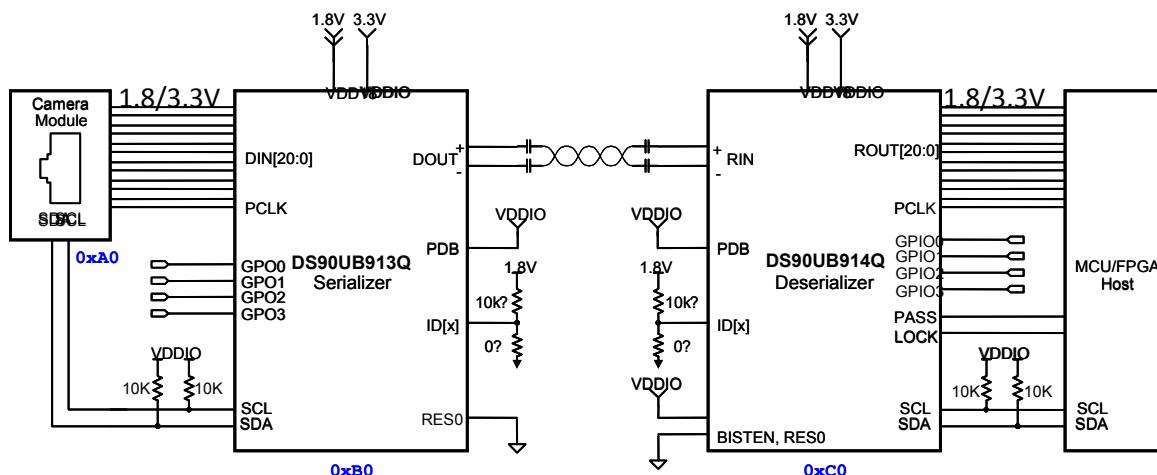
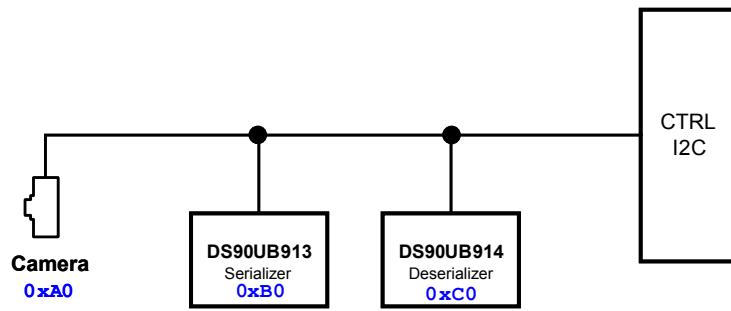


Figure 7. Example of DS90UB913Q/914Q in Camera Application

## Procedure – Camera Mode:

- 1) Connect the 1.8V and 3.3V power with +1.8V and +3.3V supplies accordingly. Keep the power off.
- 2) Verify that all the jumper positions and switches are correctly set.
- 3) Connect a Leoni-Dacar cable across the Serializer and Deserializer board.
- 4) Set hardware configuration for DS90UB913Q Serializer and DS90UB914Q Deserializer devices
  - a. Verify peripheral device (camera) address is set to [0xA0](#)
  - b. Set Serializer and Deserializer I<sup>2</sup>C slave address on ID[x] (CAD) pin:
    - i. Serializer Rid=0ohm; Serializer I<sup>2</sup>C slave address is [0xB0](#)
    - ii. Deserializer Rid=0ohm; Deserializer I<sup>2</sup>C slave address is [0xC0](#)
- 5) Turn on the +1.8V and +3.3V power supplies
- 6) The DS90UB914Q Deserializer I<sup>2</sup>C slave is enabled to receive data directly from the I<sup>2</sup>C Master Controller. I<sup>2</sup>C transfers are processed in a one byte basis. After receiving one byte, the Deserializer slave will need to acknowledge (ACK) the transfer to receive the next following byte. The Deserializer slave holds SCL low (clock stretch) for the required period until an ACK (or NACK) is established and then releases it. The Deserializer I<sup>2</sup>C slave acknowledges all the transfers addressed to Deserializer, Serializer, or remote device.
- 7) Before initiating any I<sup>2</sup>C commands, the Deserializer needs to be programmed with the target slave device addresses and Serializer device address. SER\_DEV\_ID Register 0x07h sets the Serializer device address and SLAVE\_x\_MATCH/ SLAVE\_x\_INDEX registers 0x08h~0x17h set the remote target slave addresses. In slave mode the address register is compared with the address byte sent by the I<sup>2</sup>C master. If the addresses are equal to any of registers values, the I<sup>2</sup>C slave will acknowledge and hold the bus to propagate the transaction to the target device otherwise it returns no acknowledge.
- 8) Execute I<sup>2</sup>C instructions to write the following registers
  - a. Assign ID Match values for camera address on Deserializer
    - i. Write 0xA0 to Register 0x08 of Deserializer ([0xC0](#))
    - ii. Write 0xA0 to Register 0x10 of Deserializer ([0xC0](#))
  - b. Wake up the Serializer by programming the ‘Remote Wakeup’ Register on the Deserializer
    - i. Write 0x04 to Register 0x01 of Deserializer ([0xC0](#))
- 9) Monitor the LOCK pin on the Deserializer board. If the LOCK pin is HIGH, the Deserializer has locked into the Serializer.
- 10) After initialization, the camera PCLK clock and input data can begin transmission to the Serializer. The Serializer locks onto PCLK input (if present) otherwise the on-chip oscillator (25 MHz) is used as the input clock source. Note the MCU controller should monitor the LOCK pin and confirm LOCK = H before performing any I<sup>2</sup>C communication across the link.



## I<sup>2</sup>C Communication over Bi-directional Control Channel in Camera Mode

This section provides instructions for a simple I<sup>2</sup>C Read/Write transaction over the bi-directional control channel validating the interface between the host and Deserializer to Serializer.

- 1) Check the Deserializer SER DEV ID register 0x07 contents
- 2) The value entered in Deserializer register 0x07 sets the target Serializer device to communicate with. Load the Serializer slave address register.
- 3) Host controller to load and transmit data byte to Serializer address 0xB0
- 4) For verification purposes Serializer register 0x13 General-purpose register will be exercised for reading and writing data. Other Serializer registers can be programmed to check internal functions; such as register 0x03 b[0] TRFB.
- 5) Host controller to load and transmit write transaction to register byte 0x13 = 0xFF. Note default of register 0x13 = 0x00.
- 6) Host controller to read back Serializer 0xB0 register 0x13 = 0xFF

## Troubleshooting Demo Setup

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems. If the problem persists, please contact the local Sales Representative for assistance.

### QUICK CHECKS:

1. Check that Powers and Grounds are connected to both Serializer and Deserializer boards.
2. Check the supply voltage (typical 1.8V) and also current draw with both Serializer and Deserializer boards. The Serializer board should draw about 70mA with clock and all data bits switching at 43 MHz. The Deserializer board should draw about 100mA with clock and all data bits switching at 43 MHz.
3. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the selected rising/falling (RFB register) edge of the clock.
4. Check that the Jumpers and Switches are set correctly.
5. Check that the cable is properly connected.

## TROUBLESHOOTING CHART

Problem...	Solution...
There is only the output clock.	Make sure the data is applied to the correct input pin.
There is no output data.	Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both Serializer and Deserializer boards to make sure that the devices are enabled (PDB=Vdd) for operation.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the Serializer and Deserializer boards.
After powering up the demo boards, the power supply reads less than 1.8V when it is set to 1.8V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA minimum power supply is recommended.

Note: Please note that the following references are supplied only as a courtesy to our valued customers.  
It is not intended to be an endorsement of any particular equipment or supplier.

## Cable References

For optimal performance, we recommend Shielded Twisted Pair (STP) 100ohm differential impedance and 24 AWG (or larger diameter) cable for high-speed data applications.

Leoni Dacar 535 series cable:

[www.leoni-automotive-cables.com](http://www.leoni-automotive-cables.com)

Rosenberger HSD connector:

[www.rosenberger.de/en/Products/35\\_Automotive\\_HSD.php](http://www.rosenberger.de/en/Products/35_Automotive_HSD.php)

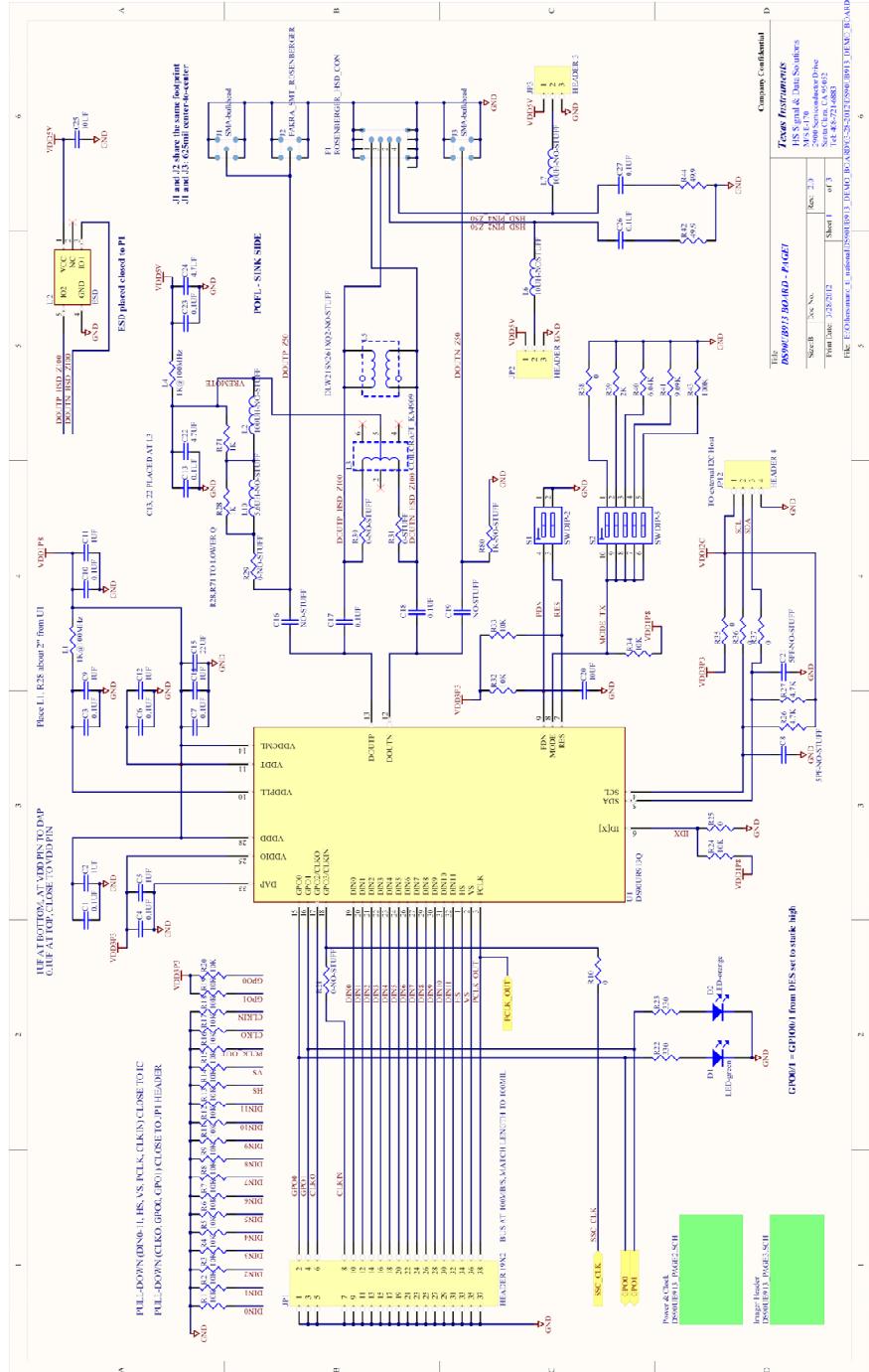
## Equipment References

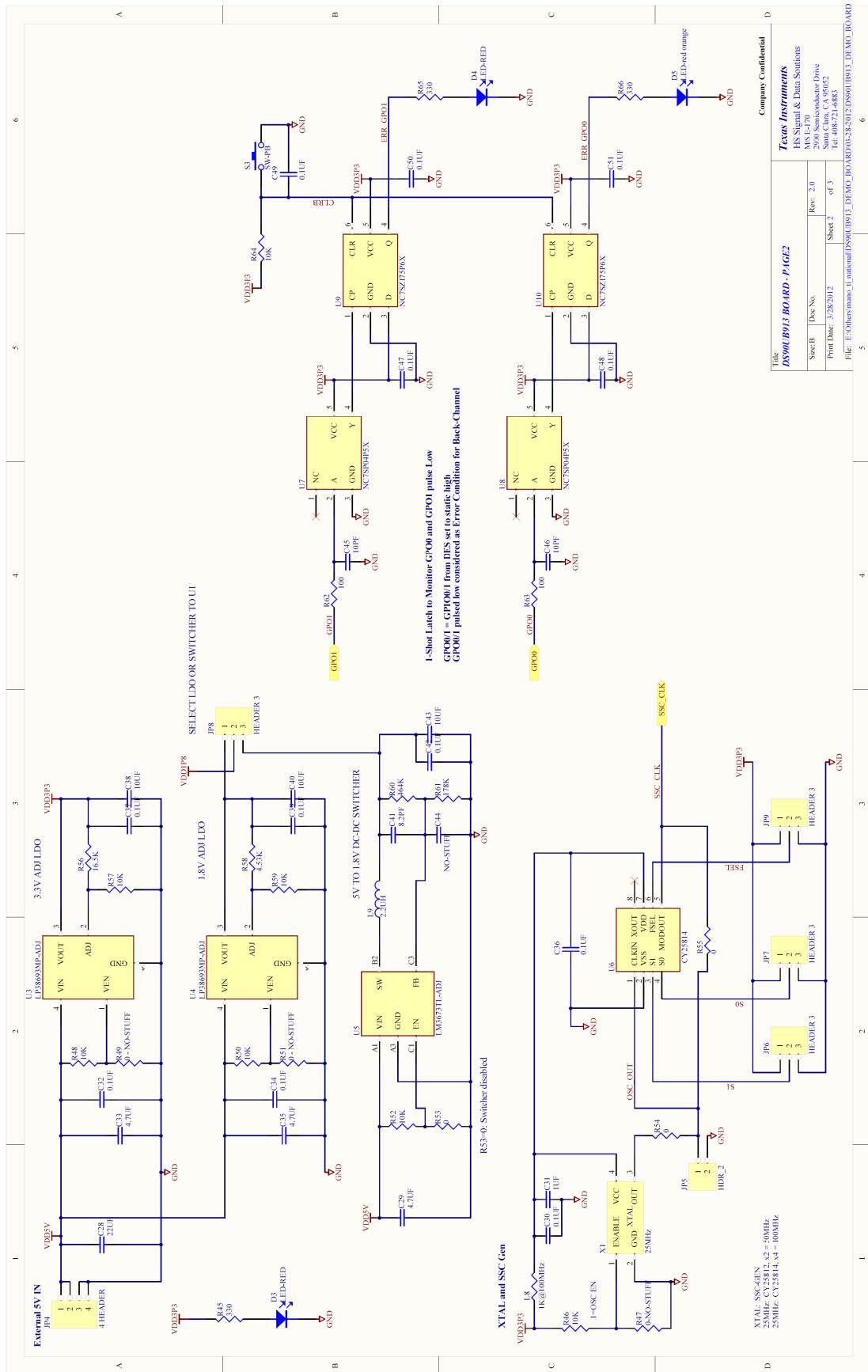
Corelis CAS-1000-I2C/E I2C Bus Analyzer and Exerciser Products:

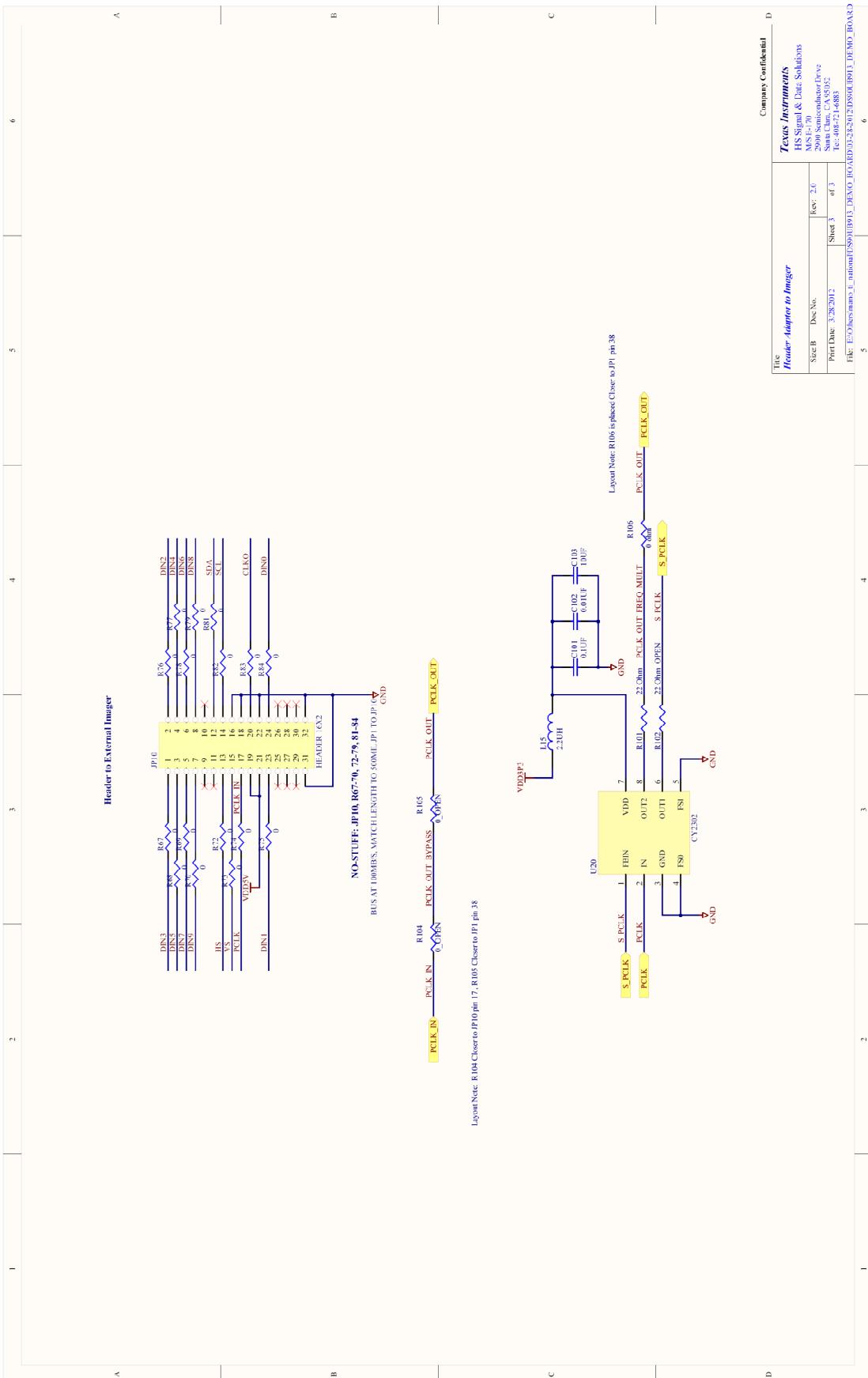
[www.corelis.com/products/I2C-Analyzer.htm](http://www.corelis.com/products/I2C-Analyzer.htm)

## Appendix

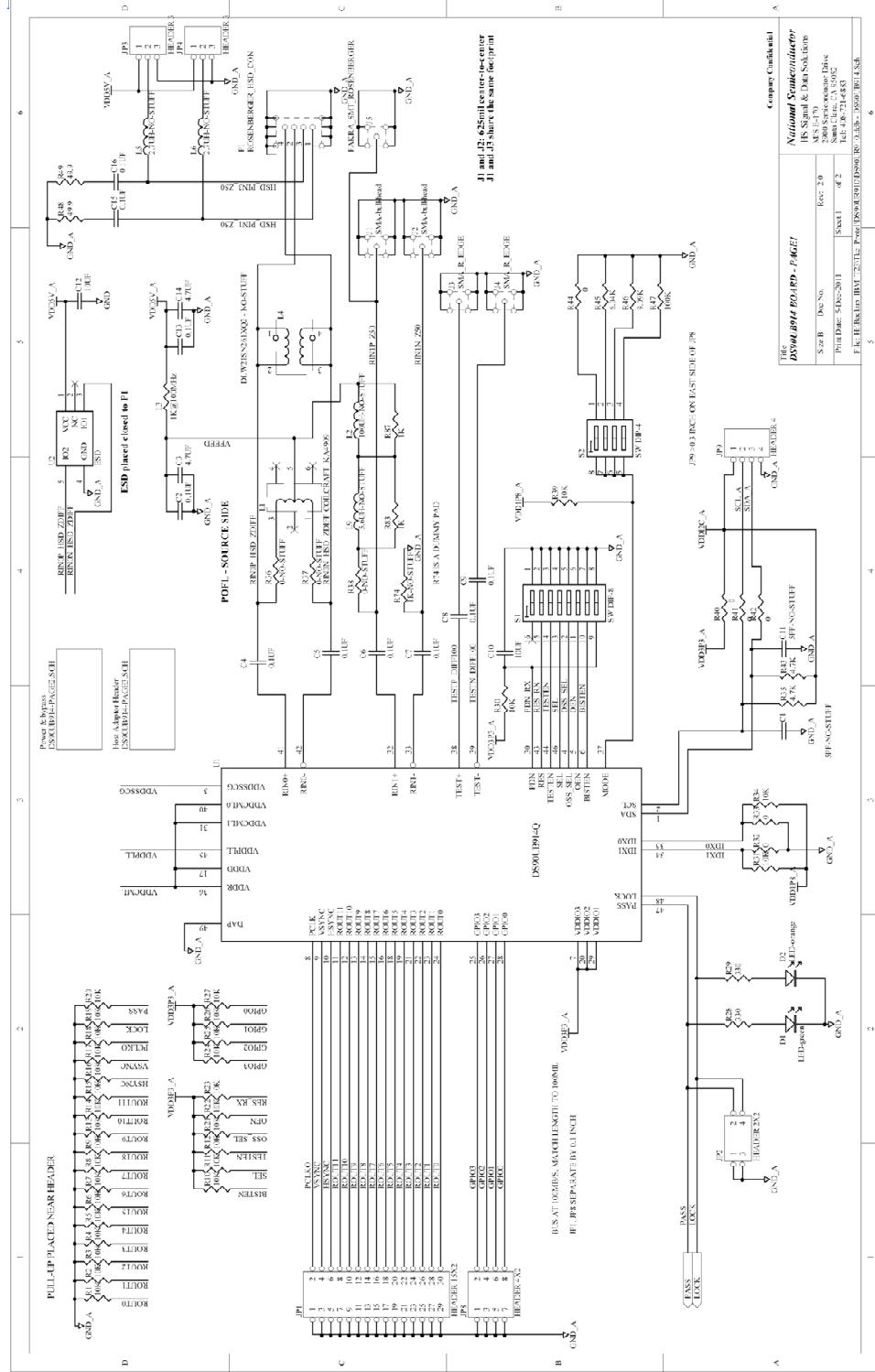
## DS90UB913Q EVK Schematic

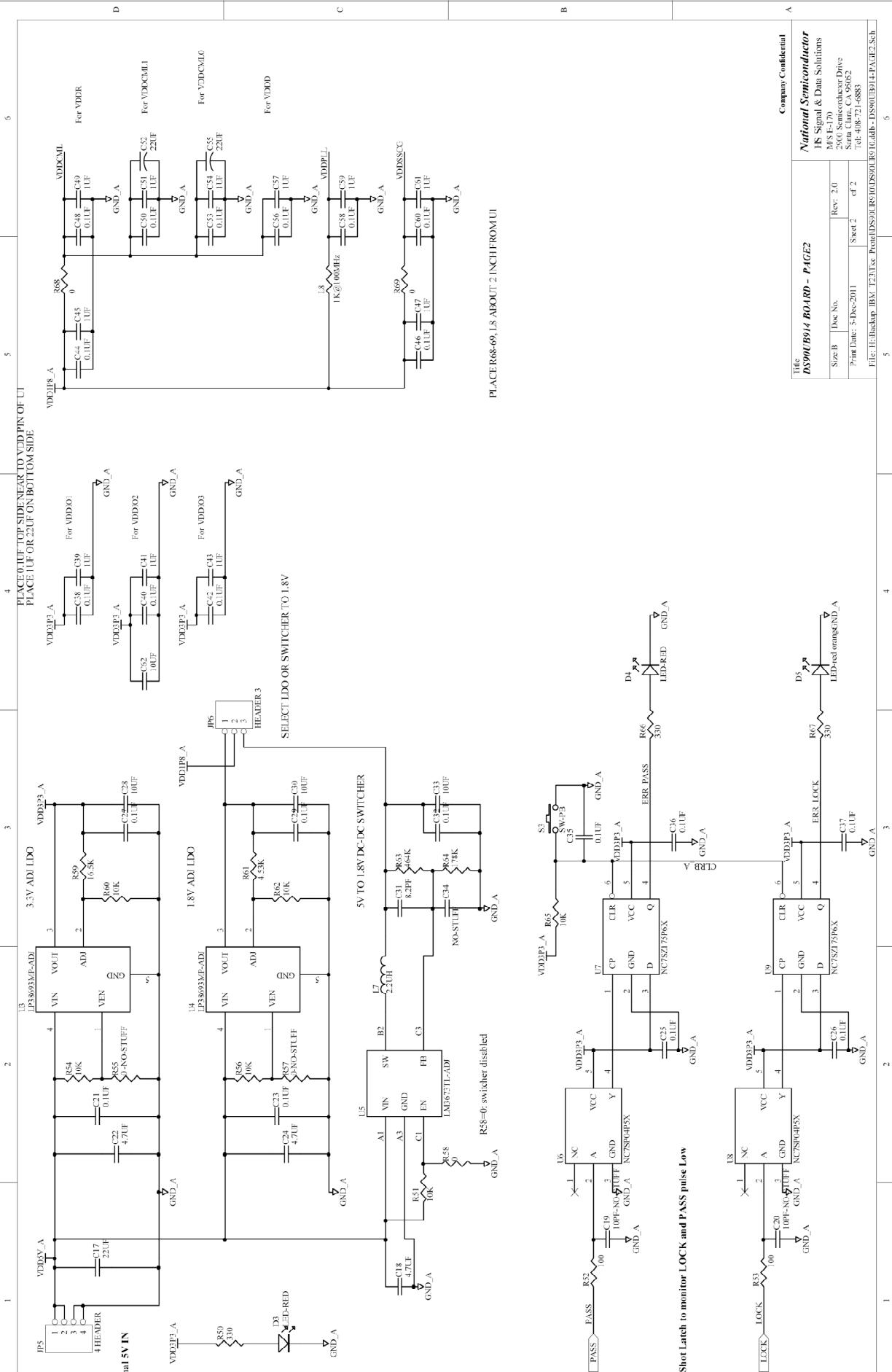


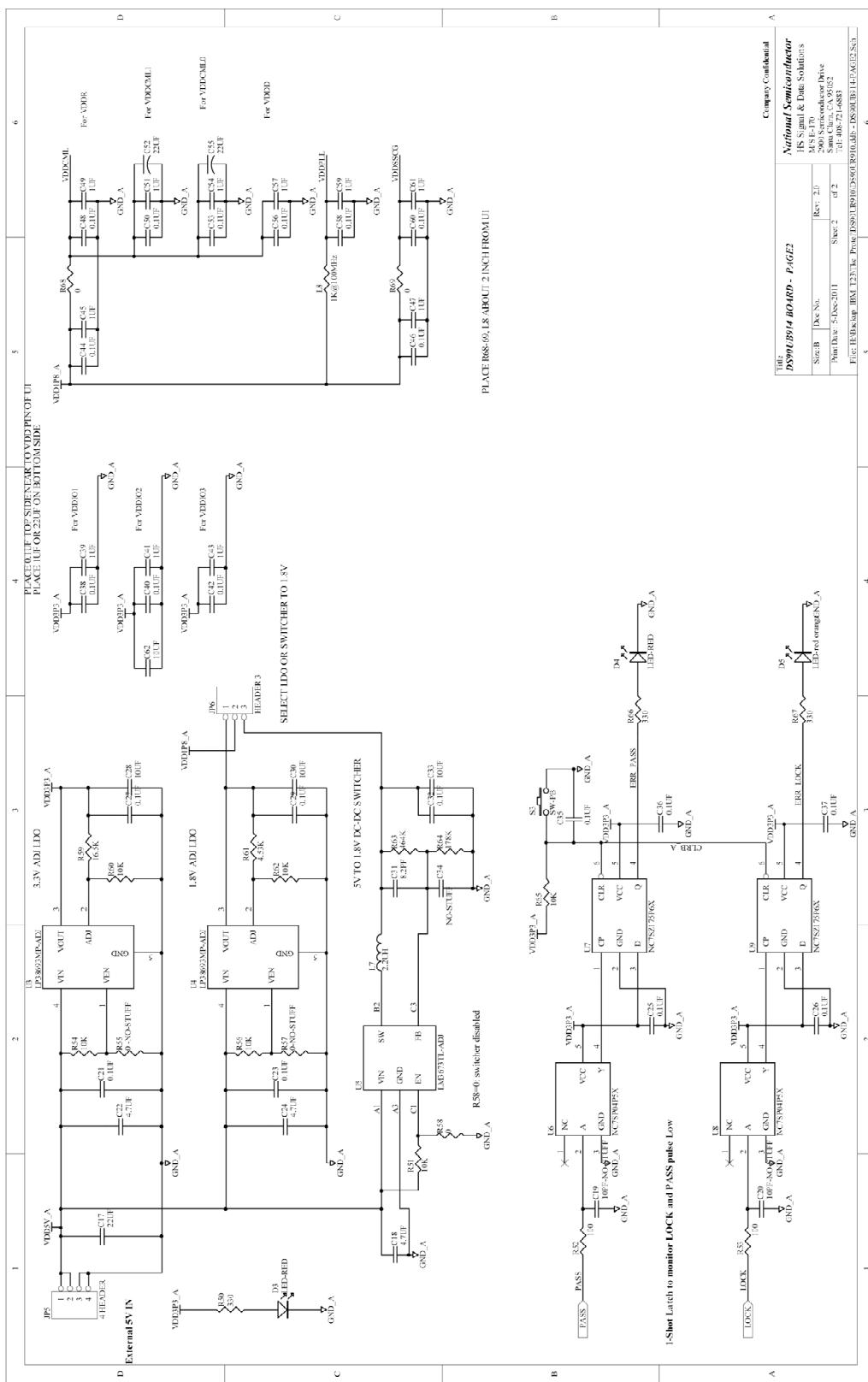


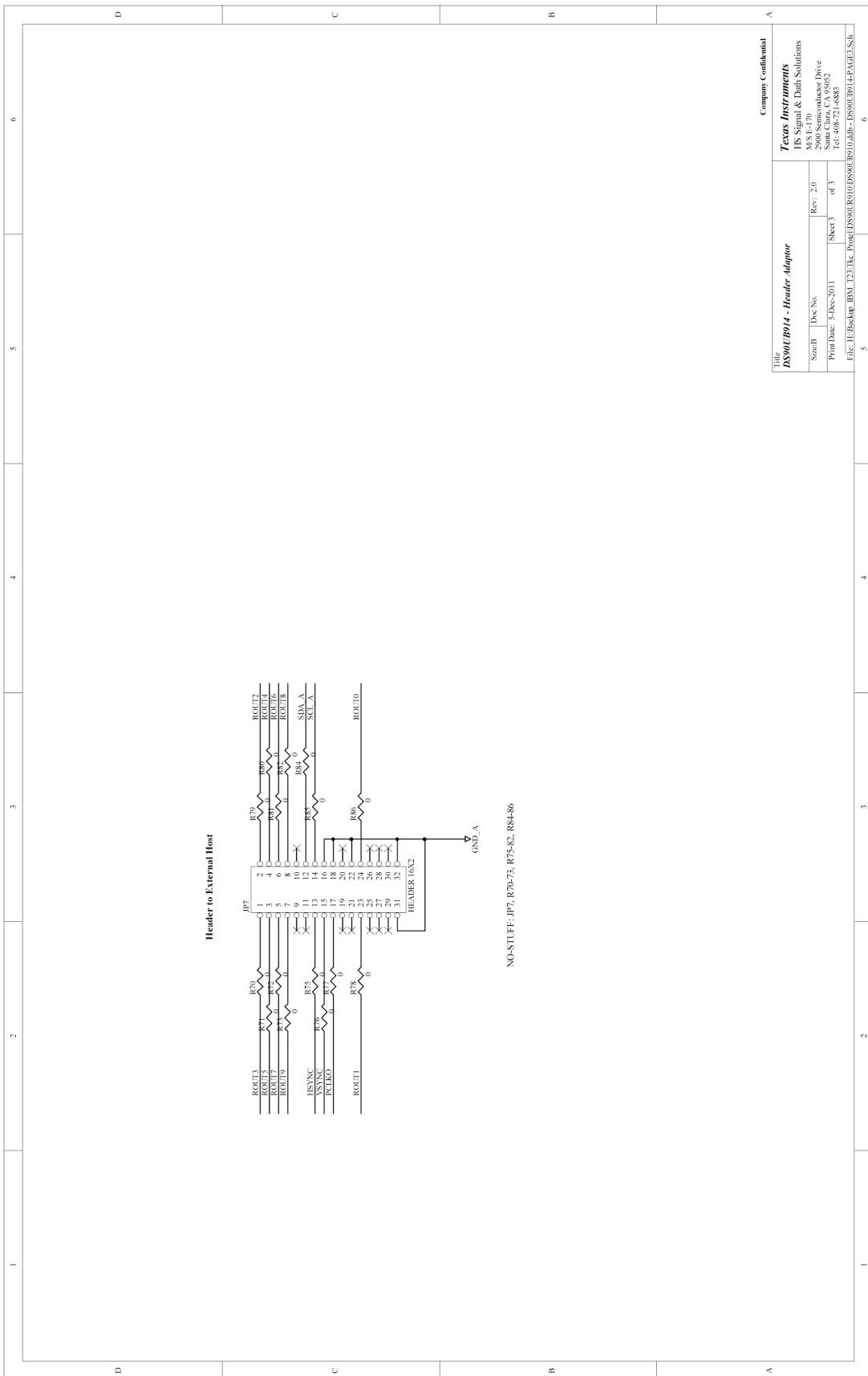


DS0011B0140 EWK Schematic

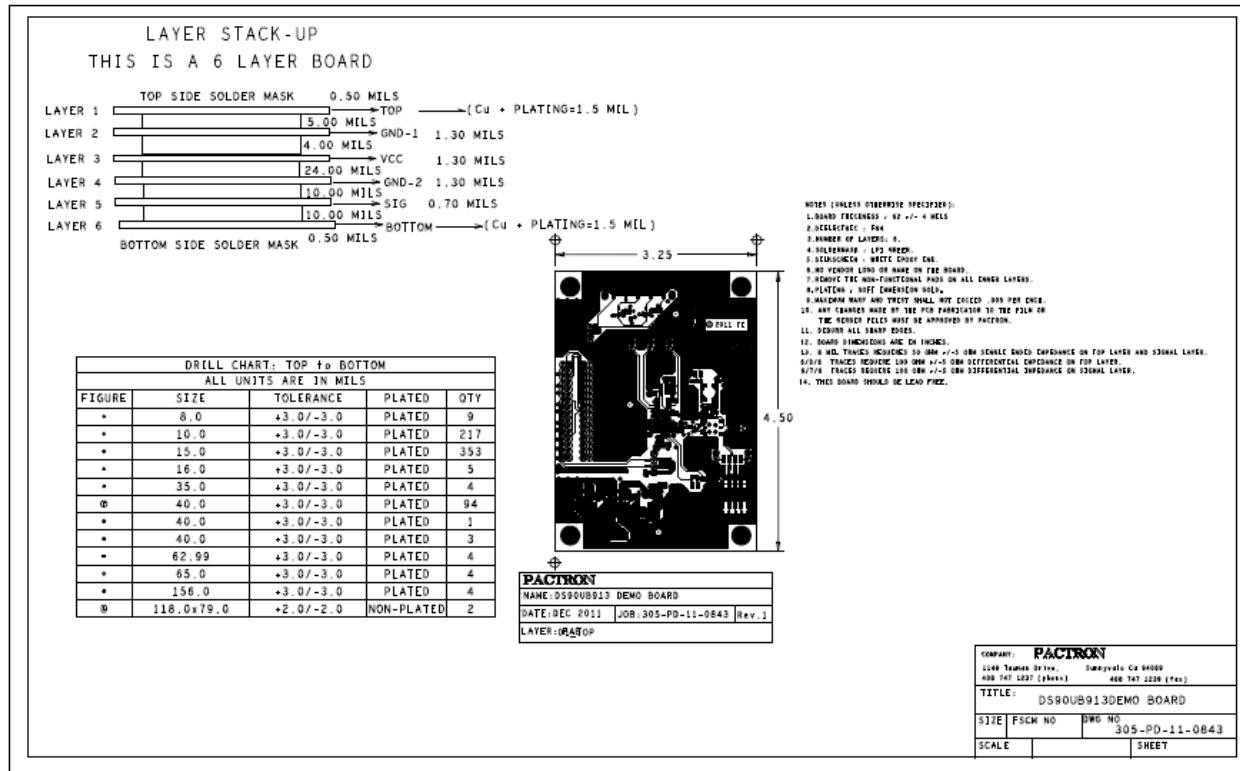


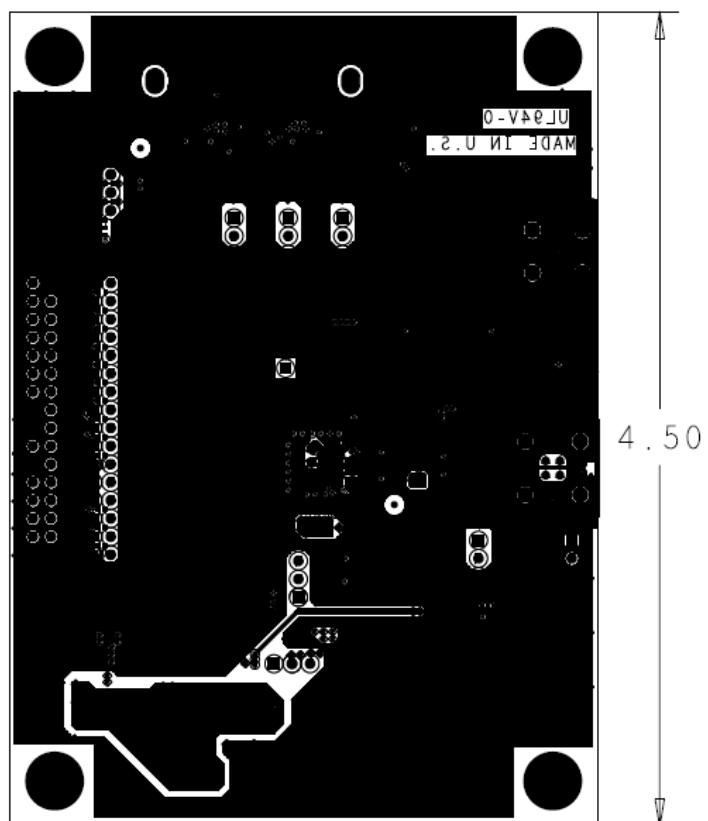
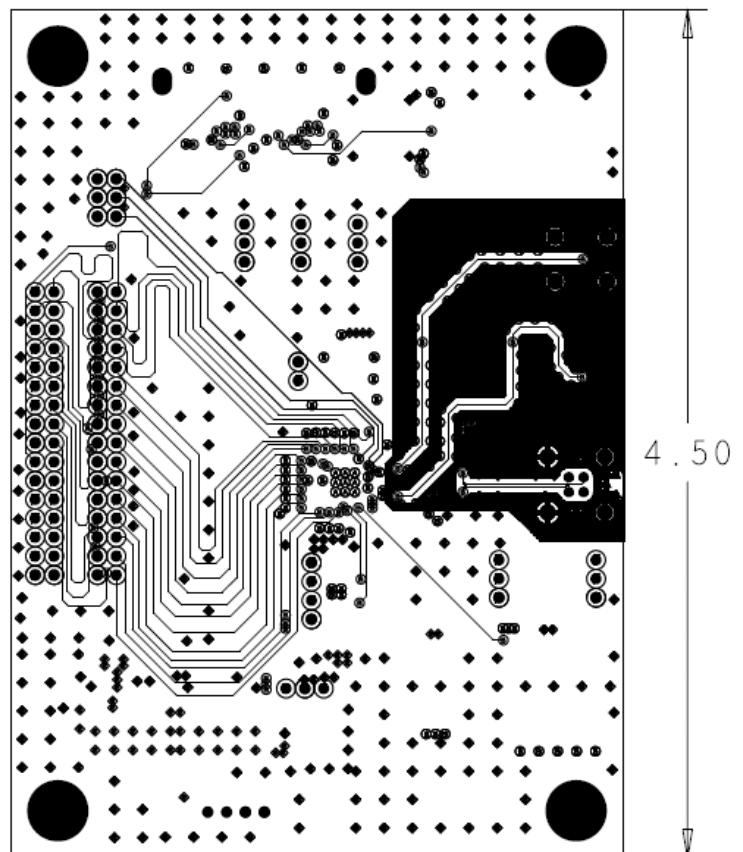




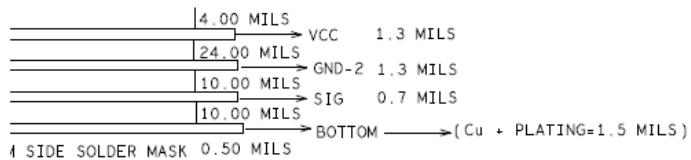


## DS90UB913Q PCB Layout

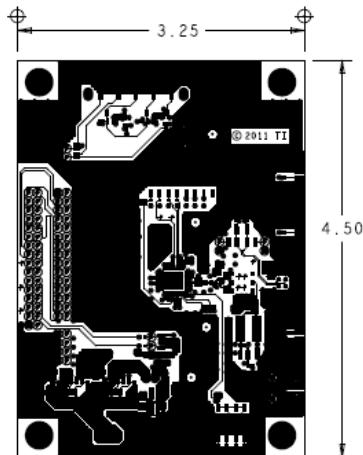




## DS90UB914Q EVK Layout



TOLL CHART: TOP to BOTTOM			
ALL UNITS ARE IN MILS			
E	TOLERANCE	PLATED	QTY
0	+3.0/-3.0	PLATED	9
0	+3.0/-3.0	PLATED	335
0	+3.0/-3.0	PLATED	312
0	+3.0/-3.0	PLATED	5
0	+3.0/-3.0	PLATED	4
0	+3.0/-3.0	PLATED	87
0	+3.0/-3.0	PLATED	3
0	+3.0/-3.0	PLATED	1
29	+3.0/-3.0	PLATED	4
0	+3.0/-3.0	PLATED	4
0	+2.0/-2.0	NON-PLATED	4
79.0	+2.0/-2.0	NON-PLATED	2



NOTES (UNLESS OTHERWISE SPECIFIED):  
 1. BOARD THICKNESS = .02 +/- .005 MILS  
 2. DIELECTRIC : FR4  
 3. NUMBER OF LAYERS: 6.  
 4. SOLDERMASK : LPI GREEN.  
 5. SILKSCREEN : WHITE EPOXY INK.  
 6. NO VENDOR LOGO OR NAME ON THE BOARD.  
 7. REMOVE THE NON-FUNCTIONAL PADS ON ALL INNER LAYERS.  
 8. PLATING : SOFT IMMERSION GOLD.  
 9. MAXIMUM WARP AND TWIST SHALL NOT EXCEED .005 PER INCH.  
 10. ANY CHANGES MADE BY THE PCB FABRICATOR TO THE FLM  
     THE GERBER FILES MUST BE APPROVED BY PACTRON.  
 11. DEBUR ALL SHARP EDGES.  
 12. BOARD DIMENSIONS ARE IN INCHES.  
 13. 8 MIL TRACES REQUIRES 50 OHM +/-5 OHM SINGLE ENDED  
     6/8/6 TRACES REQUIRE 100 OHM +/-5 OHM DIFFERENTIAL IMP  
     6/7/6 TRACES REQUIRE 100 OHM +/-5 OHM DIFFERENTIAL IMP  
 14. THIS BOARD SHOULD BE LEAD FREE.

PACTRON			
NAME: DS90UB914 DEMO BRD			
DATE: DEC 2011	JOB: 305-PD-11-0844	Rev. 1	
LAYER: 01_ETOP			

COMPANY:

