

ONET4201LD/ONET4211LD 4.25Gbps Laser Driver EVM User Guide

The ONET4201LD and ONET4211LD are laser drivers for fiber optic applications up to 4.25Gbps. The ONET4201LD has active back termination at the outputs while the ONET4211LD has standard terminations. All other functionality between the devices is the same. The laser drivers accept CML input data and provide bias and modulation currents for driving a laser diode. Laser bias current automatic power control (APC), temperature compensation of modulation current, fault detection, and current monitor features are also provided. The laser drivers have two fault modes: hard-fault and soft-fault. In hard-fault mode, the bias and modulation currents are disabled when a fault is detected. In soft-fault mode, the fault detection flag is set but the bias and modulation currents are not disabled.

The evaluation module (EVM) is designed to demonstrate the electrical performance of the devices.

Rev. A September 2005



Contents

1.	General Description	3			
2.	Operation				
	2.1. Open Loop Mode (APC Disabled) with Soft Fault				
	2.2. APC Mode with Soft-Fault				
	2.3. Setting Hard-Fault Mode				
3.	Schematic				
4.	Measurement Results	9			
	Figures				
Figu	ure 1: ONET4201LD EVM	3			
Figu	Figure 2: Bias and Modulation Current Adjustment Potentiometers for Open Loop Operation				
Figu	ure 3: Bias and Modulation Current Adjustment Potentiometers in APC Mode	7			
Figu	ure 4: ONET4201LD/ONET4211LD Schematic	8			
	ure 5: ONET4201LD at 4.25Gbps with K28.5 Pattern, I _{MOD} = 40mA				
Figu	ure 6: ONET4201LD at 2.125Gbps with K28.5 Pattern, I _{MOD} = 40mA	9			
Figu	ure 7: ONET4201LD at 1.0625Gbps with K28.5 Pattern, I _{MOD} = 40mA	10			



1. General Description

The Texas Instruments ONET4201LD/ONET4211LD EVM is designed to provide the ability to accurately measure the electrical performance of the ONET4201LD or ONET4211LD 4.25Gbps laser drivers. The EVM transforms the 20Ω impedance at the modulation current outputs (MOD+ and MOD-) to the 50Ω impedance used by the electrical test and measurement equipment. The modulation current output is AC coupled so that the full dynamic range of the oscilloscope or communications system analyzer can be used. The top view of the EVM is shown in Figure 1.

Potentiometers are provided to adjust the modulation current (P38 and P39), bias current (P31 and P35 in open loop mode and P29 and P33 in APC mode), bias current monitor (P3 and P4), photodiode current monitor (P1 and P2) and modulation temperature coefficient (P30 and P34).

To quickly test the laser driver, the EVM has a default setting of: APC mode with soft-fault, IBMAX of 50mA, I_{BIAS} of 40mA and I_{MOD} of 40mA. The modulation temperature coefficient resistor, RMODTC, can be adjusted if the modulation current is going to be tested over temperature.

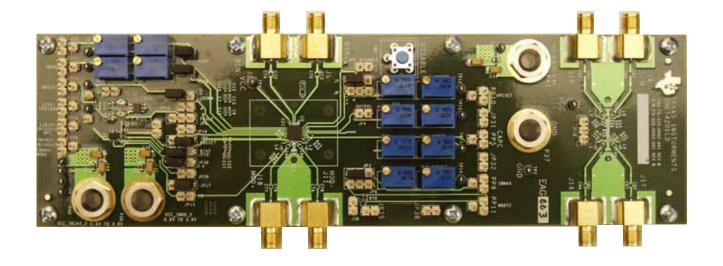


Figure 1: ONET4201LD EVM

2. Operation

2.1. Open Loop Mode (APC Disabled) with Soft Fault

The ONET4201LD and ONET4211LD have automatic power control to maintain a constant bias current with temperature and aging. When actually driving a laser, this is typically done by connecting the output of the laser monitor photodiode to PD (pin 19). The EVM includes a photodiode emulation circuit that, when enabled, will source a pseudo photodiode current to PD. In open loop mode, the APC is disabled and there is no current being sourced to PD and IBMAX is used to set the bias current.



When a fault occurs in soft-fault mode, the fault detection flag, SDOWN, is set high but the bias and modulation currents are not disabled. The SDOWN output goes low once the fault condition disappears. For evaluation, it is recommended to use soft-fault mode.

Step 1: Set Jumpers:

Short JP1 Pin 2 to Pin 3 (connect APCSET to VCC via a $2k\Omega$ resistor to disable the APC loop)

Short JP3 Pin 2 to Pin 3 (connect IBMAX to potentiometer to adjust the bias current)

Short JP5 Pin 2 to Pin 1 (connect MODSET potentiometer to adjust the modulation current)

Short JP8 Pin 2 to Pin 3 (set FLTMODE high for soft-fault mode)

Short JP9 Pin 2 to Pin 3 (activate fault indication LED controlled by SDOWN)

Short JP10 (used to set fault point for MONP)

Short JP11 (used to set fault point for MONB)

Short JP16 Pin 2 to Pin 3 (configure I_{BIAS} for open loop operation)

Short JP17 Pin 2 to Pin 1 (connect MOD+ & MOD- termination resistors to VCC IMOD 2)

Short JP30 Pin 2 to Pin 3 (connect BIAS to the VCC IBIAS 2 Power Supply)

Step 2: Adjust Potentiometers:

Rotate potentiometers P31 (course adjust) and P35 (fine adjust) fully clockwise to minimize the bias current.

Rotate potentiometers P38 (fine adjust) and P39 (course adjust) fully clockwise to minimize the modulation current.

Rotate potentiometers P3 (fine adjust) and P4 (course adjust) fully clockwise to set the MONB fault point at its lowest level.

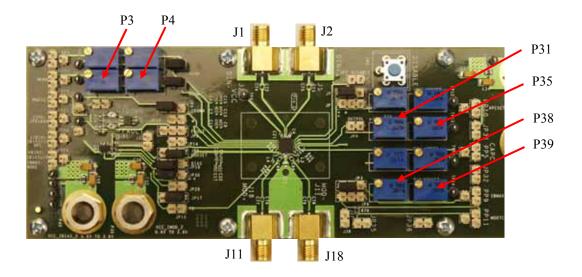


Figure 2: Bias and Modulation Current Adjustment Potentiometers for Open Loop Operation



Step 3: Connect Data Inputs and Modulation Current Outputs

Connect the data source to SMA connectors J1 and J2 which provide the connections to the device data inputs DIN+ and DIN- respectively. The cables should be phase matched to avoid duty cycle distortion. DIN+ and DIN- are AC coupled (C73 in parallel with C75 and C72 in parallel with C74) and are each terminated to 50Ω within the device.

The SMA connectors J11 and J18, which respectively provide the connection to the MOD- and MOD+ modulation current outputs, should be connected to an oscilloscope with 50Ω input impedance. The outputs are AC coupled (C78 in parallel with C79 and C76 in parallel with C77) and terminated into 25Ω in parallel with 87.5Ω (37.5 Ω in series with the 50Ω impedance of the test equipment) providing approximately 20Ω termination for the device.

Step 4: Connect DC Power Supplies

The power supply voltages are provided by 4 banana connectors. The power supplies for the VCC pins, the modulation current outputs and the laser bias current outputs are provided separately so that the individual currents can easily be measured. All of the power supply currents return to a common ground.

Configure the power supplies according to the table below.

Connector	Name	Supply Voltage (V)	Supply Current (mA)
P41	VCC	3 to 3.6	70
P36	VCC_IMOD_2	2.8 to 3.6	100
P40	VCC_IBIAS_2	2.8 to 3.6	120
P37	GND	Ground	

Step 5: Set the Bias and Modulation Currents

Rotate potentiometers P38 and P39 counterclockwise to increase the modulation current. Fine resolution of the modulation amplitude can be achieved by adjusting P38. The modulation current can be directly read from the VCC_IMOD_2 power supply or using an ammeter.

SDOWN LED D2 should be off.



Rotate potentiometers P31 and P35 counterclockwise to increase the bias current. Fine resolution of the bias current can be achieved by adjusting P35. The bias current can be directly read from the VCC_IBIAS_2 power supply or using an ammeter. LED D2 will come on as the bias current is increased.

To set the bias current fault point, rotate potentiometers P3 and P4 counterclockwise until LED D2 just goes off. Any increase in bias current from that set above, will cause the LED to come on.

2.2. APC Mode with Soft-Fault

To set the EVM in APC mode, closed loop control is required using APCSET and PD. The function of the IBMAX pin changes in APC mode. The bias current that flows when IBMAX is set in the open-loop mode now becomes the maximum allowed bias current. When the APC loop goes to this maximum bias current a fault will be generated.

Step 1: Set IBMAX

Follow steps 1 through 5 in section 2.1 and set the maximum bias current in open loop mode. This IBMAX setting now defines the maximum bias current in the APC mode. A bias current setting of 100mA avoids causing a fault when exercising the full bias current range using APCSET.

Step 2: Set Jumpers and Minimize Bias Current

The following jumpers need to be set differently from that in section 2.1:

Short JP1 Pin 2 to Pin 1 (enables adjustment of the bias current using APCSET) Short JP7 Pin 2 to Pin 3 (connect APCSET to potentiometers P29 and P33) Short JP15 (connect PD to the photodiode emulation circuit) Short JP16 Pin 2 to Pin 1 (configure I_{BIAS} for closed loop APC operation)

Short 31 To 1 in 2 to 1 in 1 (configure 181AS for closed 1909 111 c operation)

Rotate potentiometers P29 (course adjust) and P33 (fine adjust) fully clockwise to minimize the bias current.

Rotate potentiometers P1 (fine adjust) and P2 (course adjust) fully counterclockwise to set the MONP fault point at its highest level, avoiding a fault triggered by high photodiode current.



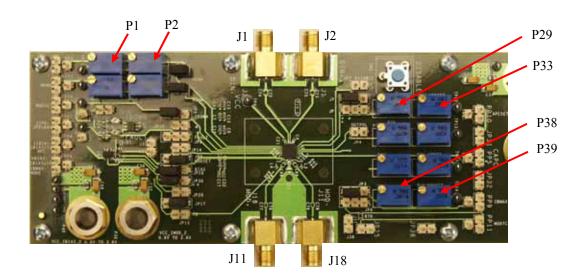


Figure 3: Bias and Modulation Current Adjustment Potentiometers in APC Mode

Step 3: Set the Bias and Modulation Currents

Rotate potentiometers P29 and P33 counterclockwise to increase the bias current. Fine resolution of the bias current can be achieved by adjusting P33. The modulation current can be directly read from the VCC_IBIAS_2 power supply or using an ammeter. The bias current can not be adjusted higher than IBMAX set in step 1.

Rotate potentiometers P38 and P39 counterclockwise to increase the modulation current or clockwise to decrease the modulation current. Fine resolution of the modulation amplitude can be achieved by adjusting P38. The modulation current can be directly read from the VCC_IMOD_2 power supply or using an ammeter.

Potentiometers P1 and P2 can be rotated clockwise to set a fault point for MONP if desired

2.3. Setting Hard-Fault Mode

To set hard-fault mode, short JP8 Pin 2 to Pin 1 which grounds the FLTMODE pin. The same functionality as in sections 2.1 and 2.2 can be achieved; however, a fault will now disable the bias and modulation currents. Once the reason for the fault has been corrected, the device fault condition can be cleared by pressing and releasing the disable pushbutton SW2.

For more detailed information on the operation of the ONET4201LD or ONET4211LD, please refer to the respective data sheet.



3. Schematic

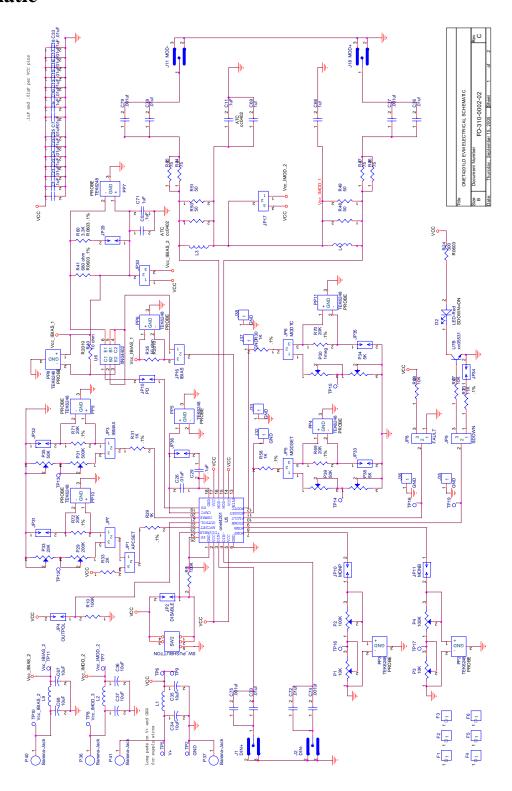


Figure 4: ONET4201LD/ONET4211LD Schematic



4. Measurement Results

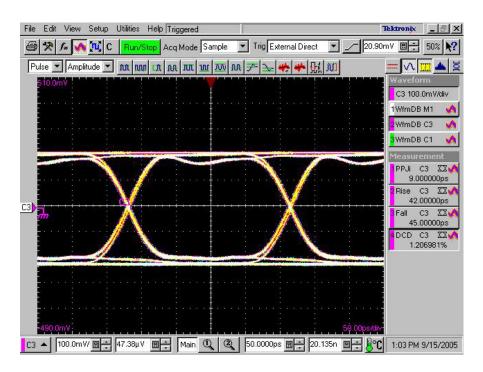


Figure 5: ONET4201LD at 4.25Gbps with K28.5 Pattern, $I_{MOD} = 40$ mA

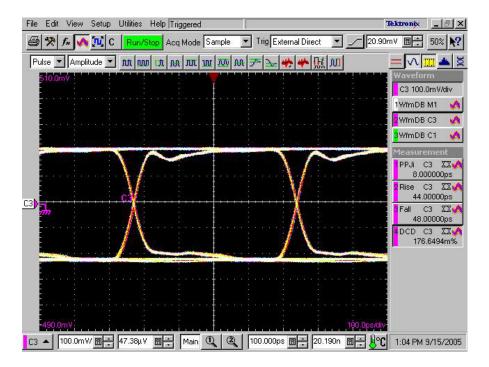


Figure 6: ONET4201LD at 2.125Gbps with K28.5 Pattern, $I_{MOD} = 40$ mA



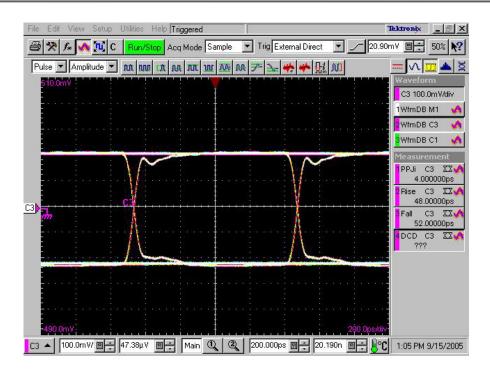


Figure 7: ONET4201LD at 1.0625Gbps with K28.5 Pattern, $I_{MOD} = 40mA$