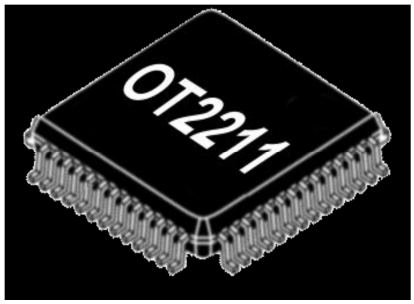
OT2211

KM Switch & Data Bridge Controller

Revision: R2
Date: 2016/9/20



Ours Technology Inc. OT2211 Datasheet

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DESCRIPTION

The OT2211 is a single chip, cost-effective, and high- performance USB2.0 Mass Storage Class Peripheral controller targeted for applications of data transfer, keyboard and mouse sharing between PCs. The design complies with USB High Speed Specification (480Mb/s), Version 2.0.

The OT2211 has two USB interfaces for connecting two PCs. With stable clock slew-rate control, the controller can reduce the EMI issue.

The controller has one dedicated LED control pin and one optional LED control pin(GPIO). The LED display modes - operation, suspend, and standby, are programmable through the production program provided by Oti.

More Value-added application software for data transfer and file, e-mail synchronization are available.

This controller can operate on Windows 10, Windows 8 Windows Vista, Windows 7, Win XP, and Win2000

The OT2211 is available in cost-saving 48-pin LQFP (7mm X 7mm) package

APPLICATIONS

- On Mother-Board design
- KM Link Cable

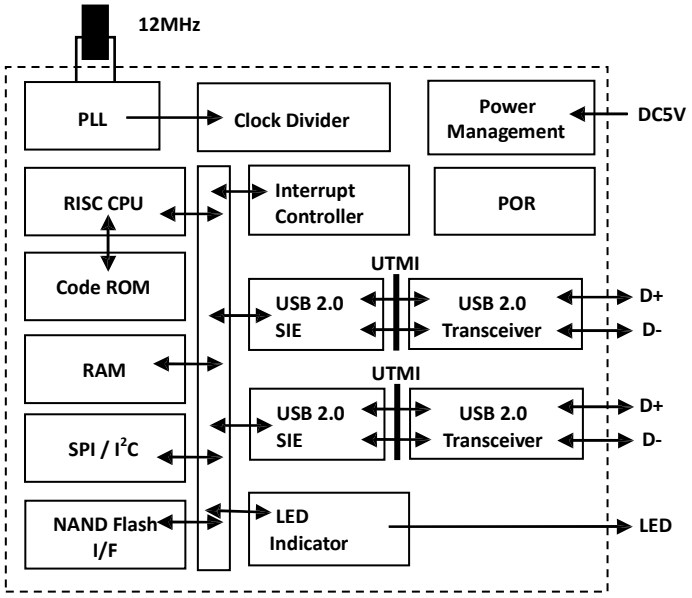
FEATURES

- Integrated two USB transceivers
- Conforms to USB HID Specification, Version 1.1, 2.0
- Conforms to high-speed (480Mb/s) USB Specification, Version 2.0 and meets the bus power specification
- Mass storage class controller with Universal Serial Bus interface
- Integrated RISC micro-controller with high-performance RISC architecture for single cycle instruction execution
- 12 MHz external clock
- Integrated regulator for 5/3.3/1.8V power operation
- Internal power on reset function
- Integrated PLL
- Integrated SPI/I2C interface
- Support Serial Nor-Flash for storing the software AP
- Support CD-ROM/CD-RW Auto-Run feature
- Configurable Vendor ID/Product ID (VID/PID)
- OS Supported :

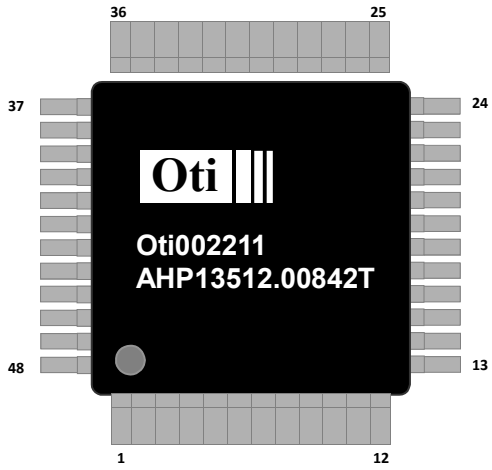
✓ Windows 10, Windows 8 ,Window 7, Window Vista, Window XP, Win2000.

- Small form factor - standard 48-pin LQFP (7mmX7mm) package

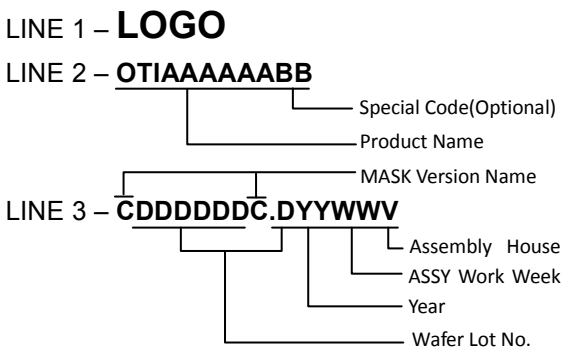
BLOCK DIAGRAM



PIN CONFIGURATION – 48 PIN LQFP



MARKING INFORMATION



PIN TABLE

PIN	PIN NAME	ATTRIBUTE	PIN	PIN NAME	ATTRIBUTE	PIN	PIN NAME	ATTRIBUTE
1	power_dect0	I	17	VDD18	P	33	VS33P_phy1	G
2	power_dect1	I	18	VSS	G	34	PADXIN_phy1	Analog I
3	LED1_oeb	O	19	VDD33	P	35	PADXOUT_phy1	Analog O
4	VDD33	P	20	F0_IO[4]	I/O	36	VDDU_phy1	P
5	REXT_phy0	Analog O	21	F0_IO[5]	I/O	37	VDD18	P
6	VD33P_phy0	P	22	F0_IO[6]	I/O	38	VSS	G
7	PADDP_phy0	Analog I/O	23	F0_IO[7]	I/O	39	VDD33	P
8	PADDN_phy0	Analog I/O	24	GPO_0	O	40	GPO_6	O
9	VS33P_phy0	G	25	VSS	G	41	GPO_7	O
10	PADXIN_phy0	Analog I	26	VDD33	P	42	GPIOA_2	I/O
11	PADXOUT_phy0	Analog O	27	GPIOA_5	I/O	43	GPIOA_3	I/O
12	VDDU_phy0	P	28	GPIOA_6	I/O	44	AGND_REG	G
13	F0_IO[0]	I/O	29	REXT_phy1	Analog O	45	VOUT18	P
14	F0_IO[1]	I/O	30	VD33P_phy1	P	46	VBUS	P
15	F0_IO[2]	I/O	31	PADDP_phy1	Analog I/O	47	VBUS	P
16	F0_IO[3]	I/O	32	PADDN_phy1	Analog I/O	48	VOUT33	P

PIN DESCRIPTIONS

SYSTEM			
USB INTERFACE			
Pin Number	Pin Name	State	Description
		Default	
7	PADDP_phy0	Hi-Z	USB D+
8	PADDN_phy0	Hi-Z	USB D-
31	PADDP_phy1	Hi-Z	USB D+
32	PADDN_phy1	Hi-Z	USB D-

APPLICATION				
Pin Number	Pin Name	State		Description
		Default	Active	
1	power_dect0	Low	High	Used for the detection of the power connection of phy0
2	power_dect1	Low	High	Used for the detection of the power connection of phy1
3	LED1_oeb	Hi-Z	X	LED enable/disable
5	REXT_phy0	X	X	Analog signal for USB PHY 0
14	F1	Hi-Z	High	Control signal for application
29	REXT_phy1	X	X	Analog signal for USB PHY 1

CLOCK INTERFACE			
Pin Number	Pin Name	State	Description
		Default	
10	PADXIN_phy0	Low	Crystal connection
11	PADXOUT_phy0	High	Crystal connection
34	PADXIN_phy1	Low	Crystal connection
35	PADXOUT_phy1	High	Crystal connection

POWER		
Pin Number	Pin Name	Description
17, 37	VDD18	Digital Core Power with 1.8V input
18, 38	VSS	Digital Ground
4, 19, 26, 39	VDD33	Digital IO Power with 3.3V input
45	VOUT18	Regulator Power with 1.8V output
46, 47	VBUS	Regulator Power with 5V input
48	VOUT33	Regulator Power with 3.3V output

6	VD33P_phy0	3.3V Analog Power for PHY0
9	VS33P_phy0	Analog Ground for PHY0
12	VDDU_phy0	1.8V Digital Power for PHY0
30	VD33P_phy1	3.3V Analog Power for PHY1
33	VS33P_phy1	Analog Ground for PHY1
36	VDDU_phy1	1.8V Digital Power for PHY1

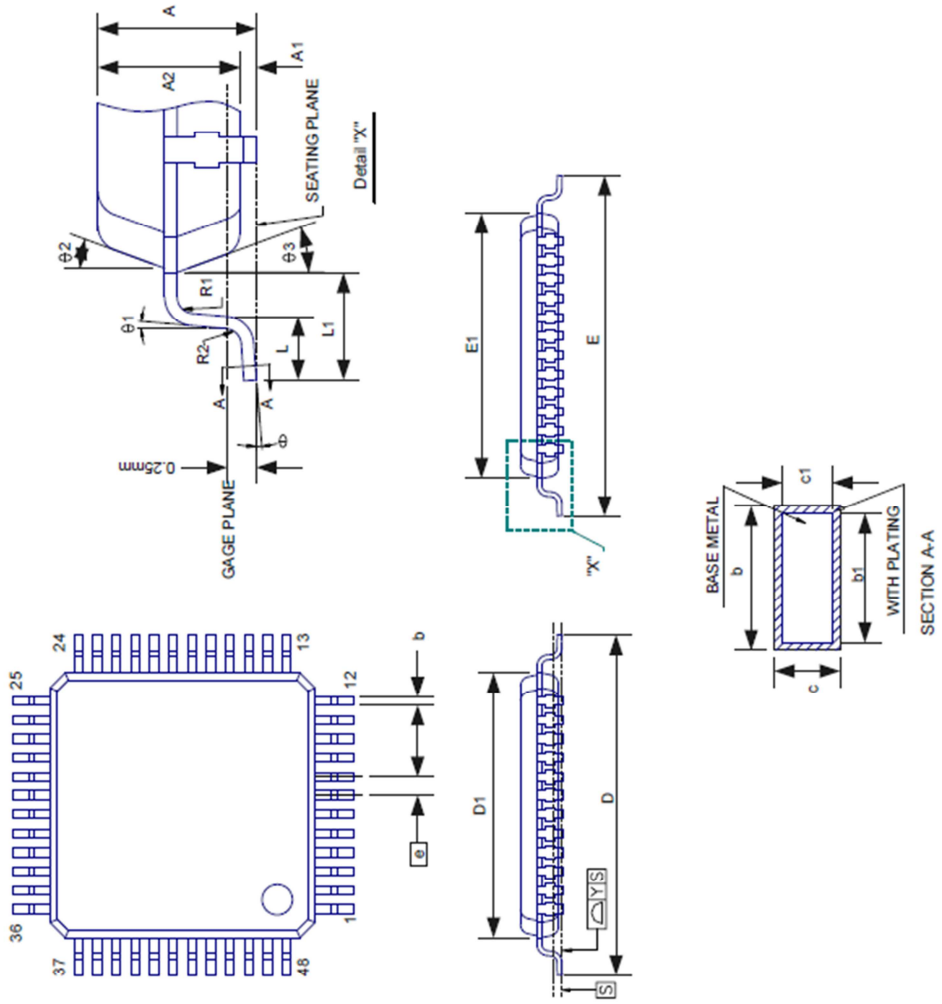
GPIO			
Pin Number	Pin Name	State	Description
		Default	
24	GPO_0	High	General Purpose I/O
27	GPIOA_5	Hi-Z	General Purpose I/O
28	GPIOA_6	Hi-Z	General Purpose I/O
40	GPO_6	High	General Purpose I/O
41	GPO_7	High	General Purpose I/O
42	GPIOA_2	Hi-Z	General Purpose I/O
43	GPIOA_3	Hi-Z	General Purpose I/O

DC ELECTRICAL CHARACTERISTICS

ITEMS	SYMBOL	MIN.	TYP.	MAX.	UNIT
DC Power Supply	V_{BUS}	+4.5	5.0	+5.5	V
DC Power Supply	V_{DD33}	3.0	3.3	3.6	V
DC Power Supply	V_{DD18}	1.62	1.8	1.98	V
Input Low Voltage	V_{IL}	-0.3		0.8	V
Input High Voltage	V_{IH}	2.0		3.6	V
Threshold Point	V_T	1.2	1.3	1.4	V
Output Low Voltage @ IOL = 8mA	V_{OL}			0.4	V
Output High Voltage @ IOH = 8mA	V_{OH}	2.4			V
Pull-up Resistor	R_{PU}	34K	41K	64K	Ω
Pull-down Resistor	R_{PD}	33K	44K	79K	Ω
Operating Temperature	Ta	-40		+85	°C
Storage Temperature	Tst	-55		+150	°C

PACKAGE OUTLINE

Figure 1 - LQFP-48 Package



NOTE:

1. Refer to JEDEC MS-026

2. Dimension D1 and D1 do not include mold protrusion.

3. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimension including mold mismatch. Dimension l0 does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum l0 dimension by more than 0.08mm.

4. All dimensions in millimeters.

48 PIN LQFP PACKAGE PARAMETERS

SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A		1.4	1.6		55	63
A1	0.05		0.15	2		6
A2	1.35	1.4	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.2	0.23	7	8	12
c	0.09		0.2	4		8
c1	0.09		0.16	4		6
D	9.00BSC			354BSC		
D1	7.00BSC			276BSC		
E	9.00BSC			354BSC		
E1	7.00BSC			276BSC		
e	0.5BSC			20BSC		
L	0.45	0.6	0.75	18	24	30
L1	1.00REF			39REF		
R1	0.08			3		
R2	0.08		0.2	3		8
Y			0.075	3.5	7	3
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°			0°		
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°