Section 4:

```
InitTable[Address, Value] = {
                {0xFF, 0x00} ,//Page 0 select
                {0x09, 0x36} ,//Enable X-Mode
                {0x0A, 0x7B} , //Disable HPD_SNK pass thru to HPD_SRC.
                //{0x0D, 0x80} , //Enable clock on AUX. Select 1/20 mode.
                {0x0D, 0xC0},           // Clock on AUX is 1/40 datarate and enabled.
                {0x0C, 0x6D} , //Set TX Swing to Max
                //{0x0C, 0x00},           // Set TX Swing to NOM
                {0x10, 0x00} , //Turn off pattern verifier
                {0x16, 0xF1} , //Disable char-alignment on all lanes.
                {0xFF, 0x01} , // Select Page 1
                //CONFIGURE PLL BLOCK
                {0x00, 0x02} , //Enable Bandgap.
                {0x04, 0x80} , //PLL_FBDIV[7:0]
                {0x05, 0x00} , //PLL_FBDIV[10:8]
                {0x08, 0x00} ,
                {0x0D, 0x02} , //Select LN0 for clock.
                {0x0E, 0x03} , //CDR_CONFIG[4:0]. FIXED, LN0.
                {0x01, 0x01} , //CP_EN is PLL mode
                {0x02, 0x3F} , //CP_CURRENT is high.
                {0x0B, 0x33} , //Loop Filter to 8K.
                {0xA1, 0x02} , //Allows for Override of PLL settings.
                {0xA4, 0x02} , //Allows for Override of PLL settings.
                //CONFIGURE TX BLOCK
                {0x10, 0xF0} , //ENTX for all four lanes (disable)
                {0x11, 0x30} , //TX_RATE is Full Rate, TX_TERM = 75 to 150 , TX_INVPAIR
                = None
                {0x14, 0x00} , //HDMI_TWPST1 is 0dB pre-emphasis
                {0x12, 0x03} , //SLEW_CTRL is Normal, SWING is 600mV.
                {0x13, 0xFF} , //FIR_UPD. Load TX settings
                {0x13, 0x00} ,
                //CONFIGURE RX BLOCK
                {0x30, 0xE0} , //Disable Receivers except lane 0
                {0x32, 0x00} , //PD_RXINT
                {0x31, 0x00} , //RX_RATE is Full
                {0x4D, 0x08} , //EQFTC = 0 and EQLEV = 8
                {0x4C, 0x01} , //Enable Fixed EQ
                {0x34, 0x01} , //Enable Offset correction
                {0x32, 0xF0} , //Load RX settings.
                {0x32, 0x00} ,
                {0x33, 0xF0} , //Load EQ settings.
                {0xFF, 0x00} , //Select Page 0
                {0x0A, 0x3B} , //Enable HPD_SNK pass thru to HPD_SRC. Retimer
                {0xFF, 0x01} , //Select Page 1
};
```

Section 4.5:

```
Ref_Clk[] = {
                {0xFF, 0x00} ,//Page 0 select
                {0x0D, 0x80} ,//The AUX_CFG bit (Page 0 offset 0Dh bit 7) must be set to
                a 1'b1.
                {0x0A, 0x08} , //The AUX_BRG_EN bit (Page 0 offset 0Ah bit 3) must be
                        set to a 1'b1.
                {0xFF, 0x01} ,//Page 1 select
                {0x00, 0x40} , //LOCK_COMPLETE bit (Page 1 offset 00h bit 6) must be set
                to a 1'b1.
                {0x10, 0x01} , //TX Lane 0 must be enabled (Page 1 offset 10h bit 0 is
                        1'b1 and Page 1 offset 10h bit 4 is 1'b0.
                {0x10, 0x40} ,
};
```

Note: *These registers were configured manually without any assurance to justify the values.*

X Mode Register Configuration R/W Log from Debug Prints

X Mode initialization

Write Address=0xFF, Write Data=0x0
Read Address=0xFF, Read Data=0x0
Write Address=0x9, Write Data=0x36
Read Address=0x9, Read Data=0x36
Write Address=0xA, Write Data=0x7B
Read Address=0xA, Read Data=0x7B
Write Address=0xD, Write Data=0xC0
Read Address=0xD, Read Data=0xC0
Write Address=0xC, Write Data=0x6D
Read Address=0xC, Read Data=0x6D
Write Address=0x10, Write Data=0x0
Read Address=0x10, Read Data=0x0
Write Address=0x16, Write Data=0xF1
Read Address=0x16, Read Data=0xF1
Write Address=0xFF, Write Data=0x1
Read Address=0xFF, Read Data=0x1
Write Address=0x0, Write Data=0x2
Read Address=0x0, Read Data=0x2
Write Address=0x4, Write Data=0x80
Read Address=0x4, Read Data=0x80
Write Address=0x5, Write Data=0x0
Read Address=0x5, Read Data=0x0
Write Address=0x8, Write Data=0x0
Read Address=0x8, Read Data=0x0
Write Address=0xD, Write Data=0x2
Read Address=0xD, Read Data=0x2

Write Address=0xE, Write Data=0x3
Read Address=0xE, Read Data=0x1

Write Address=0x1, Write Data=0x1
Read Address=0x1, Read Data=0x1
Write Address=0x2, Write Data=0x3F
Read Address=0x2, Read Data=0x3F
Write Address=0xB, Write Data=0x33
Read Address=0xB, Read Data=0x33
Write Address=0xA1, Write Data=0x2
Read Address=0xA1, Read Data=0x2
Write Address=0xA4, Write Data=0x2
Read Address=0xA4, Read Data=0x2

Write Address=0x10, Write Data=0xF0
Read Address=0x10, Read Data=0xF0
Write Address=0x11, Write Data=0x30
Read Address=0x11, Read Data=0x30
Write Address=0x14, Write Data=0x0
Read Address=0x14, Read Data=0x0
Write Address=0x12, Write Data=0x3
Read Address=0x12, Read Data=0x3
Write Address=0x13, Write Data=0xFF
Read Address=0x13, Read Data=0xFF
Write Address=0x13, Write Data=0x0
Read Address=0x13, Read Data=0x0
Write Address=0x30, Write Data=0xE0
Read Address=0x30, Read Data=0xE0
Write Address=0x32, Write Data=0x0
Read Address=0x32, Read Data=0x0
Write Address=0x31, Write Data=0x0
Read Address=0x31, Read Data=0x0
Write Address=0x4D, Write Data=0x8
Read Address=0x4D, Read Data=0x8
Write Address=0x4C, Write Data=0x1
Read Address=0x4C, Read Data=0x1
Write Address=0x34, Write Data=0x1
Read Address=0x34, Read Data=0x1
Write Address=0x32, Write Data=0xF0
Read Address=0x32, Read Data=0xF0
Write Address=0x32, Write Data=0x0
Read Address=0x32, Read Data=0x0
Write Address=0x33, Write Data=0xF0
Read Address=0x33, Read Data=0xF0
Write Address=0xFF, Write Data=0x0
Read Address=0xFF, Read Data=0x0
Write Address=0xA, Write Data=0x3B
Read Address=0xA, Read Data=0x3B
Write Address=0xFF, Write Data=0x1
Read Address=0xFF, Read Data=0x1

Reference Clock Configuration
Write Address=0xFF, Write Data=0x0
Read Address=0xFF,Read Data=0x0
Write Address=0xD, Write Data=0x80
Read Address=0xD,Read Data=0x80
Write Address=0xA, Write Data=0x8
Read Address=0xA,Read Data=0x8
Write Address=0xFF, Write Data=0x1
Read Address=0xFF,Read Data=0x1

Write Address=0x0, Write Data=0x40
Read Address=0x0,Read Data=0x0

Write Address=0x10, Write Data=0x1
Read Address=0x10,Read Data=0x1
Write Address=0x10, Write Data=0x40
Read Address=0x10,Read Data=0x40

Clock Output