Module Pin Name	Type	Termination	Description
RGMII_MDC	O		MDC: Connect to MDC pin on GbE Transceiver.
RGMII_MDIO	I/O	1.5kΩ pull-up to VDD_1V8_HS on the module	MDIO: Connect to MDIO pin on GbE Transceiver.
ENET_RST_N	O		Ethernet Reset: Connect to Reset input on Ethernet PHY.
ENET_INT	I	10kΩ pull-up to VDD_1V8	Ethernet Interrupt: Connect to Interrupt output on Ethernet PHY.

Note: Refer to the relevant device manufacturer guidelines for correct connections from the SoC input and output clock, data, control to device.

8.1 RGMII Design Guidelines

Table 8-3 shows the signal routing requirements for RGMII interface.

Table 8-3. RGMII Interface Signal Routing Requirements

Parameter	Requirement	Units	Notes
Max Frequency	125	MHz	
Topology	Point to point		Unidirectional, source terminated, source synchronous
Reference plane	GND		
Trace Impedance	50	Ω	±15%
Max breakout distance	12 (75)	mm (ps)	
Via proximity (Signal via to GND return via)	< 3.8 (24)	mm (ps)	See note 1
Trace spacing: Microstrip / Stripline	4x / 3x	dielectric height	
Max Trace Length (Delay)	265 (1670)	mm (ps)	Assumes a propagation delay of 6.3 ps/mm.
Max Trace Delay Skew Between Clock and Data MAC/PHY supports RGMII-ID (Internal Delay) MAC/PHY does not support RGMII-ID	 8 (50) See note 2	mm (ps)	
Isolation of TX and RX CLK signals	One of the following options for **TX_CLK** and **RX_CLK** signals: **GND** shielding from each other and any other signal, or >5x spacing from each other and any other signal, or Routed on separate layers and >5x spacing from other signals.		
Isolation of TX and RX groups	One of the following options for **TX** signal and **RX** signal groups: **GND** shielding from each other, or >5x spacing from each other, or Routed on separate layers from each other		

Parameter	Requirement	Units	Notes
Noise Coupling Avoidance	Keep critical traces away from other signal traces or unrelated power traces/areas or power supply components		

Notes:

1. Up to 4 signal vias can share a single GND return via
2. NVIDIA Orin SoC does not support RGMII-ID (Internal Delay) feature, meaning that Orin RGMII TX CLK and DATA are edge aligned, while Orin RGMII RX CLK and DATA must be center aligned. Therefore, a CLK-to-DATA skew of greater than 1.5ns and less than 2.0ns must be ensured on Orin RGMII RX signals, either via MAC/PHY RGMII-ID (if supported) or via PCB trace delay. The requirements and recommendations of MAC/PHY RGMII Receiver shall be followed for the CLK-to-DATA skew of Orin RGMII TX signals.

Table 8-4. Recommended Ethernet Test Points for Initial Boards

Test Points Recommended	Location
One for each of the RGMII lines.	TX near the device and RX near the Orin module connector