DP83869HM ETHERNET PHY

Route TD_P/N pairs with
100-ohms differential trace immpedance

PHY POWER SUPPLY JUMPERS

PHY_VCC_3V3 — FB3 — VDDIO — 100 Ohms, 3A
VCC_1V8_Analog — FB2 — VDDA1P8_AB — 100 Ohms, 3A
AVDD_1V1 — FB4 — VDDA1P1 — 100 Ohms, 3A
VCC_2V5 — FB5 — VDDA2P5 — 100 Ohms, 3A
VCC_1V8_Analog — FB1 — VDDA1P8_CD — 100 Ohms, 3A

LED_2 Optional

VDDIO — D11 LED Green — DNP — R207 470E — LED_2

JTAG INTERFACE

J15 2x7 (87832-1420)
JTAG_TMS, JTAG_CLK, JTAG_TDO, JTAG_TDI
R173 4.7K, R174 4.7K, R175 4.7K DNP, R176 4.7K
R255 4.7K DNP

Straps for PHY Address

RX_D0: J16 (1X3) RX_D0_Mode1 / RX_D0 / RX_D0_Mode2; J18 (1x2) RX_D0 / RX_D0_Mode3
RX_D1: J17 (1X3) RX_D1_Mode1 / RX_D1 / RX_D1_Mode2; J19 (1x2) RX_D1 / RX_D1_Mode3

RX_D0 Address: R191 10K, R209 5.76K, R201 2.49K
RX_D1 Address: R189 10K, R212 5.76K, R213 2.49K
R183 2.49K, R208 2.49K, R205 0E DNP
R184 2.49K, R211 2.49K, R210 0E DNP

Table 11. PHY Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		PHY_ADD1	PHY_ADD0
RX_D0	PHY_ADD[1:0]	33	00	MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1
					PHY_ADD3	PHY_ADD2
RX_D1	PHY_ADD[3:2]	34	00	MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1

Table 12. Strap Table for 100 Mbps Media Converter Mode

PIN NAME	STRAP NAME	PIN #	PIN STRAP CONNECTION
JTAG_TDO / GPIO_1	OPMODE_0	22	2.49KΩ Pull-up to VDDIO
RX_D3	OPMODE_1	36	OPEN
RX_D2	OPMODE_2	35	2.49KΩ Pull-up to VDDIO

Table 13. Strap Table for Copper and 100Base-FX Interface

PIN NAME	STRAP NAME	PIN #	FUNCTION		
			ANEGSEL_0	ANEGSEL_1	
LED_1	ANEGSEL_0	46			
LED_2	ANEGSEL_1	45	1	1	Copper: Auto Negotiation (100 Advertised), Auto MDIX
			MIRROR_EN		
RX_CTRL	MIRROR_EN	38	0		Copper Mirror Disable
			1		Copper Mirror Enable
			LINK_LOSS		
RX_CLK	LINK_LOSS	32	0		Link Loss Pass Thru Enabled
			1		Link Loss Pass Thru Disabled

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