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Final

P17_0306_020_IOPT-FD_TCAN1043_report00
Date of Approval: 2017-Nov-17

Test Report

Device Under Test		**Customer**	
Object Family	TCAN1043	Order No.	P17_0306
Manufacturer	Texas Instruments	Name	Texas Instruments
Type	TCAN1043 (H)(G) -Q1	Address	12500 TI Blvd MS 8700 Dallas, TX 75243 USA
Sample marking	7AA3EVM P1043		

Number of Pages	19
Test Period	from ww45/2017 until ww46/2017
Test Method / Test Requirement	CAN IOPT Test for devices - with CAN FD up to 5 Mbit/s - with low power
Performed Tests and References	1 Interoperability test specification for high-speed CAN transceiver or equivalent devices IOPT.CAN v01 2 Static Tests based on: ISO/DIS 16845-2:2017, Road vehicles — Controller area network (CAN) — Part 2: High-speed medium access unit - Conformance test plan
Conformance Test Results	The Test Results refer to the delivered device.
1 Homogeneous Network with 16 Nodes / 8 Nodes	**Pass**
Heterogeneous Network with 16 Nodes – Mix of 6 8 Nodes – Mix of 5	**Pass**
2 Test type 1, static test cases	**Pass**

For detailed information see chapter Test List at the following pages.

Approved by

D. Bollati, President

Test performed by

L. Kukla, Project Manager

Table of Content

Revision History

Old revision	New revision	Amendment Description	Editor
–	00	Final version	LK

1 Device Under Test (detailed)

General	
Date of Sample Arrival	27.10.2017
Manufacturer	Texas Instruments
Sample Marking	7AA3EVM P1043
Test performed with DUT no.	#01 to #16 // #01 to #08 (homogenous) #01 to #04 // #01 to #02 (mixed)

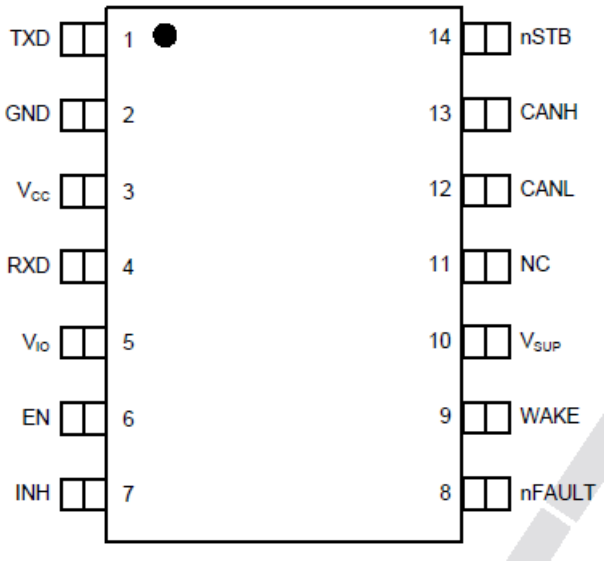
Device Specification	
Object Family	TCAN1043
Version	TCAN1043 (H)(G) -Q1
Design step	-

Documentation	
User manual / datasheet	SLLSEV0.pdf *(SLLSEV0 –OCTOBER 2017)*

Device Classification	
CAN FD Transceiver	Data bit rates up to 5 Mbit/s

2 Setup for Device Under Test

Standard CAN HS Transceiver with 14 pins and V_{IO}, V_{IO} connected to V_{cc}



3 Test Equipment

The following test equipment and test system have been used.

No.	Component	Manufacturer	Version / Type	Network
1	IOPT.CAN Tester T1	C&S	v2.0.0.159	Homogeneous
2	IOPT.CAN Tester T2	C&S	v2.0.0.159	Homogeneous Mixed
3	UT software version	C&S	HS 14-pin standard	-

4 Technical Correspondence

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5 Test List

5.1 Static Conformance Tests (ISO/DIS 16845-2, 2017(E))

Used data sheet:
SLLSEV0.pdf *(SLLSEV0 –OCTOBER 2017)*

“The motivation of static test cases is to check the availability and the boundaries in the data sheet of the IUT. For all integrated circuits every related parameter in Table 4 shall be part of the data sheet and fulfil the specified boundaries in terms of physical worst case condition. Data sheet parameter names may deviate from the names in Table 4, but in this case a cross–reference list (data sheet versus Table 4) shall be provided for this test. Parameter conditions may deviate from the conditions in Table 4, if the data sheet conditions are according to the physical worst case context in Table 4 at least.”

HS-PMA types:
a - without low-power mode and partial network,
b - with low-power mode, normal biasing and without partial network,
c - with low-power mode, automatic biasing and without partial network, **n/a**
d - with low-power mode, automatic biasing and partial network; **n/a**

No.	Parameter	Reference to ISO 11898-2 table no. / clause	Limits			Conditions	Conformance test is passed if value		
			Min	Max	Unit		≤	≥	Rating
1	General maximum rating V_{CAN_H} and V_{CAN_L}	Table 15	-27,0	+40,0	V	-/-	min	max	Pass Sec. 7.1 VBUS
2	Extended maximum rating V_{CAN_H} and V_{CAN_L} (if supported)	Table 15	-58,0	+58,0	V	-/-	min	max	Pass Sec. 7.1 VBUS
3	Maximum rating V_{Diff}	Table 15	-5,0	+10,0	V	-/-	min	max	Pass Sec. 7.1 V(Diff)
4	Single ended recessive output voltage on CAN_H (V_{CAN_H}), bus biasing active	Table 5	+2,0	+3,0	V	-/-	max	min	Pass Sec. 7.7 VO(R)
5	Single ended recessive output voltage on CAN_L (V_{CAN_L}), bus biasing active	Table 5	+2,0	+3,0	V	-/-	max	min	Pass Sec. 7.7 VO(R)
6	Differential recessive output voltage (V_{Diff}), bus biasing active	Table 5	-0,5	+0,05	V	-/-	max	min	Pass Sec. 7.7 VOD(R)
7	Single ended recessive output voltage on CAN_H (V_{CAN_H}), bus biasing inactive	Table 6	-0,1	+0,1	V	-/-	max	min	Pass Sec. 7.7 VO(STB)
8	Single ended recessive output voltage on CAN_L (V_{CAN_L}), bus biasing inactive	Table 6	-0,1	+0,1	V	-/-	max	min	Pass Sec. 7.7 VO(STB)
9	Differential recessive output voltage (V_{Diff}), bus biasing inactive	Table 6	-0,2	+0,2	V	-/-	max	min	Pass Sec. 7.7 VO(STB)

10	Single ended voltage on CAN_H, dominant output (V_{CAN_H})	Table 2	+2,75	+4,50	V	R_L = 50 Ω … 65 Ω	max	min	Pass Sec. 7.7 $V_{O(D)}$
11	Single ended voltage on CAN_L, dominant output (V_{CAN_L})	Table 2	+0,5	+2,25	V	R_L = 50 Ω … 65 Ω	max	min	Pass Sec. 7.7 $V_{O(D)}$
12	Differential voltage on normal bus load, dominant output (V_{Dfiff})	Table 2	+1,5	+3,0	V	R_L = 50 Ω … 65 Ω	max	min	Pass Sec. 7.7 $V_{OD(D)}$
13	Differential voltage on effective resistance during arbitration, dominant output (V_{Diff})	Table 2	+1,5	+5,0	V	R_L = 2240 Ω	max	min	Pass Sec. 7.7 $V_{O(D)}$
14	Differential voltage on extended bus load, dominant output (V_{Diff}) (if supported)	Table 2	+1,4	+3,3	V	R_L = 45 Ω … 70 Ω	max	min	Pass Sec. 7.7 $V_{O(D)}$
15	Driver symmetry (V_{SYM}), with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, however, at most 1 MHz (2 MBit/s)	Table 3	+0,9	+1,1	-/-	R_L = 60 Ω; C_1 = 4,7 nF	max	min	Pass Sec. 7.7 V_{SYM}
16	Absolute current on CAN_H (I_{CAN_H}), Maximum driver output current	Table 4	-/-	+115	mA	-3,0 V ≤ V_{CAN_H} ≤ +18,0 V	max	-/-	Pass Sec. 7.7 $I_{OS(DOM)}$
17	Absolute current on CAN_L (I_{CAN_L}), Maximum driver output current	Table 4	-/-	+115	mA	-3,0 V ≤ V_{CAN_L} ≤ +18,0 V	max	-/-	Pass Sec. 7.7 $I_{OS(DOM)}$
18	Transmit dominant time out (t_{dom}), (if supported) *b) The minimum value of 0,3 ms is accepted for legacy implementations.*	Table 7	+0,8[b]	+10,0	ms	-/-	max	min	Pass Sec. 7.8 t_{TxD_DTO}

19	Receiver recessive state differential input voltage range, bus biasing active (V_{Diff})	Table 8	-3,0	+0,5	V	-12,0 V ≤ V_{CAN_L} ≤ +12,0 V -12,0 V ≤ V_{CAN_H} ≤ +12,0 V	min	max	Pass Sec. 7.7 VREC
20	Receiver dominant state differential input voltage range, bus biasing active (V_{Diff})	Table 8	+0,9	+8,0	V	-12,0 V ≤ V_{CAN_L} ≤ +12,0 V -12,0 V ≤ V_{CAN_H} ≤ +12,0 V	min	max	Pass Sec. 7.7 VDOM
21	Receiver recessive state differential input voltage range, bus biasing inactive (V_{Diff}), (if supported)	Table 9	-3,0	+0,4	V	-12,0 V ≤ V_{CAN_L} ≤ +12,0 V -12,0 V ≤ V_{CAN_H} ≤ +12,0 V	min	max	Pass Sec. 7.7 VREC(Sleep)
22	Receiver dominant state differential input voltage range, bus biasing inactive (V_{Diff}), (if supported)	Table 9	+1,15	+8,0	V	-12,0 V ≤ V_{CAN_L} ≤ +12,0 V -12,0 V ≤ V_{CAN_H} ≤ +12,0 V	min	max	Pass Sec. 7.7 VDOM(Sleep)
23	Differential internal resistance, receiver input resistance (R_{Diff})	Table 10	12	100	kΩ	-2,0 V ≤ V_{CAN_H} ≤ +7,0 V -2,0 V ≤ V_{CAN_L} ≤ +7,0 V	max	min	Pass Sec. 7.7 RID
24	Single ended internal resistance, receiver input resistance (R_{CAN_H}, R_{CAN_L})	Table 10	6	50	kΩ	-2,0 V ≤ V_{CAN_H} ≤ +7,0 V -2,0 V ≤ V_{CAN_L} ≤ +7,0 V	max	min	Pass Sec. 7.7 RIN
25	Matching of receiver internal resistance (m_R)	Table 11	-0,03	+0,03	-/-	V_{CAN_H} = +5,0 V V_{CAN_L} = +5,0 V	max	min	Pass Sec. 7.7 RIN(M)
26	Loop delay (t_{Loop})	Table 12	-/-	255	ns	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	max	-/-	Pass Sec. 7.8 tPROP(LOOP1) tPROP(LOOP2)
27	Transmitted recessive bit width @ 2 Mbit/s ($t_{Bit(Bus)}$), (if supported)	Table 13	435	530	ns	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	max	min	Pass Sec. 7.8 tBIT(BUS)
28	Received recessive bit width @ 2 Mbit/s ($t_{Bit(RXD)}$), (if supported)	Table 13	400	550	ns	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	max	min	Pass Sec. 7.8 tBIT(RXD)
29	Receiver timing symmetry @ 2 Mbit/s (Δt_{Rec}), (if supported)	Table 13	-65	+40	ns	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	max	min	Pass Sec. 7.8 ΔtREC
30	Transmitted recessive bit width @ 5 Mbit/s ($t_{Bit(Bus)}$), (if supported)	Table 14	155	210	ns	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	max	min	Pass Sec. 7.8 tBIT(BUS)

31	Received recessive bit width @ 5 Mbit/s ($t_{Bit(RXD)}$), (if supported)	Table 14	120	220	ns	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	max	min	Pass Sec. 7.8 $t_{BIT(RXD)}$
32	Receiver timing symmetry @ 5 Mbit/s (Δt_{Rec}), (if supported)	Table 14	-45	+15	ns	R_L = 60 Ω, C_2 = 100 pF, C_{RXD} = 15 pF	max	min	Pass Sec. 7.8 Δt_{REC}
33	Leakage current on CAN_H, CAN_L (I_{CAN_H}, I_{CAN_L}), maximum leakage currents, unpowered	Table 16	-10	+10	µA	V_{CAN_H} = 5 V, V_{CAN_L} = 5 V,	max	min	Pass Sec. 7.7 $I_{IOFF(LKG)}$
34	CAN activity filter time, long (t_{Filter}), (if supported)	Table 20	0,5	5,0	µs	-/-	max	min	Pass Sec. 7.8 t_{WK_FILTER}
35	CAN activity filter time, short (t_{Filter}), (if supported)	Table 20	0,15	1,8	µs	-/-	max	min	Not supported
36	Wake-up timeout (t_{Wake}), (if supported) *c) For legacy implementations a minimum value of 350 µs is acceptable.*	Table 20	800,0[c]	10000,0	µs	-/-	max	min	Pass Sec. 7.8 $t_{WK\_TIMEOUT}$
37	Timeout for bus inactivity (t_{Silece})	Table 20	$0,6*10^6$	$1,2*10^6$	µs	-/-	max	min	n/a
38	Bus Bias reaction time (t_{Bais})	Table 20	-/-	250,0	µs	-/-	max	-/-	n/a
39	Number of recessive bits before a new SOF shall be accepted (n_{Bits_idle}) (if supported)	Table 18	6	10	-/-	-/-	max	min	n/a
40	CAN FD data phase glitch filter (slow) ($pGlitch_{Slow}$) (if supported)	Table 19	5,00	17,50	% of arbitration bit time	-/-	min	max	n/a
41	CAN FD data phase glitch filter (fast) ($pGlitch_{Fast}$) (if supported)	Table 19	2,50	8,75	% of arbitration bit time	-/-	min	max	n/a

5.2 *Dynamic Tests (CAN IOPT v01)*

Following test case numeration relates on the corresponding test specification.

5.4 –Tests in Homogeneous Network with 16 Nodes – 2 Mbit/s with wake-up via bus for “5 Mbit/s Devices”

No.	Tests in Homogeneous Network with 16 Nodes - 2 Mbit/s with wake-up via bus	Result	Comment
5.4.1	**Test Flow 1** Op. mode variation after recovery at normal mode, failure application on startup		*Performed in 8-node-network with 5 MBit/s*
5.4.1.1.x	GND Shift = 0V	n/a	
5.4.1.2.x	GND Shift = +1V	n/a	
5.4.1.3.x	GND Shift = -1V	n/a	
5.4.2	**Test Flow 2** Op. mode variation after recovery at normal mode, failure application in normal mode		4224 Test cases
5.4.2.1.x	GND Shift = 0V	E/Pass	
5.4.2.2.x	GND Shift = +1V	E/Pass	
5.4.2.3.x	GND Shift = -1V	E/Pass	
5.4.3	**Test Flow 3** Op. mode variation before recovery at normal Mode, failure application in normal mode		4224 test cases
5.4.3.1.x	GND Shift = 0V	E/Pass	
5.4.3.2.x	GND Shift = +1V	E/Pass	
5.4.3.3.x	GND Shift = -1V	E/Pass	
5.4.4	**Test Flow 4** Op. mode variation with failure before recovery at normal mode, failure application on startup		264 Test cases
5.4.4.1.x	GND Shift = 0V	E/Pass	
5.4.4.2.x	GND Shift = +1V	E/Pass	
5.4.4.3.x	GND Shift = -1V	E/Pass	

No.	Tests in Homogeneous Network with 16 Nodes - 2 Mbit/s with wake-up via bus	Result	Comment
5.4.5	**Test Flow 5** Op. mode variation with failure before recovery at low-power mode, failure application in normal mode		4224 Test cases
5.4.5.1.x	GND Shift = 0V	E/Pass	
5.4.5.2.x	GND Shift = +1V	E/Pass	
5.4.5.3.x	GND Shift = -1V	E/Pass	
5.4.6	**Test Flow 6** Op. mode variation with failure before recovery at low-power mode, failure application in low-power mode		4224 Test cases
5.4.6.1.x	GND Shift = 0V	E/Pass	
5.4.6.2.x	GND Shift = +1V	E/Pass	
5.4.6.3.x	GND Shift = -1V	E/Pass	
5.4.7	**Test Flow 7** Op. mode variation with failure before recovery at normal mode, failure application in low-power mode		264 Test cases
5.4.7.1.x	GND Shift = 0V	E/Pass	
5.4.7.2.x	GND Shift = +1V	E/Pass	
5.4.7.3.x	GND Shift = -1V	E/Pass	

Signs and symbols

E executed

5.4 –Tests in Homogeneous Network with 8 Nodes – 5 Mbit/s with wake-up via bus

No.	Tests in Homogeneous Network with 8 Nodes - 5 Mbit/s with wake-up via bus	Result	Comment
5.4.1	**Test Flow 1** Op. mode variation after recovery at normal mode, failure application on startup		1088 Test cases
5.4.1.1.x	GND Shift = 0V	E/Pass	
5.4.1.2.x	GND Shift = +1V	E/Pass	
5.4.1.3.x	GND Shift = -1V	E/Pass	

Signs and symbols

E executed

6.4 –Tests in Heterogeneous Network with 16 Nodes – 2 Mbit/s with wake-up via bus for “5 Mbit/s Devices”

No.	Tests in Heterogeneous Network with 16 Nodes – 2 Mbit/s with wake-up via bus – Mix of 6*: 2xA / 3xB / 2xC / 2xD / 3xE / 4xIUT	Result	Comment
6.4.1	**Test Flow 1** Op. mode variation after recovery at normal mode, failure application on startup		*Performed in 8-node-network with 5 MBit/s*
6.4.1.1.x	GND Shift = 0V	n/a	
6.4.1.2.x	GND Shift = +1V	n/a	
6.4.1.3.x	GND Shift = -1V	n/a	
6.4.2	**Test Flow 2** Op. mode variation after recovery at normal mode, failure application in normal mode		4224 Test cases
6.4.2.1.x	GND Shift = 0V	E/Pass	
6.4.2.2.x	GND Shift = +1V	E/Pass	
6.4.2.3.x	GND Shift = -1V	E/Pass	
6.4.3	**Test Flow 3** Op. mode variation before recovery at normal Mode, failure application in normal mode		4224 Test cases
6.4.3.1.x	GND Shift = 0V	E/Pass	
6.4.3.2.x	GND Shift = +1V	E/Pass	
6.4.3.3.x	GND Shift = -1V	E/Pass	
6.4.4	**Test Flow 4** Op. mode variation with failure before recovery at normal mode, failure application on startup		264 Test cases
6.4.4.1.x	GND Shift = 0V	E/Pass	
6.4.4.2.x	GND Shift = +1V	E/Pass	
6.4.4.3.x	GND Shift = -1V	E/Pass	

No.	Tests in Heterogeneous Network with 16 Nodes – 2 Mbit/s with wake-up via bus – Mix of 6*: 2xA / 3xB / 2xC / 2xD / 3xE / 4xIUT	Result	Comment
6.4.5	**Test Flow 5** Op. mode variation with failure before recovery at low-power mode, failure application in normal mode		4224 Test cases
6.4.5.1.x	GND Shift = 0V	E/Pass	
6.4.5.2.x	GND Shift = +1V	E/Pass	
6.4.5.3.x	GND Shift = -1V	E/Pass	
6.4.6	**Test Flow 6** Op. mode variation with failure before recovery at low-power mode, failure application in low-power mode		4224 Test cases
6.4.6.1.x	GND Shift = 0V	E/Pass	
6.4.6.2.x	GND Shift = +1V	E/Pass	
6.4.6.3.x	GND Shift = -1V	E/Pass	
6.4.7	**Test Flow 7** Op. mode variation with failure before recovery at normal mode, failure application in low-power mode		264 Test cases
6.4.7.1.x	GND Shift = 0V	E/Pass	
6.4.7.2.x	GND Shift = +1V	E/Pass	
6.4.7.3.x	GND Shift = -1V	E/Pass	

Signs and symbols

E executed

Abbreviations to identify components:

- 2 x A TJA1044GT
- 3 x B TJA1043T
- 2 x C TLE9252
- 2 x D TLE9255WSK
- 3 x E TLE9251
- 4 x IUT Implementation Under Test

Positions of the reference devices in 500 kbit/s and 2 Mbit/s reference environments:

Node:	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15	#16
TRX:	B	A	IUT	C	E	D	IUT	B	E	A	IUT	B	C	D	IUT	E

6.4 –Tests in Heterogeneous Network with 8 Nodes – 5 Mbit/s with wake-up via bus

No.	Tests in Heterogeneous Network with 8 Nodes – 5 Mbit/s with wake-up via bus – Mix of 5*: 1xA / 2xB / 1xC / 2xD / 2xIUT	Result	Comment
6.4.1	**Test Flow 1** Op. mode variation after recovery at normal mode, failure application on startup		1088 Test cases
6.4.1.1.x	GND Shift = 0V	E/Pass	
6.4.1.2.x	GND Shift = +1V	E/Pass	
6.4.1.3.x	GND Shift = -1V	E/Pass	

Signs and symbols

E executed

Abbreviations to identify components:

- 1 x A TJA1044GT
- 2 x B TJA1043T
- 1 x C TLE9252
- 2 x D TLE9251
- 2 x IUT Implementation Under Test

Positions of the reference devices in 5 Mbit/s reference environments:

Node:	#1	#2	#3	#4	#5	#6	#7	#8
TRX:	A	B	IUT	C	B	D	IUT	D