Pin FMA	**Device Names:**	PCA9546A and TCA9546A	**Applicable to the following packages: D, DGV, DW, and PW**		
	Spec Version:	SCPS148G and SCPS205B			
	Created on/by:	09/03/2020, Duy 'Bobby' Nguyen			

Pin	Function	Abs Max Rating	Defect Mode	Defect Reason	Consequences on the device	Consequences on the system
1	A0	-0.5V … 7V	Short to V_{CC}	SC to supply	Address may change if previously pulled down to GND through resistor. Damage to device is not expected.	Potential short to GND if A0 were referenced to GND w/o a resistor. If referenced to GND with a resistor, master would not be able to communicate to device due to the address change. Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
			Short to GND	SC to gnd	Address may change if previously pulled up to Vcc through resistor. Damage to device is not expected.	Potential short to Vcc if A0 were referenced to Vcc without a resistor. If referenced to Vcc with a resistor, master would not be able to communicate to device due to the address change. Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
			floating pin	bond open	Address is in an unknown state. Additional leakage/Standby current may occur.	Master may not be able to communicate to device (may work intermittently). Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
			SC to Pin(2)	Pin Short	Assuming address pins are referenced with a resistor; If references differ and reference resistors are equal, the address pins for both devices may be in an unknown state and be susceptible to noise. If references to both are the same, device will see no consequences aside from potential additional leakage currents	If references differ and reference resistors are equal, master may not be able to communicate to device (may work intermittently). Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
2	A1	-0.5V … 7V	Short to V_{CC}	SC to supply	Address may change if previously pulled down to GND through resistor. Damage to device is not expected.	Potential short to GND if A1 were referenced to GND w/o a resistor. If referenced to GND with a resistor, master would not be able to communicate to device due to the address change. Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
			Short to GND	SC to gnd	Address may change if previously pulled up to Vcc through resistor. Damage to device is not expected.	Potential short to Vcc if A1 were referenced to Vcc w/o a resistor. If referenced to Vcc with a resistor, master would not be able to communicate to device due to the address change. Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
			floating pin	bond open	Address is in an unknown state. Additional leakage/Standby current may occur.	Master may not be able to communicate to device (may work intermittently). Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
			SC to Pin(3)	Pin Short	Assuming address pin is referenced with a resistor; If references differ and reference resistors are equal, the address pin for the device may be in an unknown state and be susceptible to noise. If references to both are the same (referenced HIGH since this is a reset pin short), the device will see no consquences aside from potential additional leakage currents	If references differ and reference resistors are equal, master may not be able to communicate to device (may work intermittently). Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
3	#RESET	-0.5V … 7V	Short to V_{CC}	SC to supply	None (RESET errata is present in the PCA)	None
			Short to GND	SC to gnd	Device will be held in RESET assuming the pin is biased to Vcc through a resistor	Master will not be able to get an ACK from slave.
			floating pin	bond open	Device is in an unknown state. Additional leakage/Standby current may occur.	Device may work intermittenly and may reset its channels due to noise coupling onto the pad.
			SC to Pin(4)	Pin Short	Device will reset itself at all start conditions and will never ACK.	Master will not be able to get an ACK from slave.
			Short to V_{CC}	SC to supply	If CH0 is enabled, may push the pass FET between SD0 and SDA into saturation. IoL through device could exceed absolute maximum Output current of 25mA spec'd in datasheet. Device reliabilty/FIT rate may be affected if absolute maximum current is violated	Large IoL current could damage masters/slaves on the I2C bus. Large VoL seen by downstream slaves could cause signal integrity issues where lows a no longer perceived as a logic '0.'

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4	SD0	-0.5V … 7V	Short to GND	SC to gnd	If CH0 is enabled, I2C bus will get stuck. No expected harm to device but functionality is affected.	If CH0 is enabled, I2C bus will get stuck. This means I2C communication is no longer possible. Only way to resolve is to reset the device or power cycle.
			floating pin	bond open	No damage or reliabilty concerns expected. But device functionality will be affected.	Downstream slaves/masters will not see the data line go low, I2C communication downstream will be ineffective.
			SC to Pin(5)	Pin Short	No damage or reliabilty concerns expected. But device functionality may be affected.	Signal integrity will be greatly affected. I2C communication will basically be ineffective (similar to a stuck bus). Power cycle or RESET is required to resolve.
5	SC0	-0.5V … 7V	Short to V$_{CC}$	SC to supply	If CH0 is enabled, may push the pass FET between SC0 and SCL into saturation. IoL through device could exceed absolute maximum Output current of 25mA spec'd in datasheet. Device reliabilty/FIT rate may be affected if absolute maximum current is violated	Large IoL current could damage masters/slaves (who support clock stretching) on the I2C bus. Large VoL seen by downstream slaves could cause signal integrity issues where lows a no longer perceived as a logic '0.'
			Short to GND	SC to gnd	If CH0 is enabled, I2C bus will get stuck. No expected harm to device but functionality is affected.	If CH0 is enabled, I2C bus will get stuck. This means I2C communication is no longer possible. Only way to resolve is to reset the device or power cycle.
			floating pin	bond open	No damage or reliabilty concerns expected. But device functionality will be affected.	Downstream slaves/masters will not see the clock signal go low, I2C communication downstream will be ineffective.
			SC to Pin(6)	Pin Short	No damage or reliabilty concerns expected. But device functionality may be affected.	If both CH0 and CH1 are enabled: Signal integrity could be greatly be affected . I2C communication will basically be ineffective (similar to a stuck bus). Powercycle or RESET is required to resolve. If only one of the channels are enabled: bus loading could exceed I2C spec limit. In worst case scenario, cross talk could result in a glitch/I2C stuck bus on SC1 when it is enabled.
6	SD1	-0.5V … 7V	Short to V$_{CC}$	SC to supply	If CH1 is enabled, may push the pass FET between SD1 and SDA into saturation. IoL through device could exceed absolute maximum Output current of 25mA spec'd in datasheet. Device reliabilty/FIT rate may be affected if absolute maximum current is violated	Large IoL current could damage masters/slaves on the I2C bus. Large VoL seen by downstream slaves could cause signal integrity issues where lows a no longer perceived as a logic '0.'
			Short to GND	SC to gnd	If CH1 is enabled, I2C bus will get stuck. No expected harm to device but functionality is affected.	If CH1 is enabled, I2C bus will get stuck. This means I2C communication is no longer possible. Only way to resolve is to reset the device or power cycle.
			floating pin	bond open	No damage or reliabilty concerns expected. But device functionality will be affected.	Downstream slaves/masters will not see the data line go low, I2C communication downstream will be ineffective.
			SC to Pin(7)	Pin Short	No damage or reliabilty concerns expected. But device functionality may be affected.	Signal integrity will be greatly affected. I2C communication will basically be ineffective (similar to a stuck bus). Power cycle or RESET is required to resolve.
7	SC1	-0.5V … 7V	Short to V$_{CC}$	SC to supply	If CH1 is enabled, may push the pass FET between SC1 and SCL into saturation. IoL through device could exceed absolute maximum Output current of 25mA spec'd in datasheet. Device reliabilty/FIT rate may be affected if absolute maximum current is violated	Large IoL current could damage masters/slaves (who support clock stretching) on the I2C bus. Large VoL seen by downstream slaves could cause signal integrity issues where lows a no longer perceived as a logic '0.'
			Short to GND	SC to gnd	If CH1 is enabled, I2C bus will get stuck. No expected harm to device but functionality is affected.	If CH1 is enabled, I2C bus will get stuck. This means I2C communication is no longer possible. Only way to resolve is to reset the device or power cycle.
			floating pin	bond open	No damage or reliabilty concerns expected. But device functionality will be affected.	Downstream slaves/masters will not see the clock signal go low, I2C communication downstream will be ineffective.
			SC to Pin(8)	Pin Short	If CH1 is enabled, I2C bus will get stuck. No expected harm to device but functionality is affected.	If CH1 is enabled, I2C bus will get stuck. This means I2C communication is no longer possible. Only way to resolve is to reset the device or power cycle.
8	GND		Short to V$_{CC}$	SC to supply	Damage may occur on a system level but may not occur to device.	Large current from Vcc to GND due to short. May damage power supply or cause large GND shift.
			Short to GND	SC to gnd	None	None
			floating pin	bond open	Device is in an unknown state. Back biasing could occur.	Device likely won't respond to I2C communication.
9	SD2	-0.5V … 7V	Short to V$_{CC}$	SC to supply	If CH2 is enabled, may push the pass FET between SD2 and SDA into saturation. IoL through device could exceed absolute maximum Output current of 25mA spec'd in datasheet. Device reliabilty/FIT rate may be affected if absolute maximum current is violated	Large IoL current could damage masters/slaves on the I2C bus. Large VoL seen by downstream slaves could cause signal integrity issues where lows a no longer perceived as a logic '0.'
			Short to GND	SC to gnd	If CH2 is enabled, I2C bus will get stuck. No expected harm to device but functionality is affected.	If CH2 is enabled, I2C bus will get stuck. This means I2C communication is no longer possible. Only way to resolve is to reset the device or power cycle.
			floating pin	bond open	No damage or reliabilty concerns expected. But device functionality will be affected.	Downstream slaves/masters will not see the data line go low, I2C communication downstream will be ineffective.
			SC to Pin(10)	Pin Short	No damage or reliabilty concerns expected. But device functionality may be affected.	Signal integrity will be greatly affected. I2C communication will basically be ineffective (similar to a stuck bus). Power cycle or RESET is required to resolve.
			Short to V$_{CC}$	SC to supply	If CH2 is enabled, may push the pass FET between SC2 and SCL into saturation. IoL through device could exceed absolute maximum Output current of 25mA spec'd in datasheet. Device reliabilty/FIT rate may be affected if absolute maximum current is violated	Large IoL current could damage masters/slaves (who support clock stretching) on the I2C bus. Large VoL seen by downstream slaves could cause signal integrity issues where lows a no longer perceived as a logic '0.'

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10	SC2	-0.5V … 7V	Short to GND	SC to gnd	If CH2 is enabled, I2C bus will get stuck. No expected harm to device but functionality is affected.	If CH2 is enabled, I2C bus will get stuck. This means I2C communication is no longer possible. Only way to resolve is to reset the device or power cycle.
			floating pin	bond open	No damage or reliabilty concerns expected. But device functionality will be affected.	Downstream slaves/masters will not see the clock signal go low, I2C communication downstream will be ineffective.
			SC to Pin(11)	Pin Short	No damage or reliabilty concerns expected. But device functionality may be affected.	If both CH2 and CH3 are enabled: Signal integrity could be greatly affected . I2C communication will basically be ineffective (similar to a stuck bus). Powercycle or RESET is required to resolve. If only one of the channels are enabled: bus loading could exceed I2C spec limit. In worst case scenario, cross talk could result in a glitch/I2C stuck bus on SC3 when it is enabled.
11	SD3	-0.5V … 7V	Short to V$_{CC}$	SC to supply	If CH3 is enabled, may push the pass FET between SD3 and SDA into saturation. IoL through device could exceed absolute maximum Output current of 25mA spec'd in datasheet. Device reliabilty/FIT rate may be affected if absolute maximum current is violated	Large IoL current could damage masters/slaves on the I2C bus. Large VoL seen by downstream slaves could cause signal integrity issues where lows a no longer perceived as a logic '0.'
			Short to GND	SC to gnd	If CH3 is enabled, I2C bus will get stuck. No expected harm to device but functionality is affected.	If CH3 is enabled, I2C bus will get stuck. This means I2C communication is no longer possible. Only way to resolve is to reset the device or power cycle.
			floating pin	bond open	No damage or reliabilty concerns expected. But device functionality will be affected.	Downstream slaves/masters will not see the data line go low, I2C communication downstream will be ineffective.
			SC to Pin(12)	Pin Short	No damage or reliabilty concerns expected. But device functionality may be affected.	Signal integrity will greatly be affected. I2C communication will basically be ineffective (similar to a stuck bus). Power cycle or RESET is required to resolve.
12	SC3	-0.5V … 7V	Short to V$_{CC}$	SC to supply	If CH3 is enabled, may push the pass FET between SC3 and SCL into saturation. IoL through device could exceed absolute maximum Output current of 25mA spec'd in datasheet. Device reliabilty/FIT rate may be affected if absolute maximum current is violated	Large IoL current could damage masters/slaves (who support clock stretching) on the I2C bus. Large VoL seen by downstream slaves could cause signal integrity issues where lows a no longer perceived as a logic '0.'
			Short to GND	SC to gnd	If CH3 is enabled, I2C bus will get stuck. No expected harm to device but functionality is affected.	If CH3 is enabled, I2C bus will get stuck. This means I2C communication is no longer possible. Only way to resolve is to reset the device or power cycle.
			floating pin	bond open	No damage or reliabilty concerns expected. But device functionality will be affected.	Downstream slaves/masters will not see the clock signal go low, I2C communication downstream will be ineffective.
			SC to Pin(13)	Pin Short	If CH3 is not enabled and A2 is referenced to GND with a resistor, a resistor divider will be formed between the two reference resistors. The address of the device may change due to noise and may not respond to its address. If CH3 is not enabled and A2 is referenced HIGH, device is expected to work until CH3 is enabled. If CH3 becomes enabled, device may work intermittently or not at all and may remain enabled to CH3 at all times without being able to disable or enable other channels without a power cycle or toggling reset. Device damage	Changing the device's channels may not be possible and device may remain stuck to CH3 in the worst case.
13	A2	-0.5V … 7V	Short to V$_{CC}$	SC to supply	Address may change if previously pulled down to GND through resistor. Damage to device is not expected.	Potential short to GND if A2 were referenced to GND without a resistor. If referenced to GND with a resistor, master would not be able to communicate to device due to the address change. Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
			Short to GND	SC to gnd	Address may change if previously pulled up to Vcc through resistor. Damage to device is not expected.	Potential short to Vcc if A2 were referenced to Vcc without a resistor. If referenced to Vcc with a resistor, master would not be able to communicate to device due to the address change. Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
			floating pin	bond open	Address is in an unknown state. Additional leakage/Standby current may occur.	Master may not be able to communicate to device (may work intermittently). Worst case scenario is an address conflict which could result in signal integrity loss or wrong data being written into device (unintentional channel enable)
			SC to Pin(14)	Pin Short	The device may not ACK to its address call. Functionality may be intermittent.	Communicating/programming the device may not work or work intermittently.
14	SCL	-0.5V … 7V	Short to V$_{CC}$	SC to supply	None	Damage likely to master; even if master can handle the large IoL, the master's driver will likely saturate and VoLs will be come large, potentially higher than ViL on slave devices on I2C bus. I2C communication may not work.
			Short to GND	SC to gnd	None	I2C bus will be inaccessable through I2C transactions.
			floating pin	bond open	Device will always NACK its own address	Master will not be able to access downstream I2C devices.
			SC to Pin(15)	Pin Short	Device will always NACK	I2C bus will have signal integrity issues, all I2C slaves will not respond and bus may get stuck.

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15	SDA	-0.5V … 7V	Short to V_{CC}	SC to supply	Potential damage to device if device ACK's to its address or a read transaction is occuring (in which the device is sending data to the master).	Damage likely to master; even if master can handle the large IoL, the master's driver will likely saturate and VoLs will be come large, potentially higher than ViL on slave devices on I2C bus. I2C communication may not work.
			Short to GND	SC to gnd	None	I2C bus will be inaccessable through I2C transactions.
			floating pin	bond open	Device will always NACK its own address	Master will not be able to access downstream I2C devices.
			SC to Pin(16)	Pin Short	Potential damage to device if device ACK's to its address or a read transaction is occuring (in which the device is sending data to the master).	Damage likely to master; even if master can handle the large IoL, the master's driver will likely saturate and VoLs will be come large, potentially higher than ViL on slave devices on I2C bus. I2C communication may not work.
16	Vcc	-0.5V … 7V	Short to V_{CC}	SC to supply	None	None
			Short to GND	SC to gnd	Damage may occur on a system level but may not occur to device.	Large current from Vcc to GND due to short. May damage power supply or cause large GND shift.
			floating pin	bond open	Device will not be functional.	Communication to downstream devices will not be possible, device is not funtional.