PCIe Simulation
Using WEBENCH Interface Designer
Fast and accurate Multi-Gbps Simulations

December 2016

Lee Sledjeski - SDS High Speed Datapath

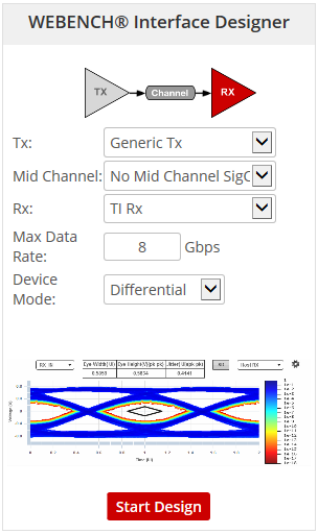
WEBENCH® Interface Designer

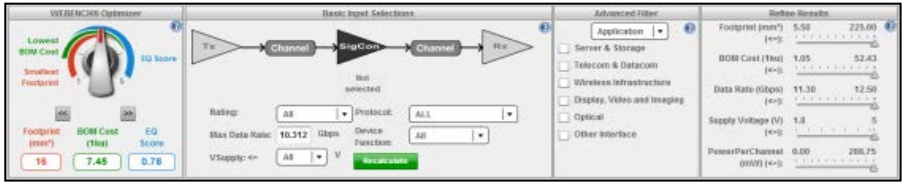
Quickly optimize signal integrity in high-speed designs

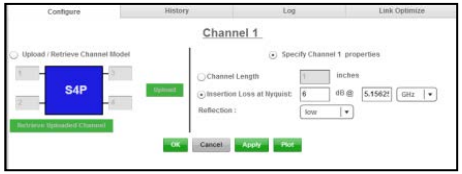
Start!

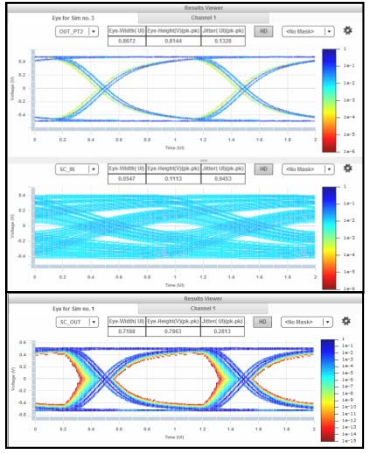
Select!

Sim!





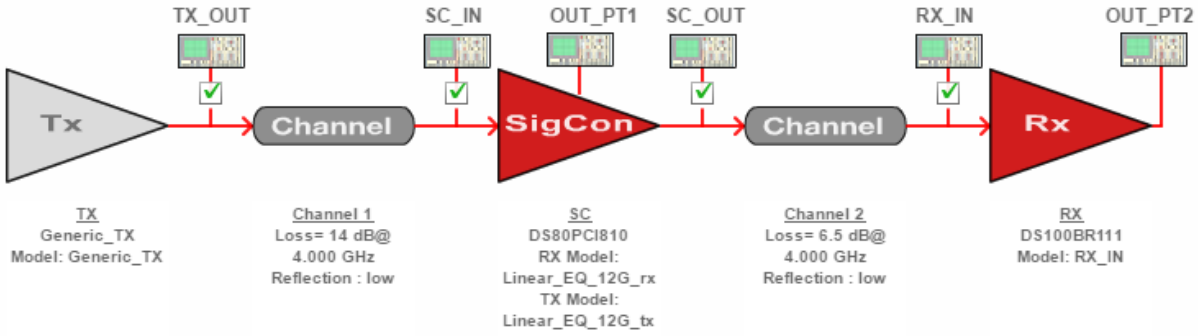




www.ti.com/interfacedesigner

Configure the Simulation Components

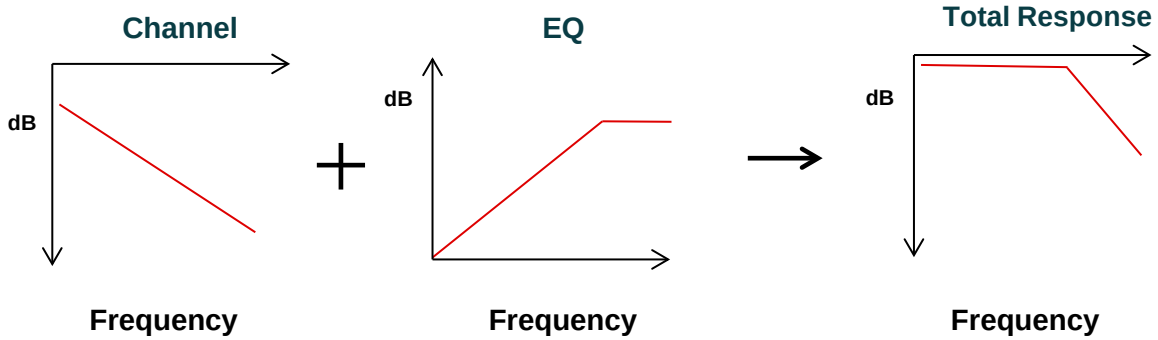
- **Transmit**
  - Utilize Tx FIR
  - Emulate PCIe settings



- **Channel**
  - Set “Insertion Loss at Nyquist” to define channel attenuation
- **Alternate Method for Channel**
  - Import your own S4P file to use in the simulation
- **Receiver**
  - Utilize TI CTLE to emulate PCIe Rx

Equalizer Theory

Continuous Time Linear Equalization (**CTLE**)



Common Terminology: Nyquist Frequency (GHz) = ½ Data Rate (Gbps)

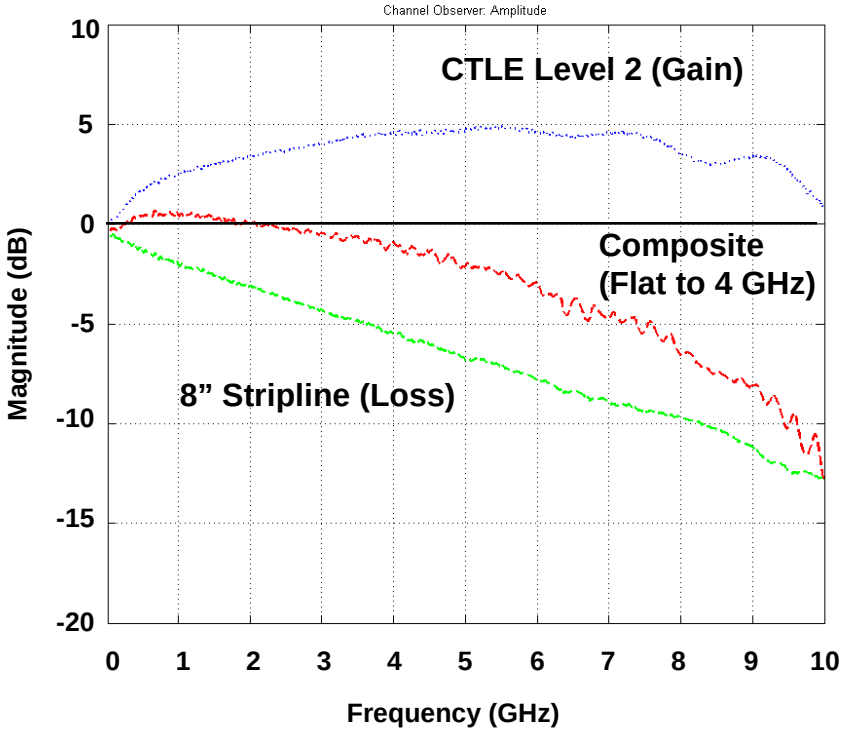
Equalizer goals:

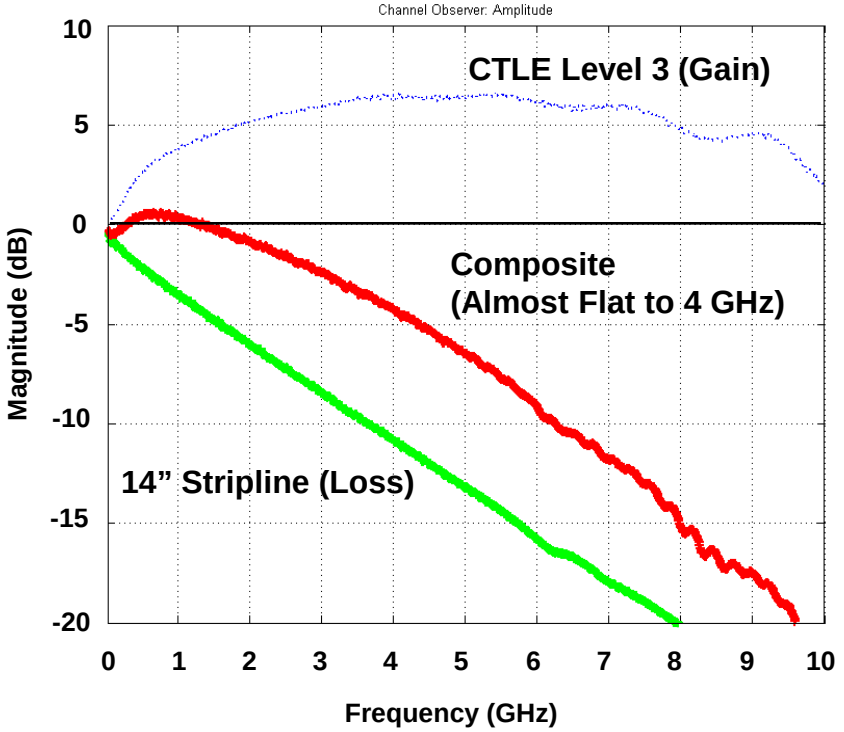
- ✓ Remove loss variations over frequency (ISI, Dj). Similar amplitude for higher-frequency signals and lower-frequency signals or make the loss ***equal*** over frequencies, hence "equalizer"
- ✓ Work with link training algorithms by remaining a linear function.

PCIe Linear Equalization Example

- Using Linear Equalization to compensate for channel losses and pass analog waveform information
  - Linear Equalization
  - Equalization (Link or Backchannel) Training
  - WEBENCH configuration
  - Simulation Results

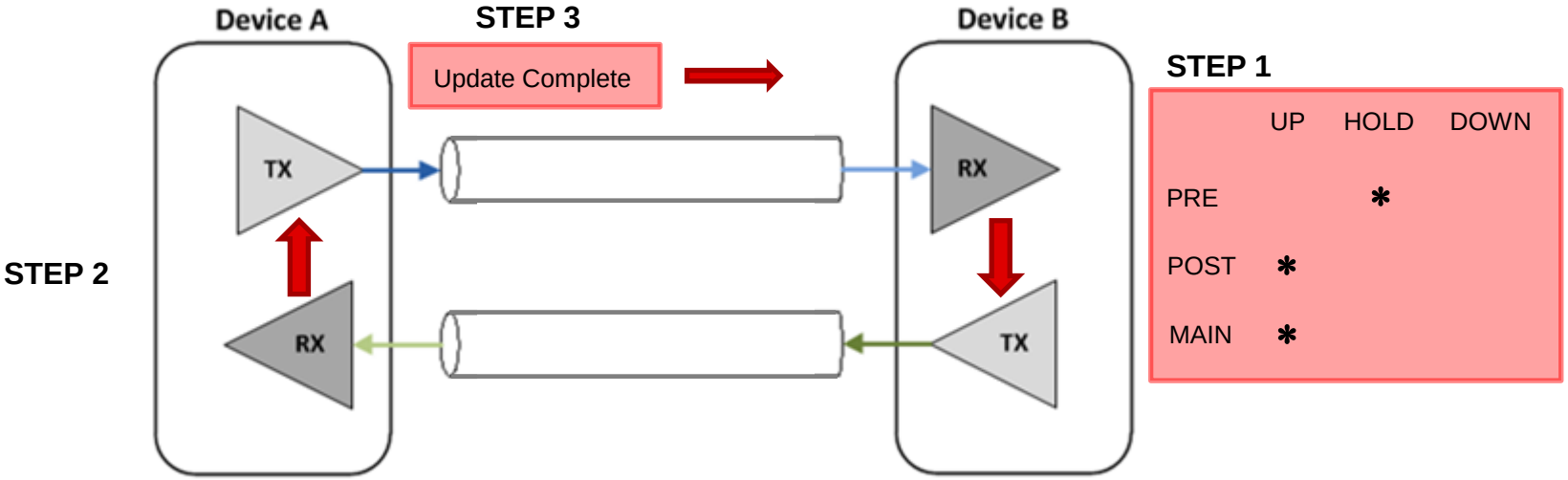
Linear Equalization Theory





Link Equalization Training

- **Many popular serial interfaces use this type of handshake**
  - PCIe (8 Gbps), 10G-KR (10 Gbps), SAS (12 Gbps)
  - Uses Rx EQ to tune the attached Tx FIR coefficients



PCIe - Transmit Equalization

PCI Express Transmit Preset Ratios

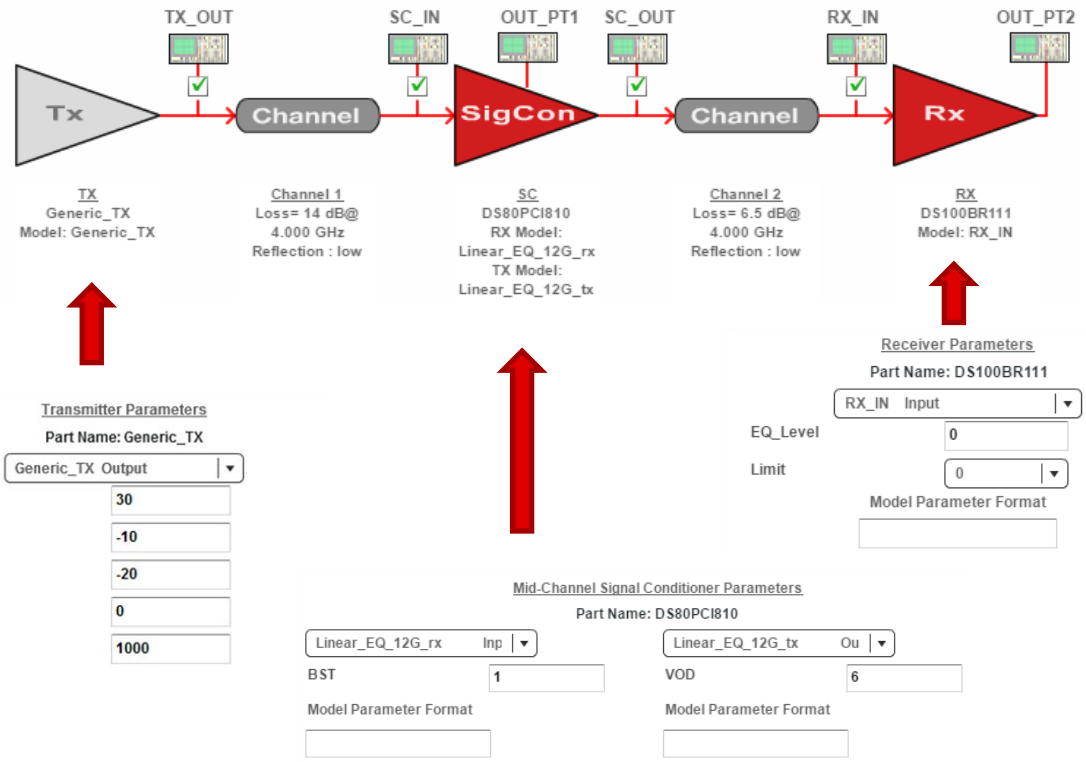
	PCIe Standard		WEBENCH Generic_TX Settings		
Preset Number	Pre-cursor (dB)	De-emphasis (dB)	Pre (%)	Pst1 (%)	Swing (mV)
P4	0.0	0.0	0.0	0.0	1000
P1	0.0	-3.5	0.0	-16.6	1000
P0	0.0	-6.0	0.0	-25.0	1000
P9	3.5	0.0	-16.6	0.0	1000
P8	3.5	-3.5	-12.5	-12.5	1000
P7	3.5	-6.0	-10.0	-20.0	1000
P5	1.9	0.0	-10.0	0.0	1000
P6	2.5	0.0	-12.5	0.0	1000
P3	0.0	-2.5	0.0	-12.5	1000
P2	0.0	-4.4	0.0	-20.0	1000
P10	0.0	-9.5	0.0	-33.0	1000

Gen 1

Gen 3

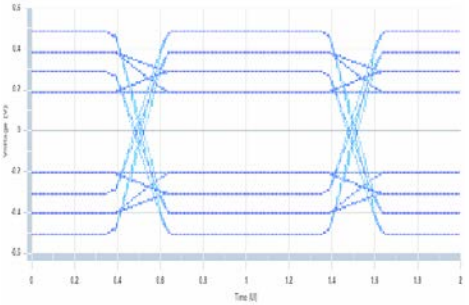
Simulation Setup with DS80PCI810

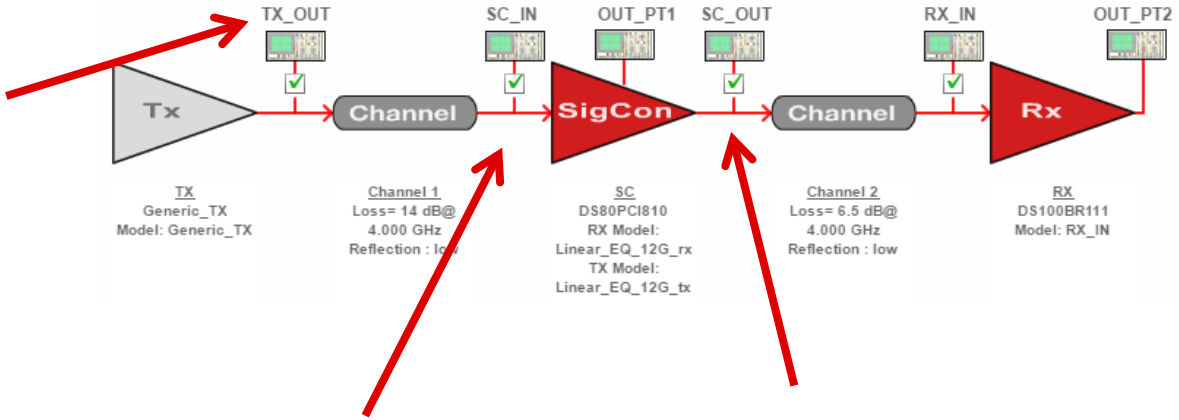
- **Configure Channel 1**
  - 14 dB loss
  - CPU Package + Trace
- **Configure Channel 2**
  - 6.5 dB loss
- **Models**
  - Tx set to Preset 7
  - SigCon set as shown
  - Rx set to 6 dB gain



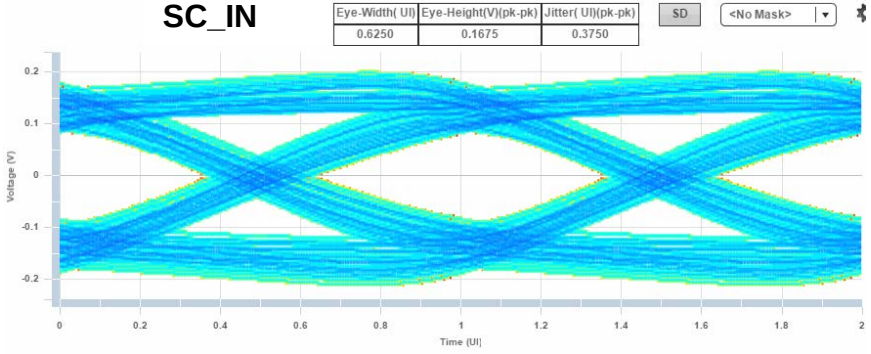
Simulation Results

TX_OUT

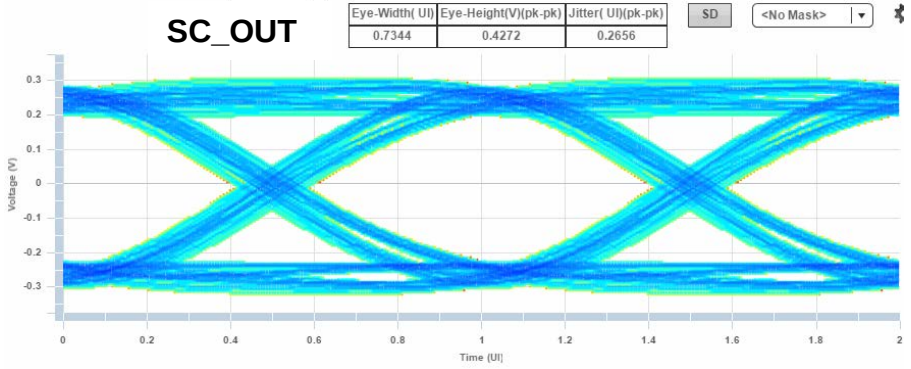




SC_IN

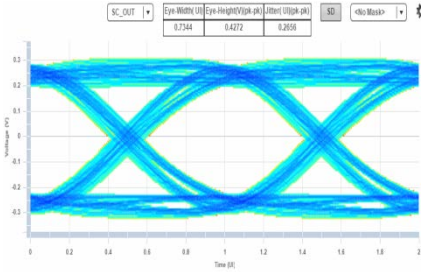


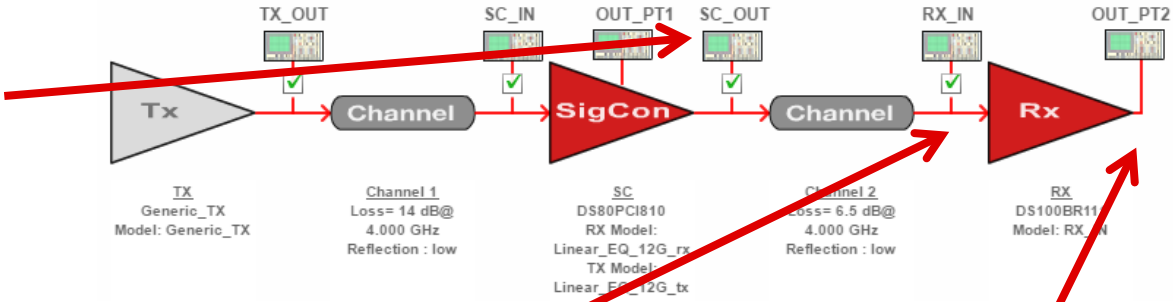
SC_OUT



Simulation Results

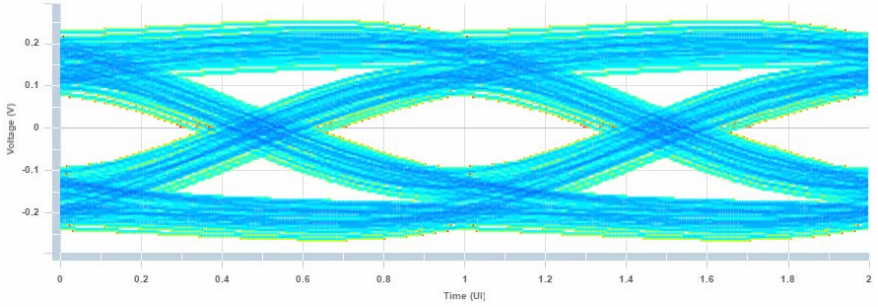
SC_OUT





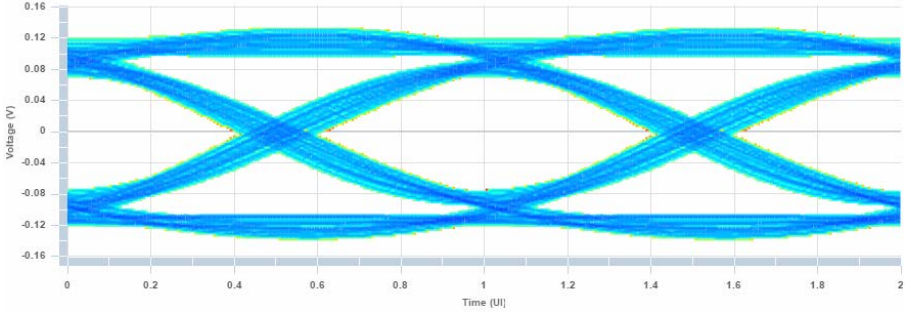
RX_IN

Eye-Width(UI)	Eye-Height(V)(pk-pk)	Jitter(UI)(pk-pk)	SD	<No Mask>
0.5156	0.1747	0.4844		



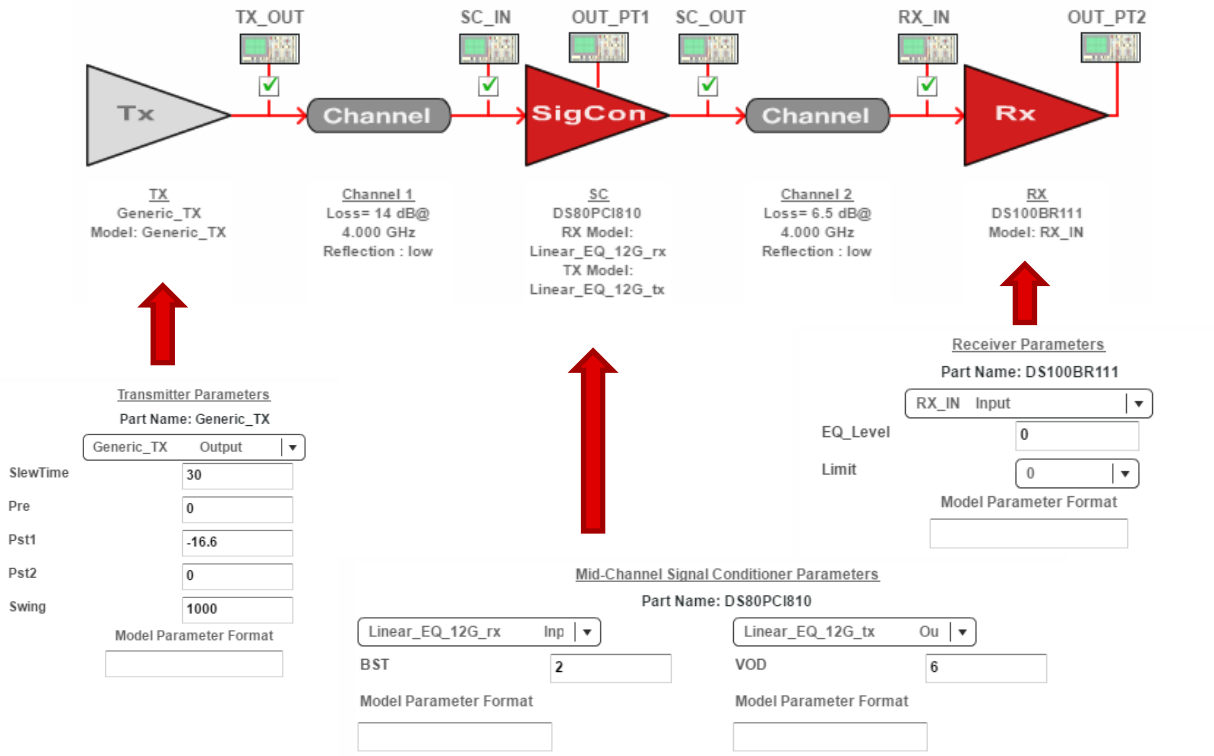
OUT_PT2 (CTLE Output)

Eye-Width(UI)	Eye-Height(V)(pk-pk)	Jitter(UI)(pk-pk)	SD	<No Mask>
0.7031	0.1489	0.2969		



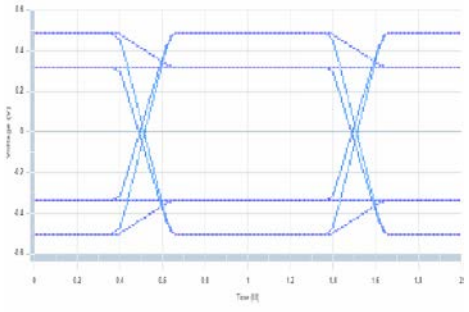
Simulation Setup with DS80PCI810

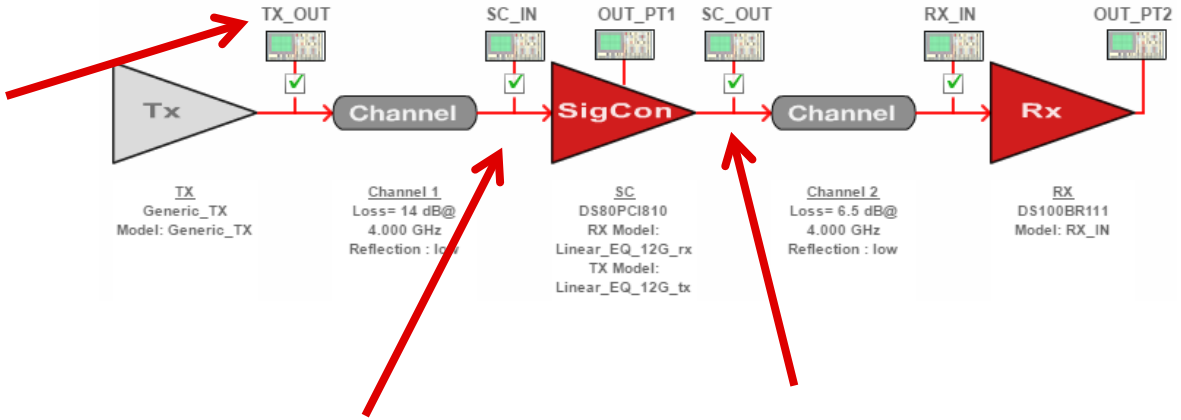
- **Configure Channel 1**
  - 14 dB loss
  - CPU Package + Trace
- **Configure Channel 2**
  - 6.5 dB loss
- **Models**
  - **Tx set to Preset 1**
  - SigCon set as shown
  - Rx set to 6 dB gain



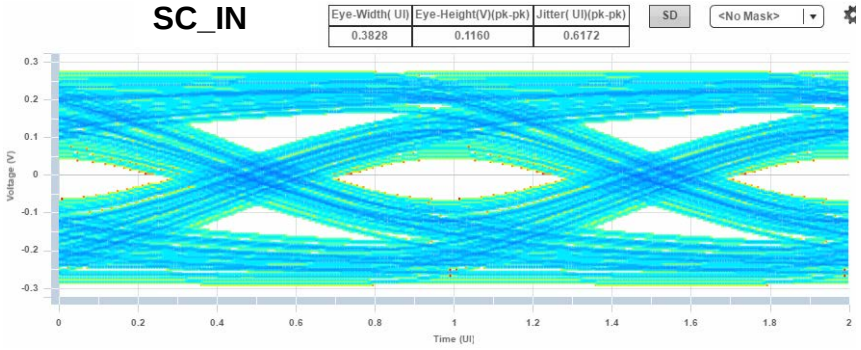
Simulation Results

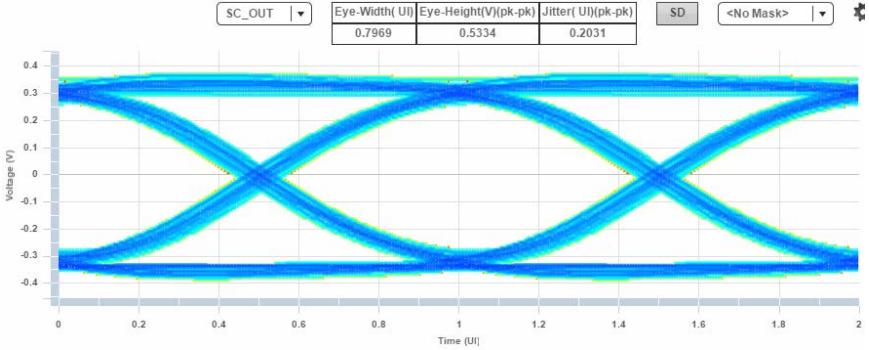
TX_OUT





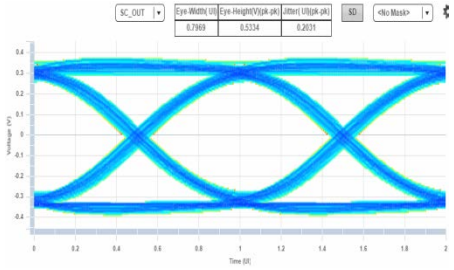
SC_IN

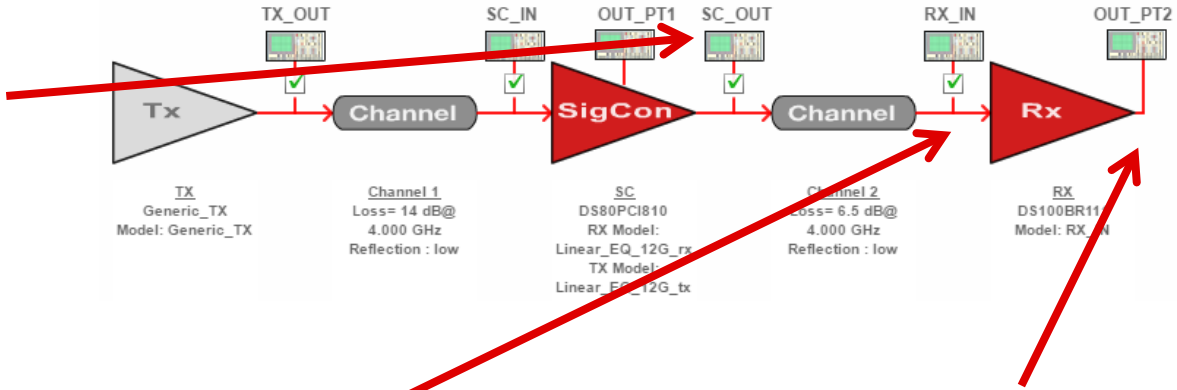




Simulation Results

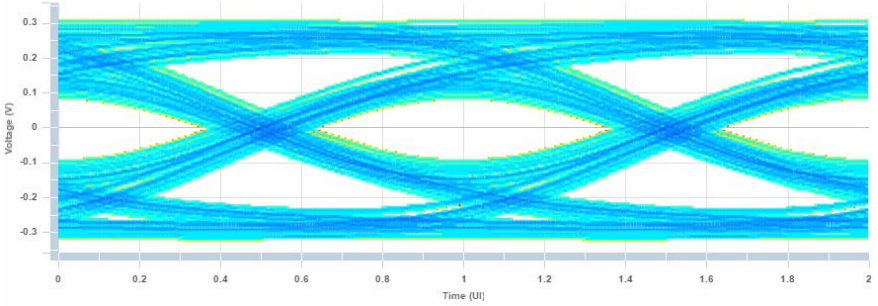
SC_OUT





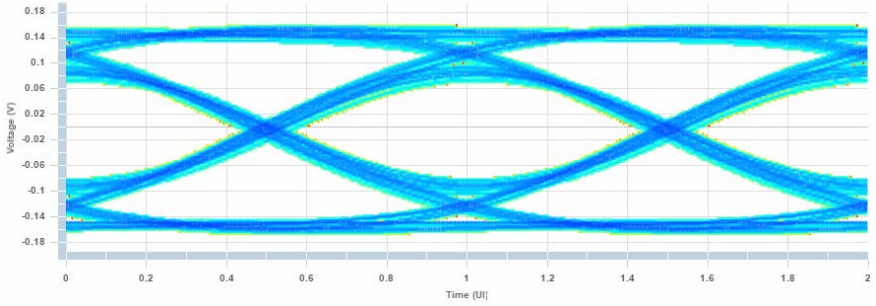
RX_IN

Eye-Width(UI)	Eye-Height(V)(pk-pk)	Jitter(UI)(pk-pk)	SD	<No Mask>
0.6016	0.1791	0.3984		



OUT_PT2 (CTLE Output)

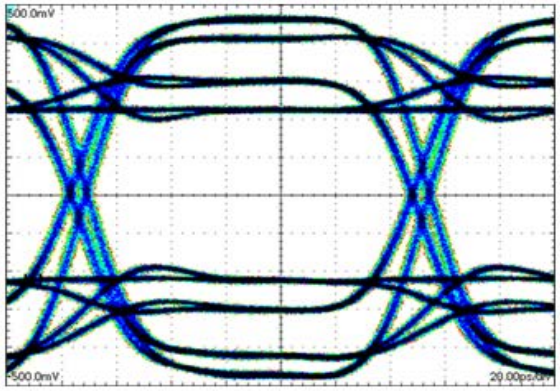
Eye-Width(UI)	Eye-Height(V)(pk-pk)	Jitter(UI)(pk-pk)	SD	<No Mask>
0.7422	0.1520	0.2578		

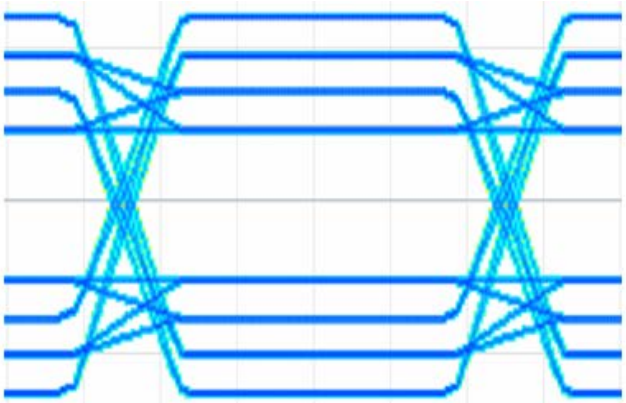


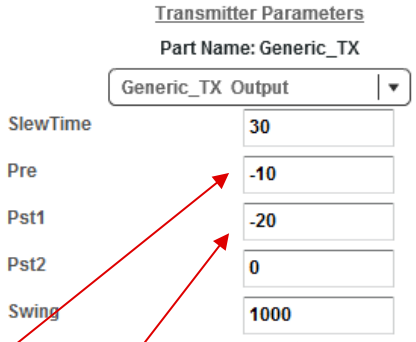
Extra Information
PCIe Simulation - Lab Correlation

PCIe Preset 7: Lab vs. WEBENCH Simulation

- Repurposed 25G TI Retimer IP as Tx generator to run at 8 Gbps



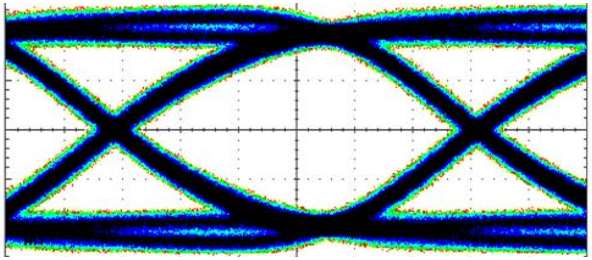




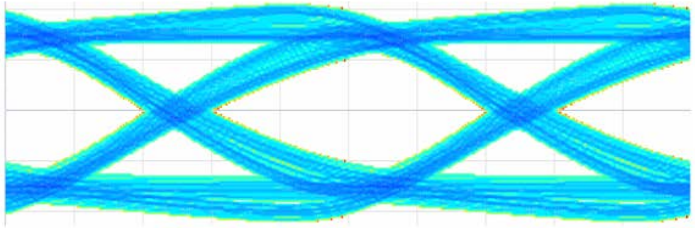
	PCIe Standard		WEBENCH Generic_TX Settings		
Preset Number	Pre-cursor (dB)	De-emphasis (dB)	Pre (%)	Pst1 (%)	Swing (mV)
P7	3.5	-6.0	-10.0	-20.0	1000

PCIe Preset 7: Driving 14” of Trace

Lab Measurement



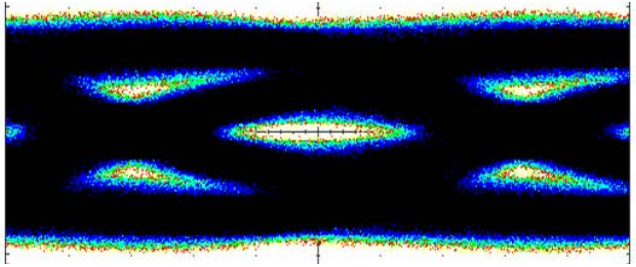
WEBENCH Simulation



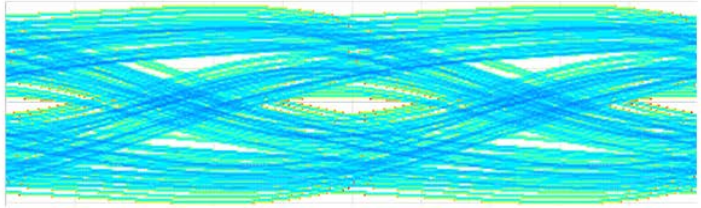
- Test Channel: PCIe Breakout + Short Calibration Channel
- Nominal Attenuation: -12 dB @ 4 GHz

PCIe Preset 7: Driving 24” of Trace

Lab Measurement



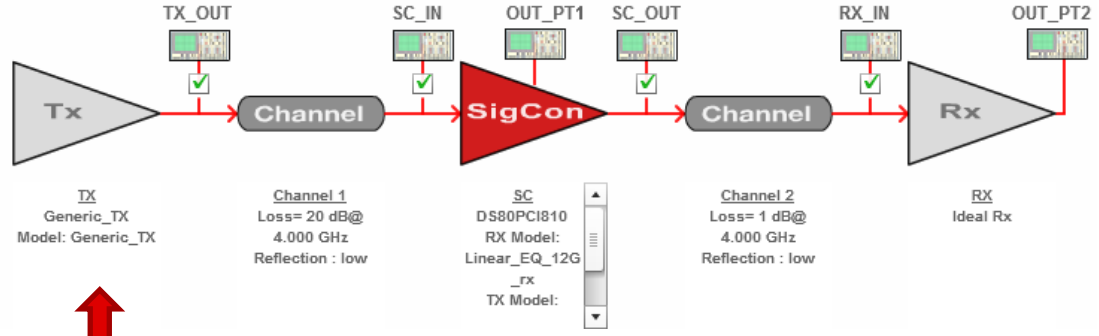
WEBENCH Simulation

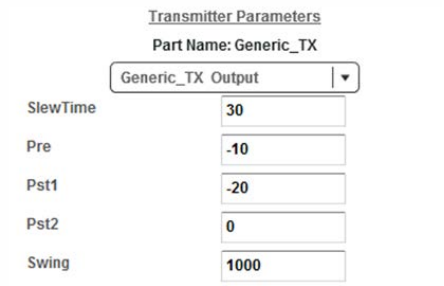


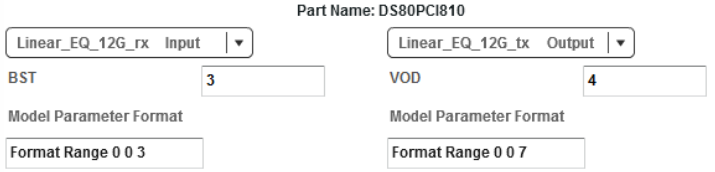
- Test Channel: PCIe Breakout + Long Calibration Channel
- Nominal Attenuation: -20 dB @ 4 GHz
- The open eye at 14” has collapsed due to the increased channel loss.

Simulation Window with DS80PCI810

- **Configure input channel**
  - 20 dB loss
  - Hit “Apply”
- **Configure output channel**
  - 1 dB loss
  - Hit “Apply”
- **Device configuration**
  - Set BST to 3
  - Set VOD to 4
  - Hit “Apply”

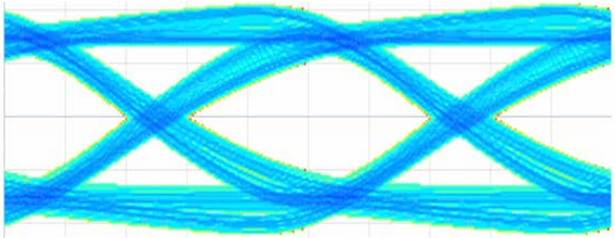




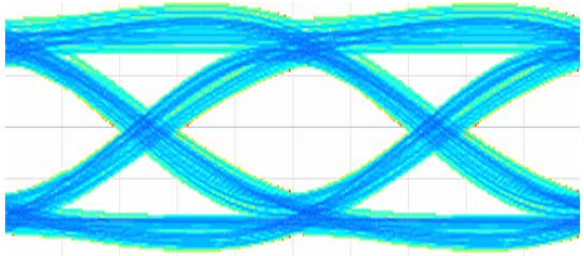


Effect of adding DS80PCI810 Linear Equalization

Simulation -12 dB
Without PCI810



Simulation -20 dB
With PCI810

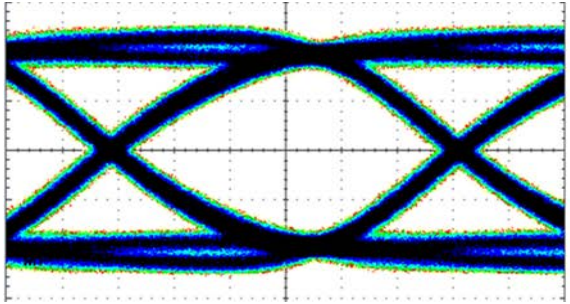


8 dB Reach Extension!!!

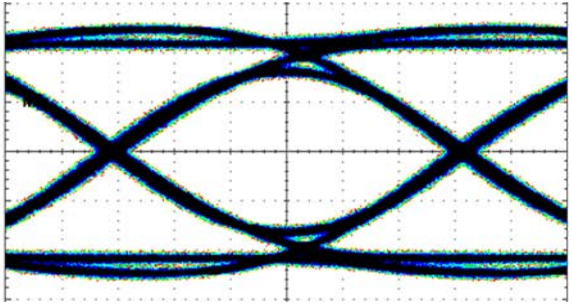
- DS80PCI810 Settings:
  - EQ = 11’b (Model Level 3 of 4)
  - VOD = 011’b (Model Level 4 of 8)
- Equalized waveform retains analog characteristics
  - **Required for equalization link training algorithms**

Effect of adding DS80PCI810 Linear Equalization

Lab Measurement 14”
Without PCI810



Lab Measurement 24”
With PCI810



- DS80PCI810 Settings:
  - EQ = 11’b (Model Level 3 of 4)
  - VOD = 011’b (Model Level 4 of 8)
  - VOD_DB = 000’b (Model Level 1 – minimum)

10” Reach Extension!!!