Table 11 describes the DP83822 configuration bootstraps:

Table 11. 4-Level Strap Pins

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
COL PU OK	29	[01] Current	MODE	FX_EN	PHY_AD0	**FX_EN:** Enables 100BASE-FX when set to '1' **PHY_AD0:** PHY Address bit[0]
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	0	1	
RX_D0 PD FIX	30	[10] Desired Current	MODE	AN_1	PHY_AD1	**AN_1:** See Table 12 below **PHY_AD1:** PHY Address bit[1]
			1 (Default)	1	0	
			2	0	0	
			3	0	1	
			4	1	1	
RX_D1 PD OK	31	[00] Current	MODE	EEE_EN	PHY_AD2	**EEE_EN:** Enables EEE operation when set to '1' **PHY_AD2:** PHY Address bit [2]
			1 (Default)	0	0	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D2 PD OK	32	[00] Current	MODE	FLD_EN	PHY_AD3	**FLD_EN:** Enables Fast Link Drop when set to '1'. Energy Detection, Low SNR threshold and RX_ER will be enabled. **PHY_AD3:** PHY Address bit[3]
			1 (Default)	0	0	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D3 PD FIX	1	[10] Desired Current	MODE	AN_EN	PHY_AD4	**AN_EN:** See Table 12 below **PHY_AD4:** PHY Address bit[4]
			1 (Default)	1	0	
			2	0	0	
			3	0	1	
			4	1	1	
LED_0 PU OK	17	[X1] Current	MODE	RESERVED	AN_0	**AN_0:** See Table 12 below
			1	X	0	
			2	X	0	
			3	X	1	
			4 (Default)	X	1	
CRS PU ? Maybe FIX	27	[01] Current Desired	MODE	LED_SPEED	LED_CFG	**LED_CFG:** See Table 13 below **LED_SPEED:** See Table 14 below
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	0	1	
RX_ER PU FIX	28	[01] Current Desired	MODE	RGMII_EN	AMDIX_EN (SD_EN)	**AMDIX_EN:** Enables Auto-MDIX when set to '1' **RGMII_EN:** See Table 15 below **SD_EN:** Enables 100BASE-FX Signal Detection on LED_1 when set to '1'. FX_EN strap must be enabled for SD_EN strap to be functional. Signal Detection is Active LOW, but polarity can be changed using the General Configuration Register (GENCFG, address 0x0465).
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	0	1	

Scope Strap Voltages
1.04V
OPEN-PU/1.96K PD
OPEN/OPEN 0V
OPEN/OPEN 0V
OPEN/OPEN 0V
3.3V
OPEN/OPEN
900mV
6.2K PU/1.96K-PD
3.3V
OPEN/OPEN

Checked HW Strap:
Already 1.96K PD
Already OPEN/OPEN
R243/R247 Already OPEN/OPEN
1.96K PU Added (Remove)? LINK Connected
Already Config 6.2K PU/ 1.96K PD
Already OPEN/ OPEN

LED1 - R193 Still connected? 2.74V Strap
1.42V After Remove R193

Table 11. 4-Level Strap Pins (continued)

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
RX_DV PD OK	26	[00]	MODE	XI_50	RMII_EN	XI_50: See Table 15 below RMII_EN: See Table 15 below OPEN/OPEN 0V
			1 (Default)	0	0	
			2	1	0	
			3	0	1	
			4	1	1	

Already OPEN/OPEN

Table 12. Modes of Operation

FX_EN	AN_EN	AN_1	AN_0	Description
Force Modes				
0	0	0	0	10BASE-Te, Half-Duplex
0	0	0	1	10BASE-Te, Full-Duplex
0	0	1	0	100BASE-TX, Half-Duplex
0	0	1	1	100BASE-TX, Full-Duplex
Advertised Modes				
0	1	0	0	10BASE-Te, Half-Duplex
0	1	0	1	10BASE-Te, Half/Full-Duplex
0	1	1	0	10BASE-Te, Half-Duplex 100BASE-TX, Half-Duplex
0	1	1	1	10BASE-Te, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex
Fiber Modes				
1	X	X	0	100BASE-FX, Half Duplex
1	X	X	1	100BASE-FX, Full Duplex

Table 13. LED_0 Configuration

Strap Mode	LED_CFG[0]	LED_0
4 & 3	1 ?	ON for Good Link OFF for No Link
2 & 1	0	ON for Good Link BLINK for TX/RX Activity

Table 14. LED_1 Configuration

Strap Mode	LED_SPEED	LED_1
4 & 1	0	LED_1 in Tri-State
3 & 2	1	ON for 100 Mbps SPEED OFF for 10 Mbps SPEED

Table 15. MAC Interface Configuration

RGMII_EN	RMII_EN	XI_50	Description
0	0	0	MII, 25-MHz Reference Clock
0	0	1	**Reserved**
0	1	0	RMII, 25-MHz Reference Clock
0	1	1	RMII, 50-MHz Reference Clock
1	X	0	RGMII, 25-MHz Reference Clock
1	X	1	**Reserved**

PHY1

Table 11 describes the DP83822 configuration bootstraps:

0x0467
0x0468

Table 11. 4-Level Strap Pins

Scope Strap Voltage | Checked Current Strap on HW:

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
COL PU FIX	29	[01] Current Desired	**MODE**	**FX_EN**	**PHY_AD0**	**FX_EN:** Enables 100BASE-FX when set to '1' **PHY_AD0:** PHY Address bit[0] 3.3V OPEN/OPEN
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	0	1	
RX_D0 PD FIX	30	[10] Desired Current	**MODE**	**AN_1**	**PHY_AD1**	**AN_1:** See Table 12 below **PHY_AD1:** PHY Address bit[1] OPEN/OPEN 0V
			1 (Default)	1	0	
			2	0	0	
			3	0	1	
			4	1	1	
RX_D1 PD OK	31	[00] Current	**MODE**	**EEE_EN**	**PHY_AD2**	**EEE_EN:** Enables EEE operation when set to '1' **PHY_AD2:** PHY Address bit [2] OPEN/OPEN 0V
			1 (Default)	0	0	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D2 PD OK	32	[00] Current	**MODE**	**FLD_EN**	**PHY_AD3**	**FLD_EN:** Enables Fast Link Drop when set to '1'. Energy Detection, Low SNR threshold and RX_ER will be enabled. **PHY_AD3:** PHY Address bit[3] 0V OPEN/OPEN
			1 (Default)	0	0	
			2	1	0	
			3	1	1	
			4	0	1	
RX_D3 PD FIX	1	[10] Desired Current	**MODE**	**AN_EN**	**PHY_AD4**	**AN_EN:** See Table 12 below **PHY_AD4:** PHY Address bit[4] 0V OPEN/OPEN
			1 (Default)	1	0	
			2	0	0	
			3	0	1	
			4	1	1	
LED_0 PU OK	17	[X1]	**MODE**	**RESERVED**	**AN_0**	**AN_0:** See Table 12 below 3.3V OPEN/OPEN
			1	X	0	
			2	X	0	
			3	X	1	
			4 (Default)	X	1	
CRS PU FIX	27	[01]	**MODE**	**LED_SPEED**	**LED_CFG**	**LED_CFG:** See Table 13 below **LED_SPEED:** See Table 14 below 158mV 6.2K-PU/1.96K-PD
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	0	1	
RX_ER PU FIX	28	[01]	**MODE**	**RGMII_EN**	**AMDIX_EN (SD_EN)**	**AMDIX_EN:** Enables Auto-MDIX when set to '1' **RGMII_EN:** See Table 15 below **SD_EN:** Enables 100BASE-FX Signal Detection on LED_1 when set to '1'. FX_EN strap must be enabled for SD_EN strap to be functional. Signal Detection is Active LOW, but polarity can be changed using the General Configuration Register (GENCFG, address 0x0465). 3.3V OPEN/OPEN
			1	0	0	
			2	1	0	
			3	1	1	
			4 (Default)	0	1	

Checked Current Strap on HW:

Already OPEN/OPEN

Already OPEN/OPEN

Already OPEN/OPEN

Already OPEN/OPEN

Already OPEN/OPEN

Already 6.2K-PU/1.96K-PD

Already OPEN/OPEN

LED1 - 2.7V

PHY1

Table 11. 4-Level Strap Pins (continued)

PIN NAME	PIN #	DEFAULT	STRAP FUNCTION			DESCRIPTION
			MODE	XI_50	RMII_EN	
RX_DV PD	26	[00]	1 (Default)	0	0	XI_50: See Table 15 below RMII_EN: See Table 15 below
OK			2	1	0	
			3	0	1	
			4	1	1	

0V

OPEN/OPEN

Already OPEN/OPEN

Table 12. Modes of Operation

FX_EN	AN_EN	AN_1	AN_0	Description
Force Modes				
0	0	0	0	10BASE-Te, Half-Duplex
0	0	0	1	10BASE-Te, Full-Duplex
0	0	1	0	100BASE-TX, Half-Duplex
0	0	1	1	100BASE-TX, Full-Duplex
Advertised Modes				
0	1	0	0	10BASE-Te, Half-Duplex
0	1	0	1	10BASE-Te, Half/Full-Duplex
0	1	1	0	10BASE-Te, Half-Duplex 100BASE-TX, Half-Duplex
0	1	1	1	10BASE-Te, Half/Full-Duplex 100BASE-TX, Half/Full-Duplex
Fiber Modes				
1	X	X	0	100BASE-FX, Half Duplex
1	X	X	1	100BASE-FX, Full Duplex

Table 13. LED_0 Configuration

Strap Mode	LED_CFG[0]	LED_0
4 & 3	1	ON for Good Link OFF for No Link
2 & 1	0	ON for Good Link BLINK for TX/RX Activity

Table 14. LED_1 Configuration

Strap Mode	LED_SPEED	LED_1
4 & 1	0	LED_1 in Tri-State
3 & 2	1	ON for 100 Mbps SPEED OFF for 10 Mbps SPEED

Table 15. MAC Interface Configuration

RGMII_EN	RMII_EN	XI_50	Description
0	0	0	MII, 25-MHz Reference Clock
0	0	1	**Reserved**
0	1	0	RMII, 25-MHz Reference Clock
0	1	1	RMII, 50-MHz Reference Clock
1	X	0	RGMII, 25-MHz Reference Clock
1	X	1	**Reserved**