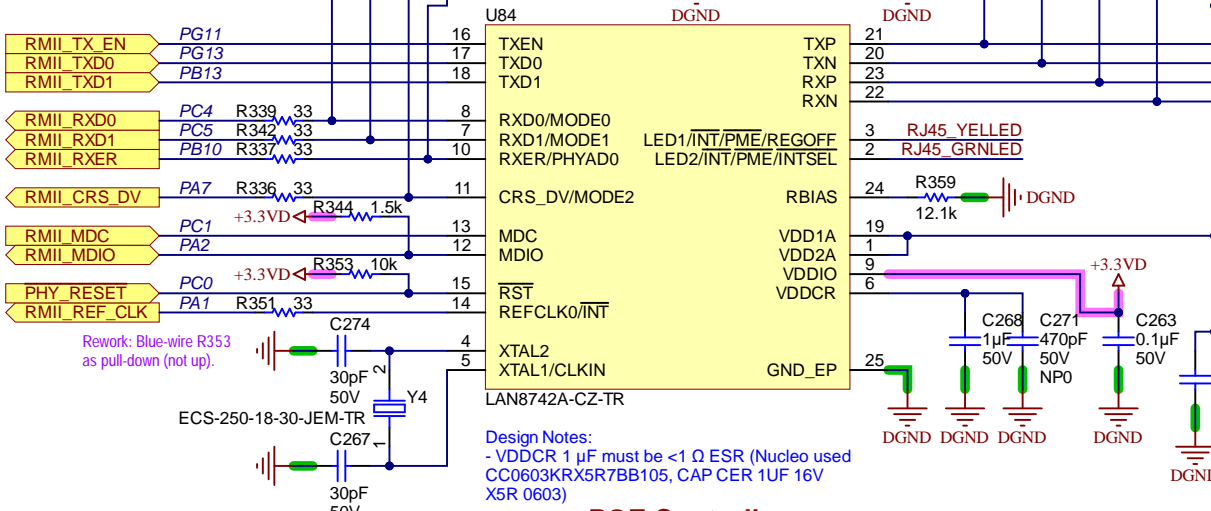


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Ethernet & POE

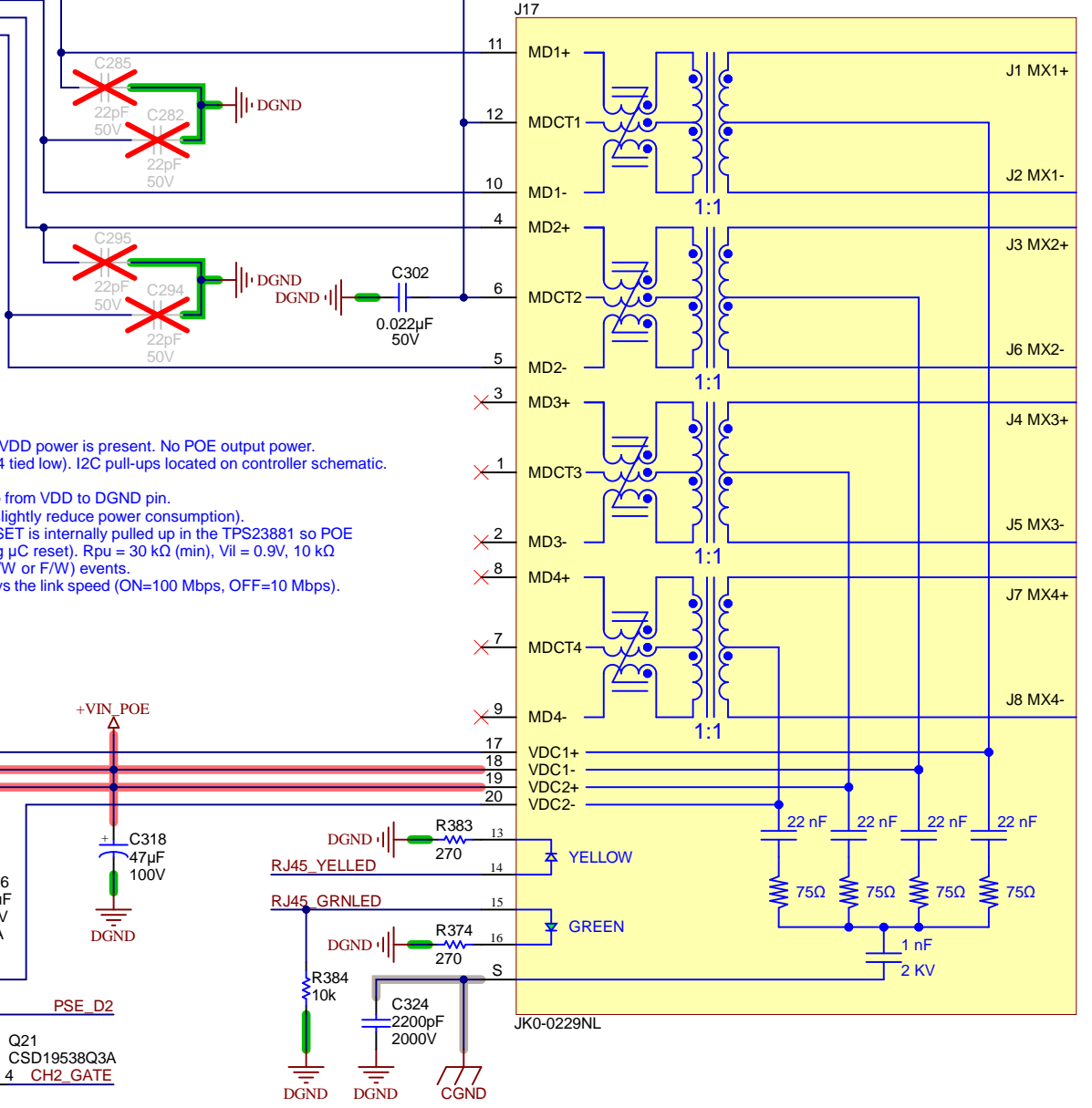
ToDos:
 - And one more thing.....

Ethernet μ C Interface



Place 49.9 Ohm resistors close to LAN8742.

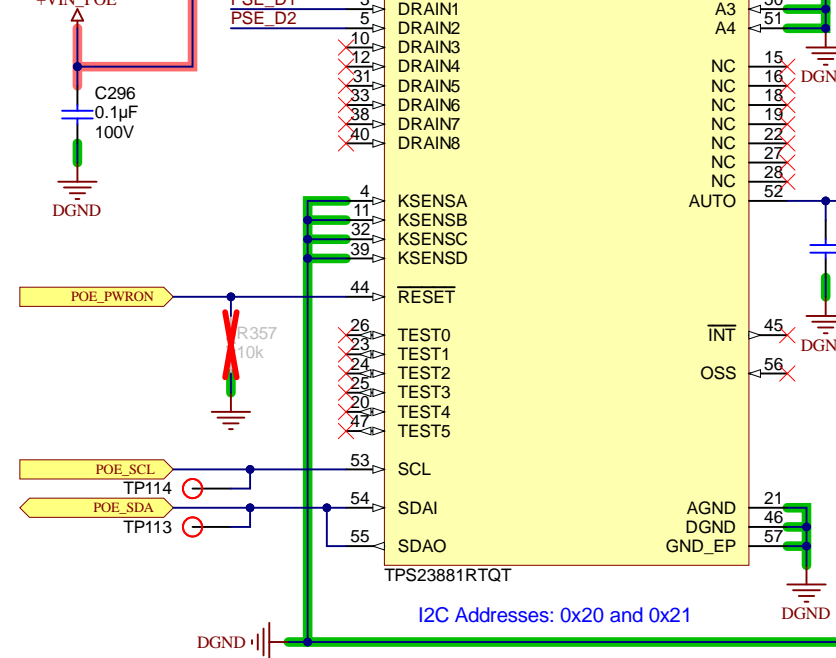
Ethernet RJ-45 Jack



POE Controller

Design Notes:
 - OK for POE controller VPWR input connected to power before VDD power is present. No POE output power.
 - The TPS23881 I2C device base address is fixed at 0x20 (A1-A4 tied low). I2C pull-ups located on controller schematic.
 - POE AUTO mode set for 4-pair, 30W.
 - VPWR bypass cap from VPWR to AGND pin. VDD bypass cap from VDD to DGND pin.
 - DRAINx pins can be grounded or left open (leaving open may slightly reduce power consumption).
 - Pulling \P_OE_RESET low turns off the POE power output. \RESET is internally pulled up in the TPS23881 so POE power will turn on if \P_OE_RESET is high impedance (e.g. during μ C reset). Rpu = 30 k Ω (min), V_{il} = 0.9V, 10 k Ω pull-down DNP to prevent POE power turning off during reset (H/W or F/W) events.
 - LED1 (yellow) displays link status/activity. LED2 (green) displays the link speed (ON=100 Mbps, OFF=10 Mbps). Configuration can be changed, this is the default.

POE Supply



Ref. TPS23881 data sheet 12.1 for layout guidelines.

Variant: ESDFixes-DRF-G

Title			PAE_Main		
Size: B	Number: 10101	Revision: A			
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