Ethernet & POE

ToDos:
- And one more thing.....

Ethernet µC Interface

RMII_TX_EN PG11 16
RMII_TXD0 PG13 17
RMII_TXD1 PB13 18
RMII_RXD0 PC4 R339 33 8
RMII_RXD1 PC5 R342 33 7
RMII_RXER PB10 R337 33 10
RMII_CRS_DV PA7 R336 33 11
+3.3VD R344 1.5k
RMII_MDC PC1 13
RMII_MDIO PA2 12
+3.3VD R353 10k
PHY_RESET PC0 15
RMII_REF_CLK PA1 R351 33 14

Rework: Blue-wire R353 as pull-down (not up).

C274 30pF 50V
Y4 ECS-250-18-30-JEM-TR
C267 30pF 50V

+3.3VD L15 600 Ohms @ 100MHz
C289 10µF 25V
C276 10µF 16V
R340 R341 R335 R338 10k
R365 R363 R369 R368 49.9

Place 49.9 Ohm resistors close to LAN8742.

U84 LAN8742A-CZ-TR

TXEN	16	21	TXP
TXD0	17	20	TXN
TXD1	18	23	RXP
		22	RXN
RXD0/MODE0	8		
RXD1/MODE1	7	3	LED1/INT/PME/REGOFF → RJ45_YELLED
RXER/PHYAD0	10	2	LED2/INT/PME/INTSEL → RJ45_GRNLED
CRS_DV/MODE2	11	24	RBIAS — R359 12.1k
MDC	13	19	VDD1A
MDIO	12	1	VDD2A
RST	15	9	VDDIO
REFCLK0/INT	14	6	VDDCR
XTAL2	4		
XTAL1/CLKIN	5	25	GND_EP

C268 1µF 50V
C271 470pF 50V NP0
C263 0.1µF 50V
C277 0.1µF 50V
C275 0.1µF 50V

Design Notes:
- VDDCR 1 µF must be <1 Ω ESR (Nucleo used CC0603KRX5R7BB105, CAP CER 1UF 16V X5R 0603)

TD_P ENET
TD_N ENET
RD_P ENET
RD_N ENET

D31 D5V0P4UR6SO-7 (I/O1 I/O4 GND VDD I/O2 I/O3)

D32 UCLAMP3301D.TCT

C285 22pF 50V
C282 22pF 50V
C295 22pF 50V
C294 22pF 50V
C302 0.022µF 50V

Ethernet RJ-45 Jack

J17 JK0-0229NL

MD1+	11	J1 MX1+
MDCT1	12	
MD1-	10	J2 MX1-
		1:1
MD2+	4	J3 MX2+
MDCT2	6	
MD2-	5	J6 MX2-
		1:1
MD3+	3	J4 MX3+
MDCT3	1	
MD3-	2	J5 MX3-
		1:1
MD4+	8	J7 MX4+
MDCT4	7	
MD4-	9	J8 MX4-
		1:1
VDC1+	17	
VDC1-	18	
VDC2+	19	
VDC2-	20	

22 nF 22 nF 22 nF 22 nF
75Ω 75Ω 75Ω 75Ω
1 nF 2 KV

R383 270 — RJ45_YELLED — YELLOW
R374 270 — RJ45_GRNLED — GREEN
R384 10k
C324 2200pF 2000V
DGND DGND CGND

POE Controller

U85 TPS23881RTQT

VDD	43	GAT1	1 → CH1_GATE
VPWR	17	GAT2	7 → CH2_GATE
		GAT3	8
		GAT4	14
		GAT5	29
		GAT6	35
		GAT7	36
		GAT8	42
SEN1	2 ← CH1_SEN		
SEN2	6 ← CH2_SEN		
SEN3	9		
SEN4	13		
SEN5	30		
SEN6	34		
SEN7	37		
SEN8	41	A1	48
		A2	49
		A3	50
		A4	51
DRAIN1	3 ← PSE_D1	NC	15
DRAIN2	5 ← PSE_D2	NC	16
DRAIN3	10	NC	18
DRAIN4	12	NC	19
DRAIN5	31	NC	22
DRAIN6	33	NC	27
DRAIN7	38	NC	28
DRAIN8	40	NC	52
		AUTO	
KSENSA	4		
KSENSB	11		
KSENSC	32		
KSENSD	39		
RESET	44 ← POE_PWRON		
TEST0	26	INT	45
TEST1	23		
TEST2	24	OSS	56
TEST3	25		
TEST4	20		
TEST5	47		
SCL	53 ← POE_SCL		
SDAI	54 ← POE_SDA		
SDAO	55		
		AGND	21
		DGND	46
		GND_EP	57

C272 10000pF 50V
R352 35.7k
R357 10k
TP114 POE_SCL
TP113 POE_SDA

I2C Addresses: 0x20 and 0x21

Design Notes:
- OK for POE controller VPWR input connected to power before VDD power is present. No POE output power.
- The TPS23881 I2C device base address is fixed at 0x20 (A1-A4 tied low). I2C pull-ups located on controller schematic.
- POE AUTO mode set for 4-pair, 30W.
- VPWR bypass cap from VPWR to AGND pin. VDD bypass cap from VDD to DGND pin.
- DRAINx pins can be grounded or left open (leaving open may slightly reduce power consumption).
- Pulling \POE_RESET low turns off the POE power output. \RESET is internally pulled up in the TPS23881 so POE power will turn on if \POE_RESET is high impedance (e.g. during µC reset). Rpu = 30 kΩ (min), Vil = 0.9V, 10 kΩ pull-down DNP to prevent POE power turning off during reset (H/W or F/W) events.
- LED1 (yellow) displays link status/activity. LED2 (green) displays the link speed (ON=100 Mbps, OFF=10 Mbps). Configuration can be changed, this is the default.
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Ref. TPS23881 data sheet 12.1 for layout guidelines.

POE Supply

+VIN_POE
C296 0.1µF 100V
C273 0.1µF 50V

C315 0.1µF 100V — D34 SMBJ51CA
C316 0.1µF 100V — D33 SMBJ51CA
C318 47µF 100V

PSE_D1 — Q20 CSD19538Q3A — CH1_GATE — CH1_SEN — R379 200m
PSE_D2 — Q21 CSD19538Q3A — CH2_GATE — CH2_SEN — R380 200m

Variant: ESDFixes-DRF-G

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