

AM69 Processor Starter Kit

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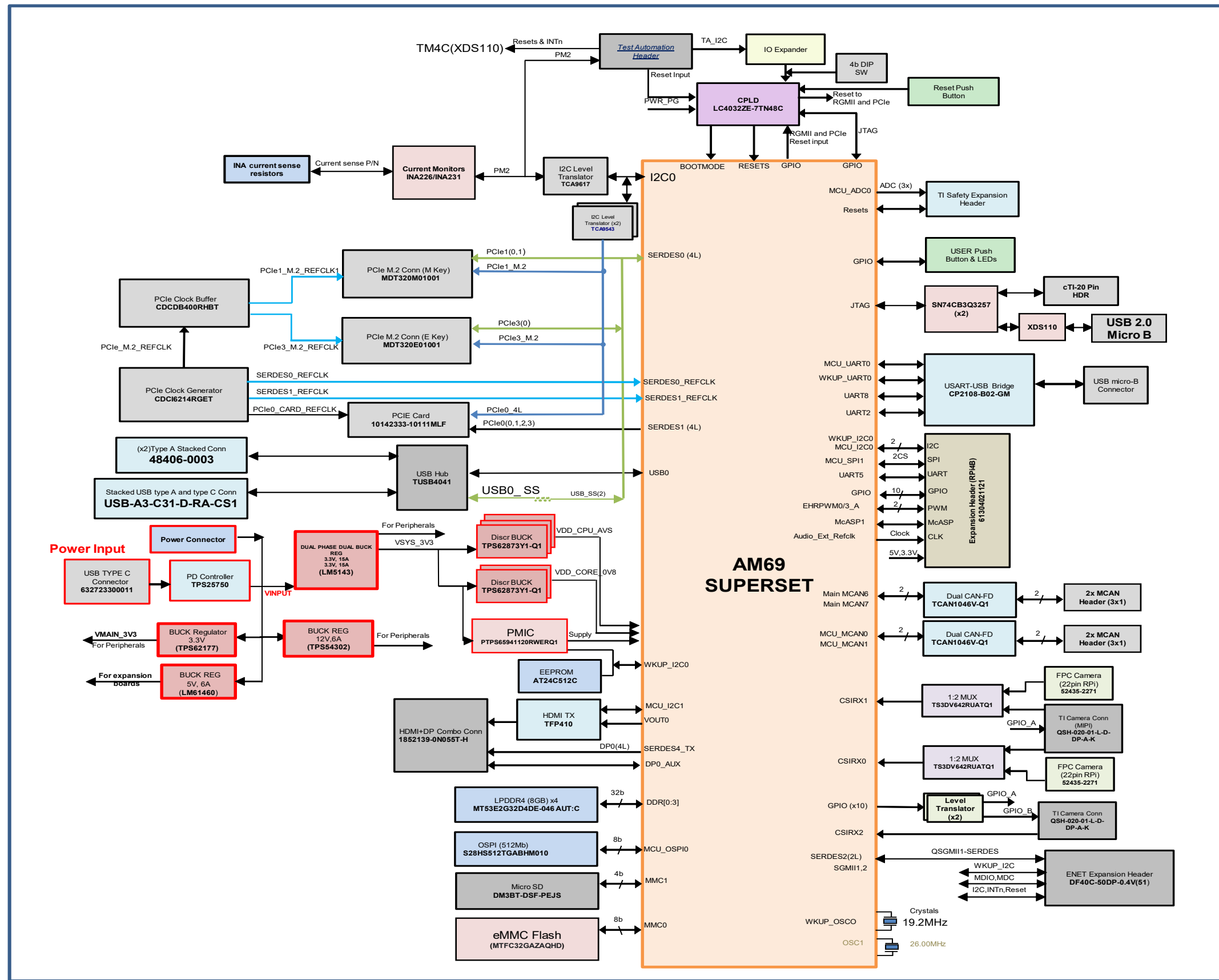
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REVISION HISTORY

REV #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
E2	21 OCT 2022	Taken AM69 SK Rev E1 design as reference and Added CDCI6214 clock generators for PCIe devices	Mistral Design Team		
	2 NOV 2022	1. Replaced U113 with clock buffer CDCDB400 as a clock source for PCIe M key and E key. 2. Updated U50 connection to provide resistor mux for CDCI1_OE2/OE3 and CDCI1_OE1/OE4 signals from U112	Mistral Design Team		
E2A	23 FEB 2023	Added ECN information for TIVA automation rework.	Mistral Design Team		
E2B	13 MAR 2023	1.Updated L1 L6 part number to XAL7070-122MEC 2.Updated U76 U78 part number to BSZ019N03LSATMA1	Mistral Design Team		
E3	16 MAR 2023	1.Updated L1 L6 part number to XAL7070-102MEC 2.Updated U76 U78 part number to CSD18563Q5A 3.Updated U75 U81 part number to CSD18543Q3A. 4. C36, R48,C42, R50 values have been modified. 5.TA_I2C_SCL , TA_I2C_SDA have been swapped with PM2_SCL, PM2_SDA. 6.Updated FB1, L28, R130, R368,R347,R267 to 0E for EMC compliance. 7.Made C801, C448, C441,C111 DNI.	Mistral Design Team		

SYSTEM BLOCK DIAGRAM



PDN Recommended for New Designs

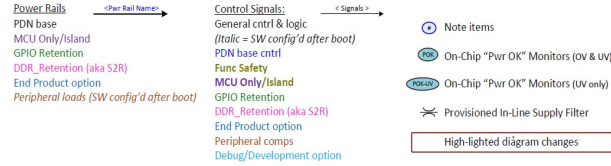
J784S4 EVM Leo + 2x High-Current Pwr Stages(HPCS) PDN-3H.1

(All SoC PN variants: TDA4AP/VP/AH/VH)
(Power Rail & GPIO Mapping Overview)

PDN-3H.1 History
V0.6 10/05/2023

- BMC: Initial capture J784S4 EVM Single Leo Dual HPCS PDN-3H.1 derived from PDN-3H v0.6 with following changes:
1. Removed in-line Safety FET to reduce cost & area
 2. Removed Safety Voltage Supervisor
 3. Removed Load Switch supplying VDD_IO_V3V to SoC and updated Note 2.
 4. Add SEL_V3V_VBns control signal to PMIC's GPIOs from SoC GPIO to provision LDO2 to supply dual VIO for SD card HS-D operation

Legend:



Notes:

- 1) An end product's Functional Safety desired ASIL target may require monitoring key "safety critical" power rails (i.e. VSYS_V3V input, key SoC supplies) that could cause severe system failures. This classification depends on the end product use case & what SoC resources a customer is using that are considered to be safety-related. SoC has internal OV & UV monitoring for key SoC MCU & Main Voltage domains. The status is reported by SoC's Power OK (POK) status bits. Optional SoC voltage monitoring inputs (i.e. VMONn_R_VDDn) can be used to extend SoC's (OV/UV) monitoring to a few board level power rails if desired (i.e. load switch Vn = VDD_IO_V3V). The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHVS (SD Card), VPP_CORE, VPP_MCU, VDDA_3P3_USB & VDD1_LPDD04_V1B.
- 2) Load Switches (L2W) in-line with VSYS_V3V can be removed to reduce PCB area & BOM cost depending upon an end product's system operation & desired features. Reasons to remove load switches from 3.3V power rails:
 - A) No latent fault protection is desired that could isolate any or all 3.3V SoC input supplies from a 1st power stage fault resulting in damage to SoC.
 - B) No system low power modes of operation (i.e. MCU Only, DDR Retention or GPIO Retention) are desired.
 - C) Full SoC PDN system power up & down sequences can be synchronized with enabling & disabling of the 1st power stage supplying VSYS_V3V input.
 - D) Enabling & disabling of SoC PDN must be executed with 1st power stage to avoid partially powering SoC for extended time periods that can negatively impact POH reliability.
 Reasons to use 3.3V load switches on 3.3V power rails:
 - A) Latent fault protection from 1st power stage that can avoid damaging SoC is desired.
 - B) Any one of the possible system low power modes of operation (i.e. MCU Only, DDR Retention or GPIO Retention) is desired.
 - C) Independent SoC power supply sequencing by PMIC resources ensures correct system start-up & shut-down timing delays per NVM settings.
 - D) Uncontrolled energizing of SoC 3.3V supplies is prevented since this will partially power SoC for extended time periods that can negatively impact POH reliability.
- 3) PMIC's GPIO_4 has been provisioned to support multiple on-state signals. The PMIC_Pwr_Disable function sets GPIO_4 = DISABLE. WDOG function following NVM initialization. This GPIO's default function can be reconfigured by system SW following SoC boot if another interface signal is needed that is not required for SoC power sequencing.
 1. Default: GPIO_4 = DISABLE. WDOG function to operate with EVM's DISABLE_WDOG signal that is latched on rising edge of PMIC's nRSTOUT = H_MCU_POR2_V1B at end of power up seq. A logic low enables normal watch dog timer operation while a logic high disables watch dog timer following a power up seq.
 2. Option 1: After system SW boots, SW can reconfigure GPIO_4 = GPI function to operate with PMIC's MAIN_PWRGRP_IRQn (asserted high = load signal). System SW must mask GPIO4 before changing GPIO's assigned function. After selecting GPI function, SW must mask GPI input and select whether the GPI will be either rising or falling edge sensitive. If any main domain processing supply rail has a fault, the changing logic level on GPIO4 will set internal register bit that is monitored by PMIC's power state machine and cause a transition from Full Active state to MCU Safe state. At the board level, the WDOG_DISABLE & MAIN_PWRGRP_IRQn signals are "time mux" onto GPIO4's input pin by using a 1-to-2 state buffer with OE control connected to H_MCU_POR2_V1B. This enables WDOG_DISABLE to set GPIO4's logic level during power up seq when H_MCU_POR2_V1B = low since buffer is tri-stated. After power up seq, H_MCU_POR2_V1B = high enabling buffer to drive MAIN_PWRGRP_IRQn logic level into GPIO4 input.
 3. Option 2: GPIO_4 = WKUP1 function can be selected by SW to operate with SoC's PMIC_PWR_EN1 signal for simulator debug control of MCU power resources (i.e. enabling VDD_CORE to activate core logic required to support JTAG signaling across the device). Combining board level WDOG_DISABLE & PMIC_PWR_EN1 signals using a resistor network is possible since WDOG_DISABLE pulls logic level high when switch is closed. Afterwards, switch can be opened and PMIC_PWR_EN1 signal will drive GPIO_4.
- 4) GPIO Retention (aka GPIO_RET_IO_RET_IO_Wake) low power mode requires:
 - A) SoC SW executes command sequence that sets key PMIC register bits in order to enter GPIO_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
 - B) After entering GPIO_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
 1. VDD_GPIORET_WK_OV8 supplying MCU's VDD_MCU_WAKE1 for MCU's D.8V wake-up logic.
 2. VDD_GPIORET_IO_V3V supplying MCU's VDDSHV_MCU for MCU's 3.3V IO toggle activity.
 - C) PDN system exits GPIO_RET state upon receiving high toggles on SoC's MCU monitored IO signals w/ VDDSHV_MCU supply. Then H_MCU_WAKE1n (= SoC's Open Drain PMIC_WAKE1n, active low) signal connected to PMIC_GPIO_4 (= WKUP1 default function for Full Active or = WKUP2 for MCU Only destination state) is asserted and PMIC state machine transitions PDN system to desired targeted wake-up state.
 - D) The Open-Drain Buffer SN74ALVC125(07B1) tri-states IO when power is off) connects PMIC_WAKE1n to SoC_PWR_Wkin net at discrete open-drain FET node. It is needed to isolate the SoC output buffer from the always on VCCA_V3V used as pull-up supply to prevent current bleeding into SoC during low power modes (MCU Only, DDR_RET) when VDD_GPIORET_V3V is typically disabled.
- 5) DDR Retention (aka DDR_RET_Support-to-RAM_S2R) low power mode requires:
 - A) PMIC PN to assign GPIO_6 = Regulator Enable (REG_ON) as open-drain output buffer type per NVM default settings. The board level net H_DDR_RET_V3V signal is pulled up to VDD_DDR_V1B & V1B is connected to SoC's DDR_RET input. When this signal is set high, SoC's EMF-IO buffers are set to high-Z state & out of entering DDR_RET mode.
 - B) SoC SW executes command sequence that sets key PMIC register bits in order to enter DDR_RET low power mode of operation and select the desired wake-up destination state (i.e. Full Active or MCU Only).
 - C) After entering DDR_RET mode, the following power rails will remain energized & all other SoC MCU & Main supplies will be shut off to minimize power:
 1. VDD_DDR_V1B supplying both SoC EMF & SDRAM IO voltages.
 2. VDD1_DDR_V1B supplying SDRAM only.
 - D) PDN system exits DDR_RET upon detecting a CAN_WARE signal edge toggle on PMIC's GPIO_4 = LP_WKUP1 function per NVM settings that initiates exiting DDR_RET mode & restores full Active operation.
- 6) SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EPUS programming is needed. If customer desires capability for in-the-field updates, then on-board EPUS programming will require an additional 1.8V, 150mA LDO. When disabled, this LDO's Vn will need a high impedance output. Recommended PNs: TPS73101-EP, Texas 1.8V TPS73101-01 or TLV70018-Q1. The EN_EPUS_VPP control signal must be sourced from a SoC GPIO for this PDN (due to limited number of PMIC GPIOs). This allows SoC SW to control EPUS VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC fuses (see SoC DM for details).
- 7) PDN shows SoC's VDDA_3P3_USB domain supplied from a low noise LDO with a VSYS_V3V input as preferred for optimal USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_V3V rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_V3V rail to support USB 2.0 I/F requires a discrete LDO & VSYS_V3V input but could negatively impact data eye performance due to higher supply noise causing data eye mask violations.
- 8) PDN shows SoC's Main domain's VDDSHVS supply being sourced from a dual voltage LDO with a VSYS_V3V input as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_V3V rail with in-line supply filter can be used as an alternate supply. Using digital VDD_IO_V3V rail to support SD Card operation removes dual voltage, discrete LDO & VSYS_V3V input but will restrict data rates to standard 12MB/s with VIO = 3.3V.
- 9) A discrete FET with low VDS (EVM uses industrial temp grade FET for low VDS) or single channel, voltage translation IC (automotive Q1 grade) can support low VDS needed to ensure a logic high level output will result with an input min 0.7V (5% supply tol). If using SN74AC125-Q1, please add a discrete FETs for an open-drain interface needed to interface with "MAIN_PWRGRP_IRQn" net.

Examples shown below:

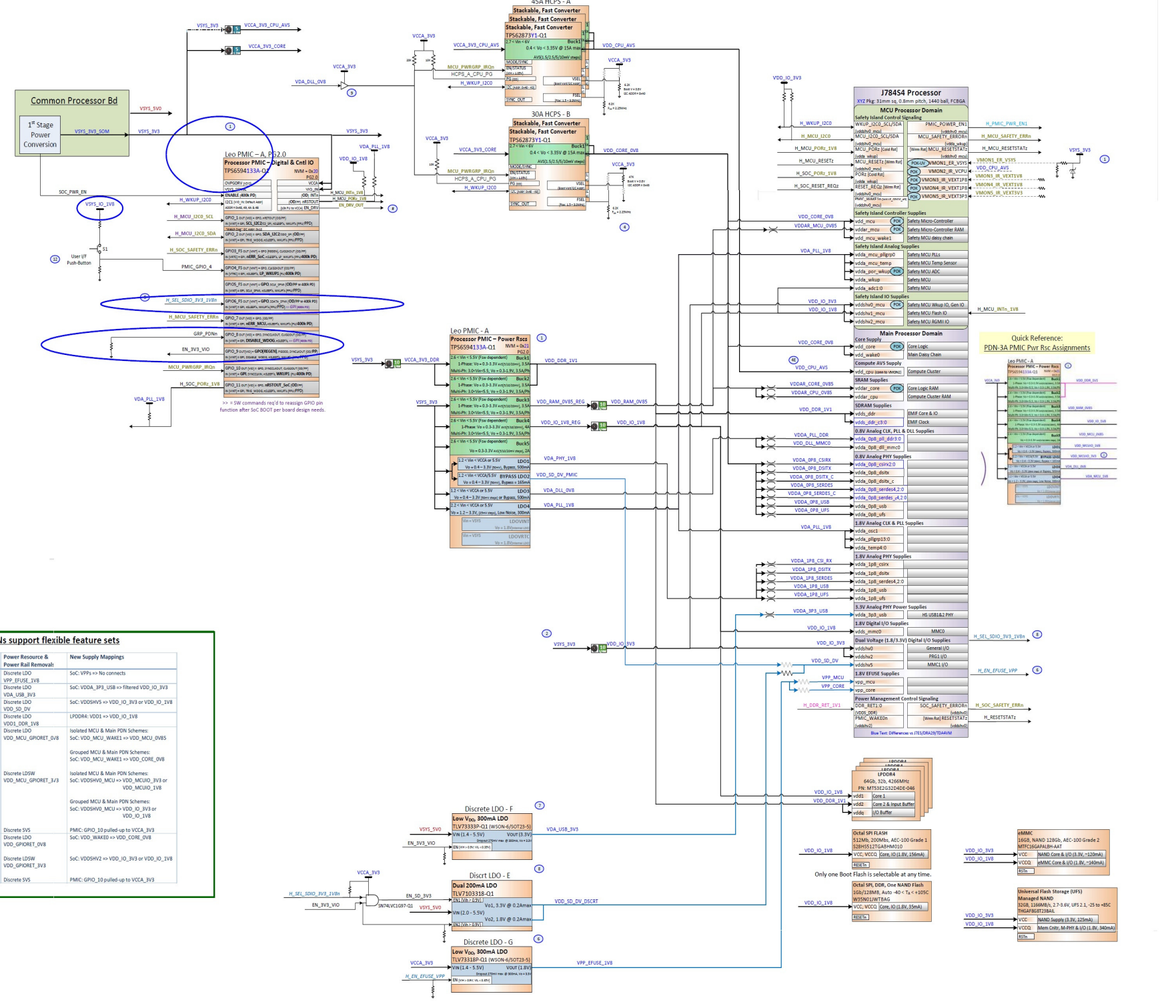
EVM Discrete FETs w/ low Vds

Auto Q1, Single Ch. Voltage Translator w/ FETs for open-drain interface
- 10) Worst case analysis for very high thermal use cases could result in VCCA_V3V load current in 15-18A range. This large load current range could lead to a 60-72mV voltage drop across Safety FET (EVM's PNM NVM5K02BN) for a max RDS(on) = 4mOhm. The TPS22965-Q1 load switches have max RDS(on) = 27mOhm with 4A max rating resulting in additional max drop of 108mV. SoC's 3.3V supply tolerance is +/-5% or 165mV. Total RDS(on) drops across Safety FET & Load Switches range from 168-180mV which exceed SoC's min voltage limit. For this reason, the Tulp buck input voltage will be moved from VCCA_V3V to VSYS_V3V since VDD_CPU_AVS & VDD_CORE_OVB rails account for more than 70% of VCCA_V3V worst case load currents.
- 11) On "Vn" or "control" "output" "Vn" to existing MCU supplies sourced from PMIC to enable 1x common PN for SVS-A & -B while avoiding false positives on "unconnected" VMONn.
- 12) An optional "User I/F Push-Button" can be connected to PMIC_GPIO_4 since a PMIC wake-up function & signal is not needed due to removal of all low power mode features. SW must write to PMIC to reassign GPIO_4's function to a GPI if this optional User I/F signal is desired.

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. a. Not a Functional Safety capable sys
- b. Grouped Main & MCU power rails (no supply FFI)
3. 4x SDRAMs: 32Gb, 4-Die, 32b, 426MT/s, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or HyperFlash & eMMC, UFS
5. Signaling Levels: MCU & Main Dual VIO

7. End Product Options:
 - a. Compliant high-speed SD Card (needs 1 indep pwr rail & 1 VIO ctrl signal & discrete LDO needs Vn = Sv)
 - b. Compliant USB 2.0 data eye (needs Sv, 1 indep pwr rail & discrete LDO needs Vn = Sv)
 - c. HS SoC Fuse programming on-board (needs 1 indep pwr rail & 1 ctrl signal)



Project : AM69 Edge AI Kit

TEXAS INSTRUMENTS

Title : SoC EVM PMIC PDN-0.6

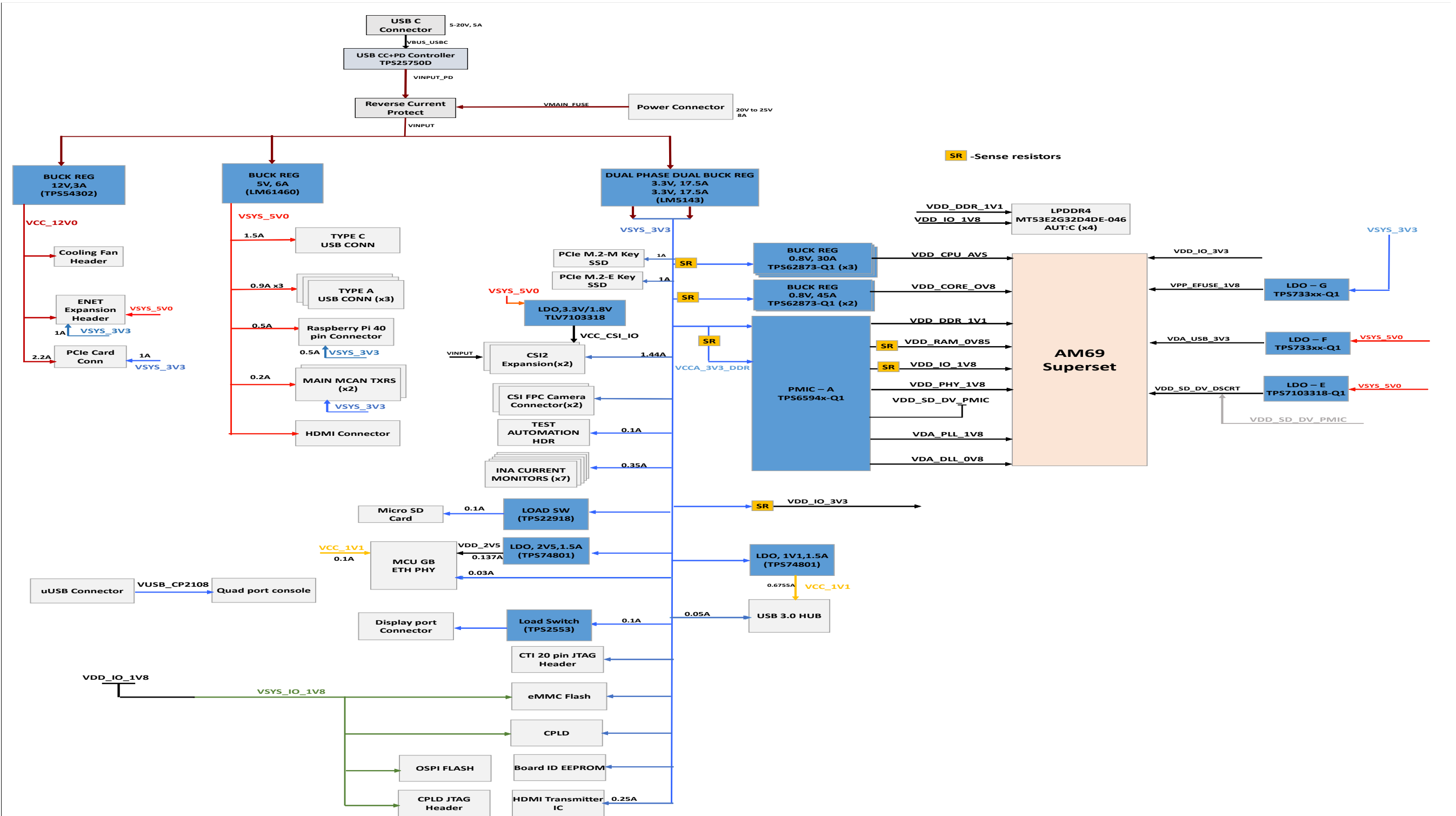
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Date : Monday, March 20, 2023

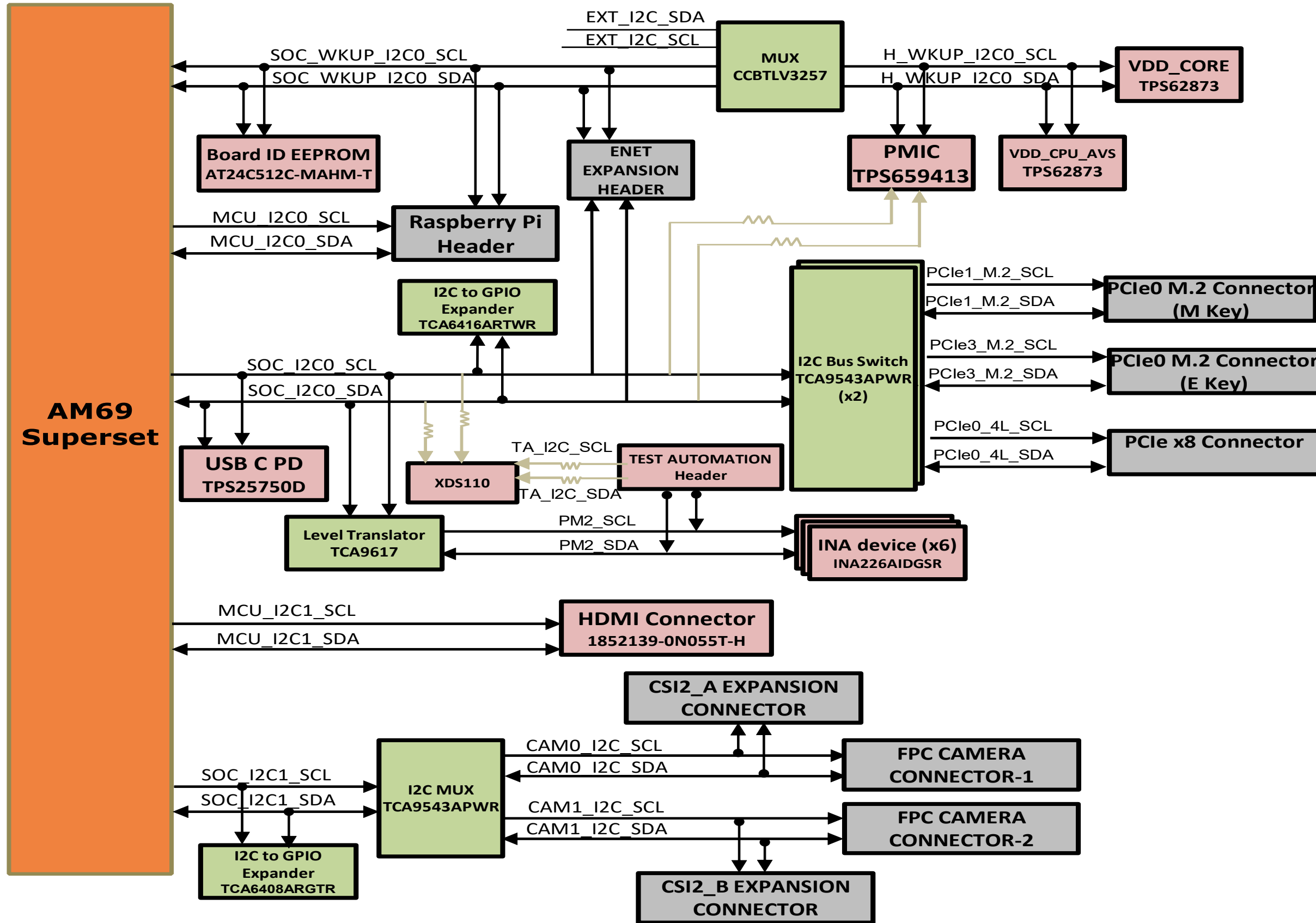
Rev : E3

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AM69 SK POWER FLOW DIAGRAM



I2C TREE



I2C TABLE

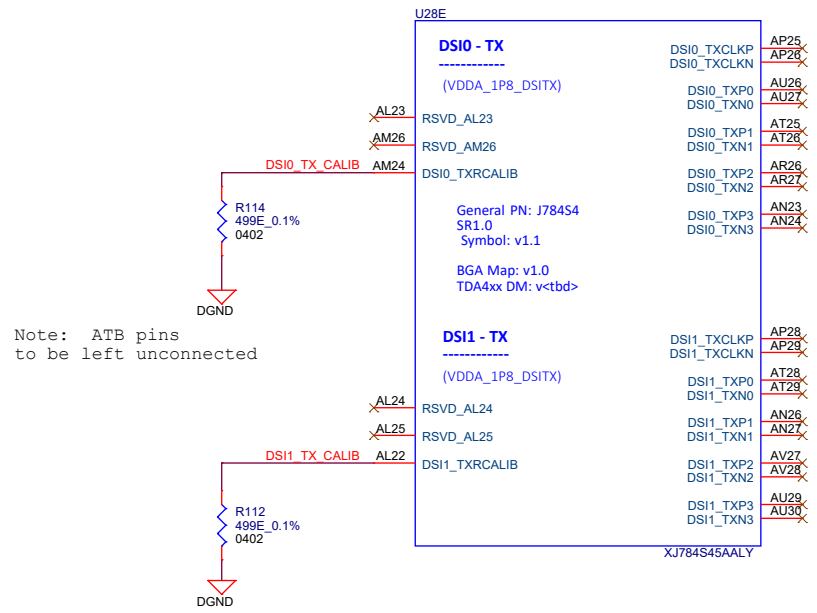
AM69 SK I2C Slave Address Table			
SOC I2C Port	Device Description	Part#	I2C Address
WKUP_I2C0	PMIC	TPS6594133ARWERQ1	0x48, 0x49, 0x4A & 0x4B
	VDD_CPU_AVS High-Current Power Stage A	TPS62873Y1QWRXSRQ1	0x40
	VDD_CORE_OV8 High-Current Power Stage B	TPS62873Y1QWRXSRQ1	0x43
	Raspberry Pi Header	61304021121	
	Board ID EEPROM	AT24C512C-MAHM-T	0x51
	ENET Expansion Header	171446-1109	0x57
MCU_I2C0	Raspberry Pi Header	61304021121	
MAIN_I2C0	Test Automation Header	687140183622	
	INA226 device for VCCA_3V3_CORE	INA226AIDGSR	0x45
	INA226 device for VCCA_3V3_CPU_AVS	INA226AIDGSR	0x4F
	INA226 device for VCCA_3V3_DDR	INA226AIDGSR	0x4D
	INA226 device for VDD_RAM_OV85	INA226AIDGSR	0x46
	INA226 device for VDD_IO_3V3	INA226AIDGSR	0x41
	INA226 device for VDD_IO_1V8	INA226AIDGSR	0x40
	PCIe_M.2_Interface M Key	MDT320M01001	
	PCIe_M.2_Interface E Key	MDT320E01001	
	Ext Power Measurement Header	61300311121	
	PCIe Card Slot	10018783-10202TLF	
	USB C PD Controller	TPS25750D	0x20
	Level Translator-1	TCA9543APWR	0x71
	Level Translator-2	TCA9543APWR	0x72
	GPIO Expander	TCA6416ARTWR	0x21
	PMIC	TPS6594133ARWERQ1	
	ENET Expansion Header	171446-1109	0x77
	MCU_I2C1	HDMI Connector	1852139-0N055T-H
MAIN_I2C1	FPC Camera Connector 1	52435-2271	
	FPC Camera Connector 2	52435-2271	
	CSI2_A Expansion Connector	QSH-020-01-L-D-DP-A-K	
	CSI2_B Expansion Connector	QSH-020-01-L-D-DP-A-K	
	GPIO Expander	TCA6408ARGTR	0x21
	Level Translator	TCA9543APWR	0x70

GPIO MAPPING TABLE

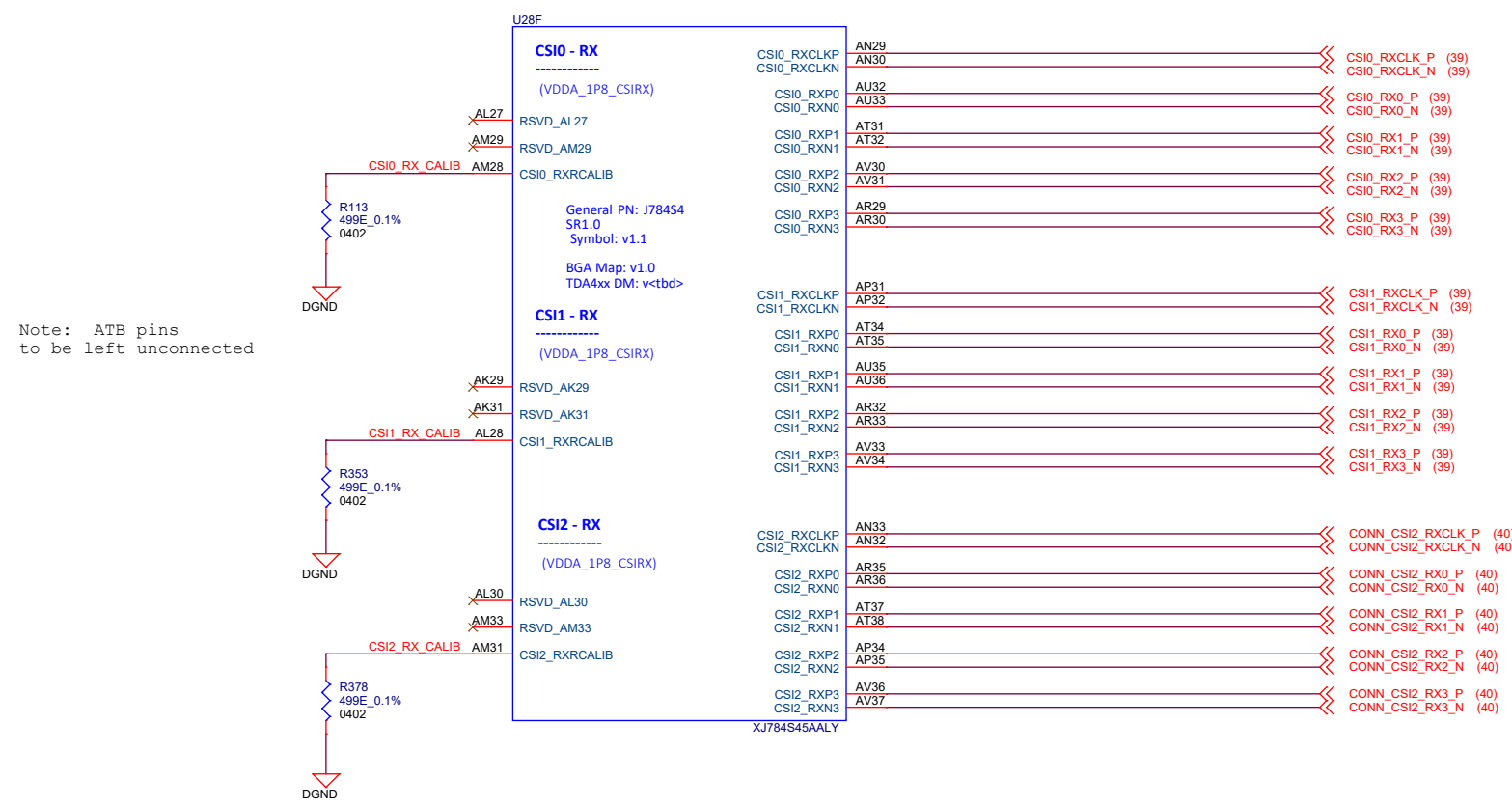
GPIO Mapping						
J7AHP Mapping		WKUP Domain				
Package Signal Name	GPIO	Net Name	Input/Output	Default	State	Usage
MCU_OSPiO_CSn1	WKUP_GPIO0_28	EN_EFUSE_VPP	O	PD	Active High	Enable for VPP_EFUSE_1V8 LDO
MCU_OSPiO_CSn2	WKUP_GPIO0_29	CPLD_TMS/CSiB_EXP_GPIO1	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_CLK	WKUP_GPIO0_31	CPLD_TCK/CSiB_EXP_GPIO2	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_LBCLKO	WKUP_GPIO0_32	CSi_EXP_GPIO_1	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_DQ5	WKUP_GPIO0_33	CPLD_TDO/CSiB_EXP_GPIO3	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_D0	WKUP_GPIO0_34	CPLD_TDI/CSiB_EXP_GPIO4	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_D1	WKUP_GPIO0_35	CSi_EXP_GPIO_5	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_D2	WKUP_GPIO0_36	CSi_EXP_GPIO_2	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_D3	WKUP_GPIO0_37	CSi_EXP_GPIO_3	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_CSn0	WKUP_GPIO0_38	CSi_EXP_GPIO_4	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_OSPi1_CSn1	WKUP_GPIO0_39	CSiB_EXP_GPIO5	IO	NA	NA	GPIO signal for CSi2 EXPANSION Connector
MCU_SPiO_CLK	WKUP_GPIO0_54	WKUP_GPIO0_54	O	Bootmode	Active High	Select line for CPLD's Mux
MCU_SPiO_D0	WKUP_GPIO0_55	USER_LED1	O	Bootmode	Active High	User LED
MCU_SPiO_D1	WKUP_GPIO0_69	SYS_MCU_PWRDN	O	Bootmode	Active High	System Power Down ('0' - normal operation '1' - system power down)
MCU_SPiO_CS0	WKUP_GPIO0_70	WKUP_GPIO0_70	IO	NA	NA	GPIO signal for FPC camera Connector
WKUP_GPIO0_10	WKUP_GPIO0_10	HDMI_LS_OE	O	PU	Active High	Level Shifter Output Enable for HDMI
WKUP_GPIO0_14	WKUP_GPIO0_14	HDMI_PDN	O	Bootmode	Active Low	Power Down Signal for HDMI
WKUP_GPIO0_49	WKUP_GPIO0_49	WKUP_GPIO0_49	IO	NA	NA	GPIO signal for 40 pin Expansion Header
PMIC_POWER_EN1	WKUP_GPIO0_88	WKUP_GPIO0_88	IO	NA	NA	GPIO signal for FPC camera Connector
WKUP_GPIO0_56	WKUP_GPIO0_56	WKUP_GPIO0_56	IO	NA	NA	GPIO signal for 40 pin Expansion Header
WKUP_GPIO0_57	WKUP_GPIO0_57	WKUP_GPIO0_57	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCU_ADC1_AIN0	WKUP_GPIO0_79	SOC_INT1z	I	PU	Active Low	Test Automation INT signal
MCU_ADC1_AIN1	WKUP_GPIO0_80	SOC_INT2z	I	PU	Active Low	Test Automation INT signal
MCU_ADC1_AIN2	WKUP_GPIO0_81	MCU_RGMII_INT#	I	PU	Active Low	Interrupt Signal from RGMII
MCU_ADC1_AIN3	WKUP_GPIO0_82	SOC_WAKE	I	PU	Active High	SOC wake signal from Reset Button
MCU_ADC1_AIN4	WKUP_GPIO0_83	PMIC_INTn	I	PU	Active Low	PMIC interrupt signal
MCU_ADC1_AIN5	WKUP_GPIO0_84	ENET1_EXP_INTB	I	NA	NA	Interrupt Signal from ENET Expansion Header
MCU_ADC1_AIN6	WKUP_GPIO0_85	IO_EXP_I2CO_INTB	O	NA	NA	I2CO Interrupt Signal to ENET Expansion Header
WKUP_GPIO0_66	WKUP_GPIO0_66	WKUP_GPIO0_66	IO	PU	NA	GPIO signal for 40 pin Expansion Header
WKUP_GPIO0_67	WKUP_GPIO0_67	WKUP_GPIO0_67	IO	NA	NA	GPIO signal for 40 pin Expansion Header
Main Domain						
EXTINTn	GPIO0_0	HDMI_HPD	I	NA	Active High	HDMI hot plug detect signal
MCAN13_TX	GPIO0_3	GPIO0_3	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCAN13_RX	GPIO0_4	DP0_3V3_EN	O	PD	Active High	Enable signal for Display port Current Limiter
MCAN1_TX	GPIO0_27	GPIO0_27	IO	NA	NA	GPIO signal for 40 pin Expansion Header
MCASPO_AXR8	GPIO0_36	GPIO0_36	IO	NA	NA	GPIO signal for 40 pin Expansion Header
ECAP0_IN_APWM_OUT	GPIO0_49	SEL_SDiO_3V3_1V8n	O	PU	Active Low	One of Enable signal for VDD_SD_DV
GPIO Expander						
Port No	GPIO	I2C	Input/Output	Default	State	Usage
P0	CSi_ViO_SEL	MAIN_I2C1 Address : 0x21 Part No - TCA6408ARGTR	O	PD	Active High	Enable signal for Camera IO supply
P1	CSi_MUX_SEL_2		O	PD	Active High	Select lines for CSi mux
P2	CSi2_RSTz		O	PD	Active Low	Reset signal for CSi Expansion Connector
P3	IO_EXP_CAM0_GPIO1		IO	NA	NA	GPIO signals for FPC Camera Connector
P4	IO_EXP_CAM1_GPIO1	IO	NA	NA	GPIO signals for FPC Camera Connector	
P00	BOARDID_EEPROM_WP	MAIN_I2C0 Address : 0x21 Part No - TCA6416ARTWR	O	PD	Active High	Board ID EEPROM Write Protect
P01	CAN_STB		O	PD	Active High	Stand By Input for CAN Transceiver
P02	GPIO_uSD_PWR_EN		O	PU	Active High	One of Enable signal for Micro SD Load Switch
P03	IO_EXP_MCU_RGMII_RST#		O	NA	Active Low	MCU_RGMII Resetz signal to CPLD
P04	IO_EXP_PClE0_4L_PERST#		O	NA	Active Low	PClE 4 lane Resetz signal to CPLD
P05	IO_EXP_PClE1_M.2_RTsz		O	NA	Active Low	PClE M Key Resetz signal to CPLD
P06	IO_EXP_PClE3_M.2_RTsz		O	NA	Active Low	PClE E Key Resetz signal to CPLD
P07	PM_INA_BUS_EN		O	PU	Active High	Enable signal for PM2 I2C lines
P10	ENET1_EXP_PWRDN		O	PU	Active High	Power Down Signal for Enet Expansion Header
P11	EXP1_ENET_RSTz		O	NA	Active Low	Reset Signal for Enet Expansion Header
P12	ENET1_I2CMUX_SEL		O	NA	Active High	I2C mux select Signal for Enet Expansion Header
P13	PClE0_CLKREQ#		I	PU	Active Low	PClE Card Clock request Signal
P14	PClE1_M.2_CLKREQ#		I	PU	Active Low	PClE M Key Clock request Signal
P15	PClE3_M2_CLKREQ#	I	PU	Active Low	PClE E Key Clock request Signal	
P16	CDCI1_OE2/OE3	IO	PU	NA	GPIO signal CDCI Clock Generator	
P17	CDCI1_OE1/OE4	IO	PU	NA	Output Enable for CDCI Clock Generator	
P0	SW_CPLD_CONTROL_IN1	TEST AUTOMATION I2C Address : 0x20 Part No - TCA6408ARGTR	O	NA	NA	CPLD Switch Control Signals for Bootmode Logic
P1	SW_CPLD_CONTROL_IN2		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic
P2	SW_CPLD_CONTROL_IN3		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic
P3	SW_CPLD_CONTROL_IN4		O	NA	NA	CPLD Switch Control Signals for Bootmode Logic

Project : AM69 Edge AI Kit	TEXAS INSTRUMENTS	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="2" style="text-align: right;">Title</td> <td colspan="2">SOC GPIO_MAPPING_TABLE</td> </tr> <tr> <td style="font-size: 8px;">Size</td> <td style="font-size: 8px;">C</td> <td style="font-size: 8px;">Rev</td> <td style="font-size: 8px;">E3</td> </tr> <tr> <td style="font-size: 8px;">Date:</td> <td style="font-size: 8px;">Monday, March 20, 2023</td> <td style="font-size: 8px;">Sheet</td> <td style="font-size: 8px;">8 of 62</td> </tr> </table>	Title		SOC GPIO_MAPPING_TABLE		Size	C	Rev	E3	Date:	Monday, March 20, 2023	Sheet	8 of 62
Title		SOC GPIO_MAPPING_TABLE												
Size	C	Rev	E3											
Date:	Monday, March 20, 2023	Sheet	8 of 62											

DSI

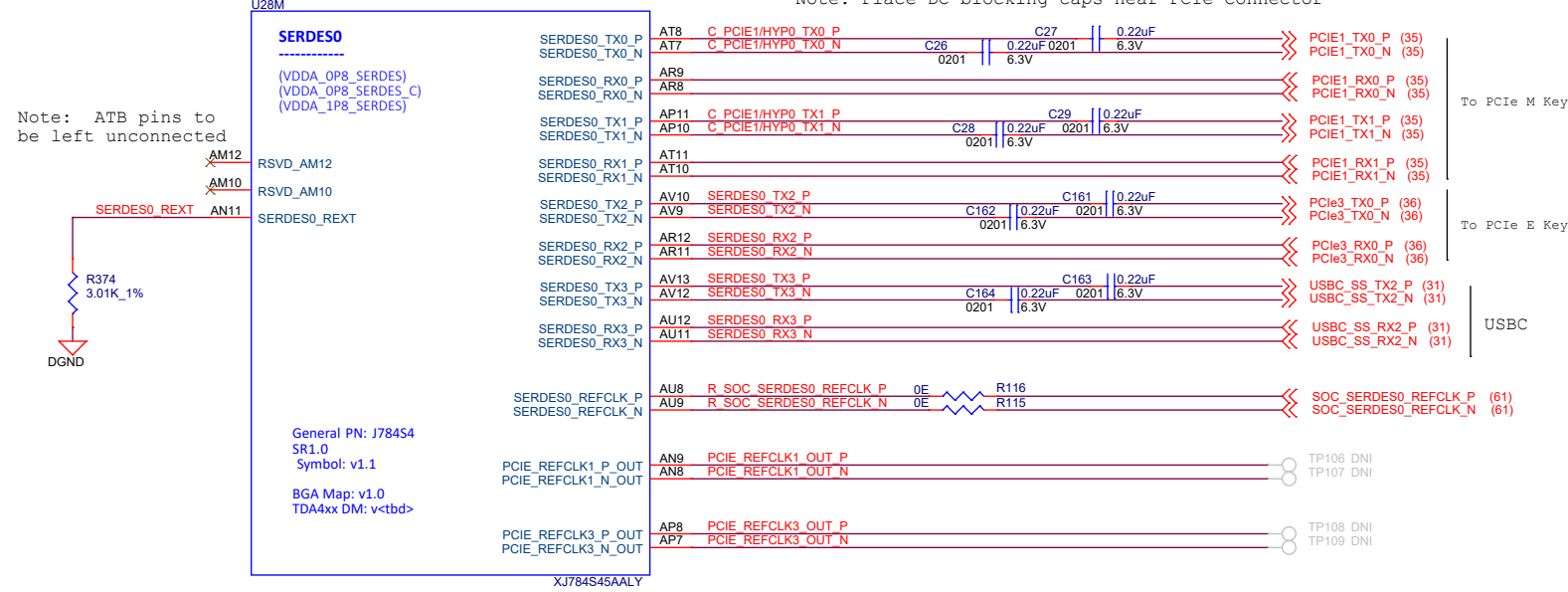


CSI

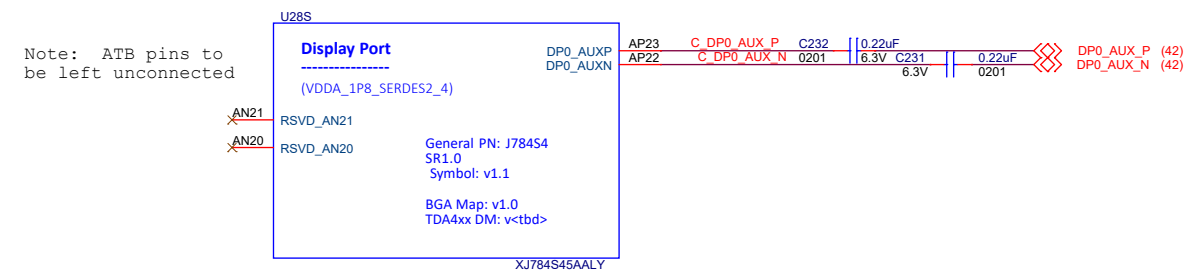


SERDES0

Note: Place DC blocking caps near PCIe Connector

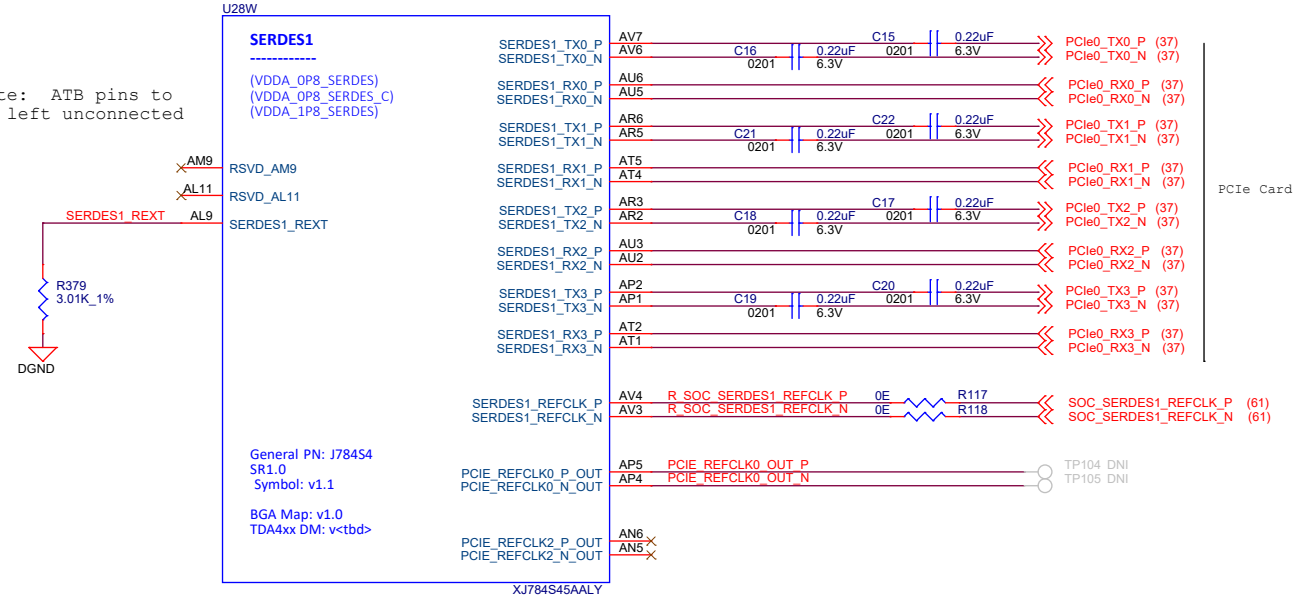


DP_AUX



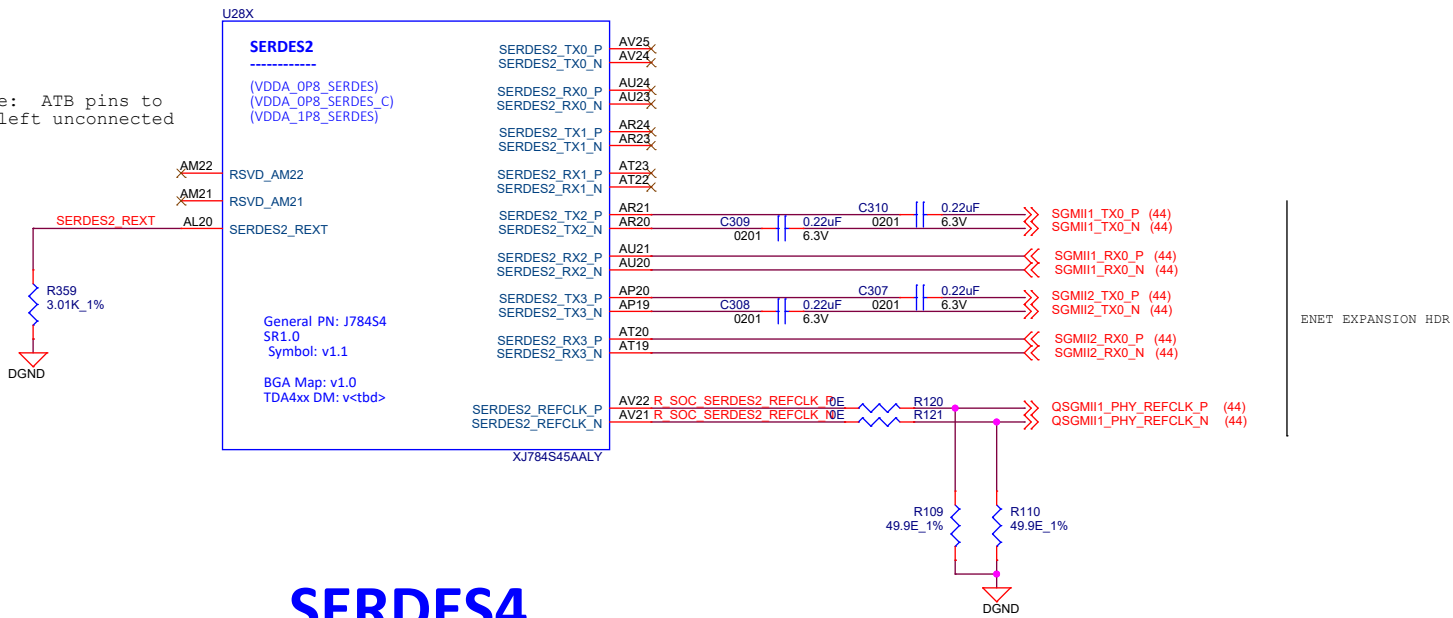
SERDES1

Note: ATB pins to be left unconnected



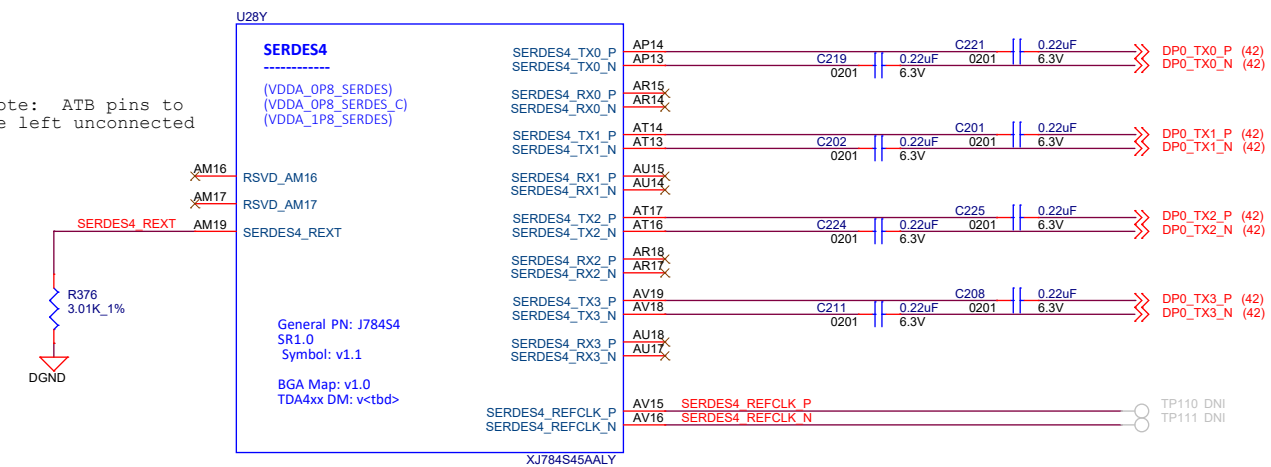
SERDES2

Note: ATB pins to be left unconnected



SERDES4

Note: ATB pins to be left unconnected



Project :
AM69 Edge AI Kit



Title SERDES INTERFACE-2

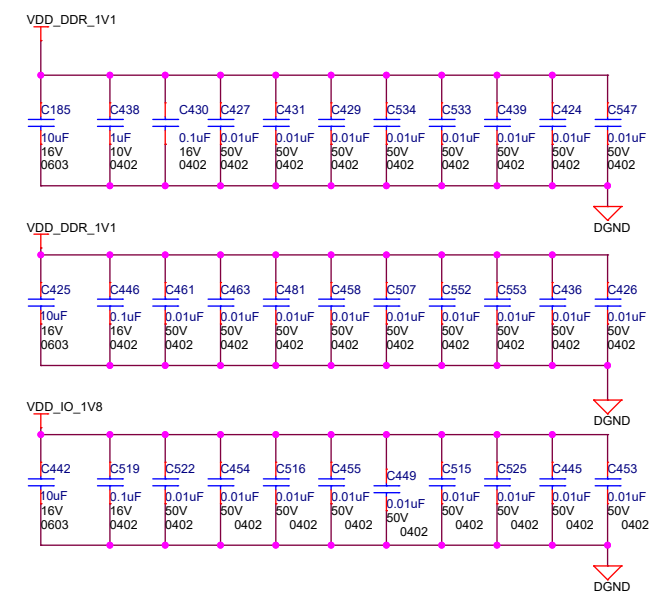
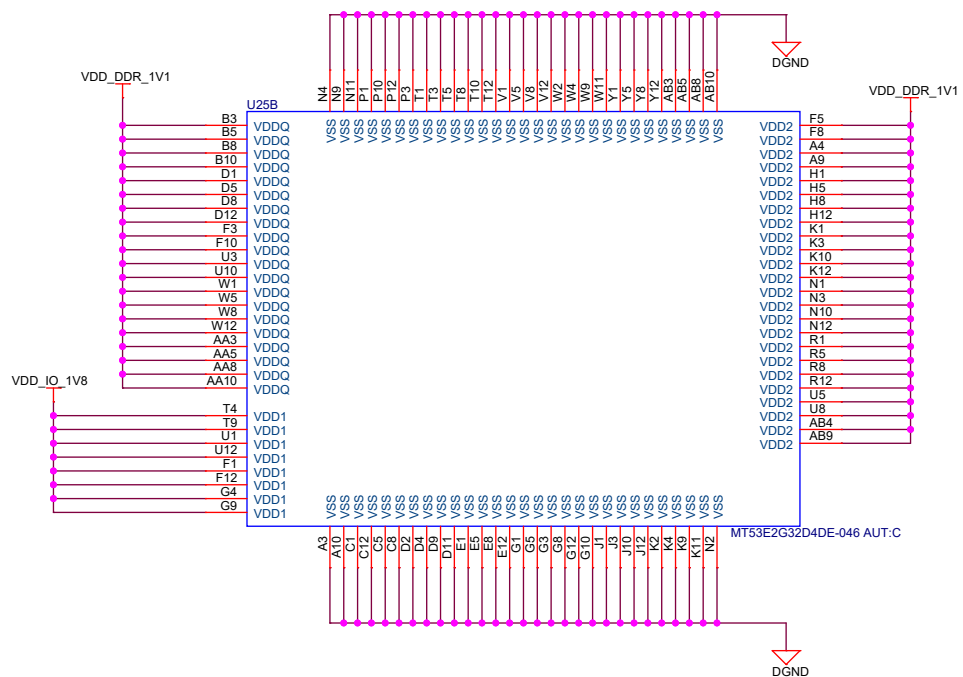
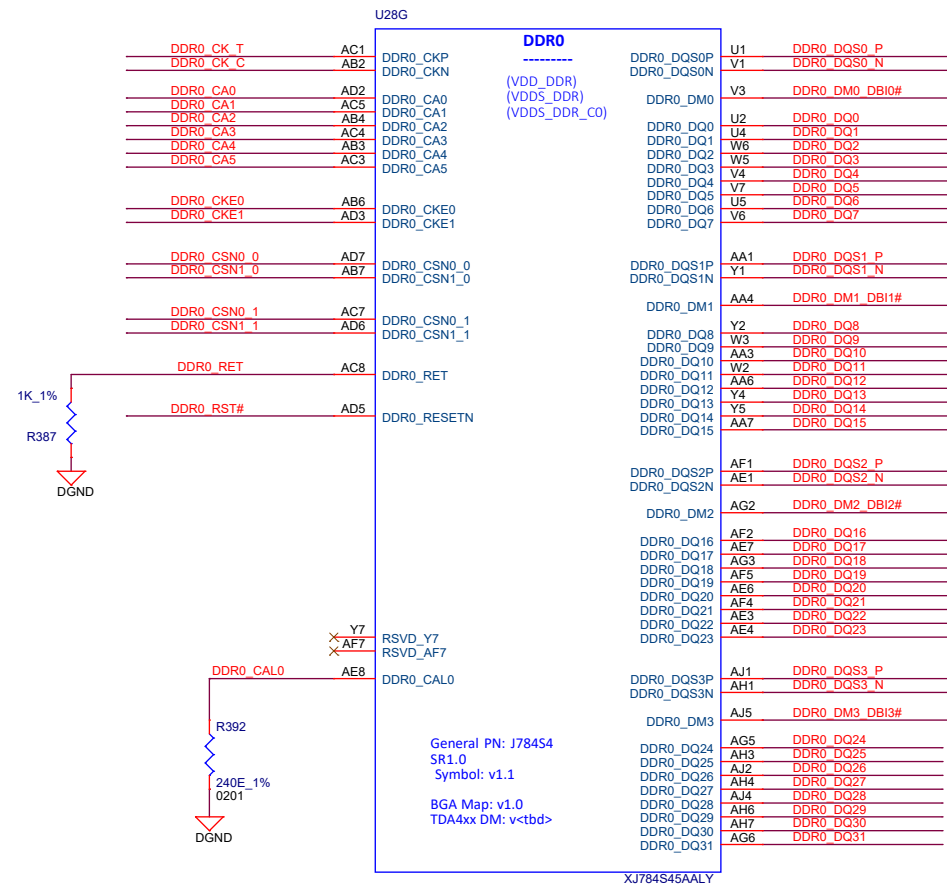
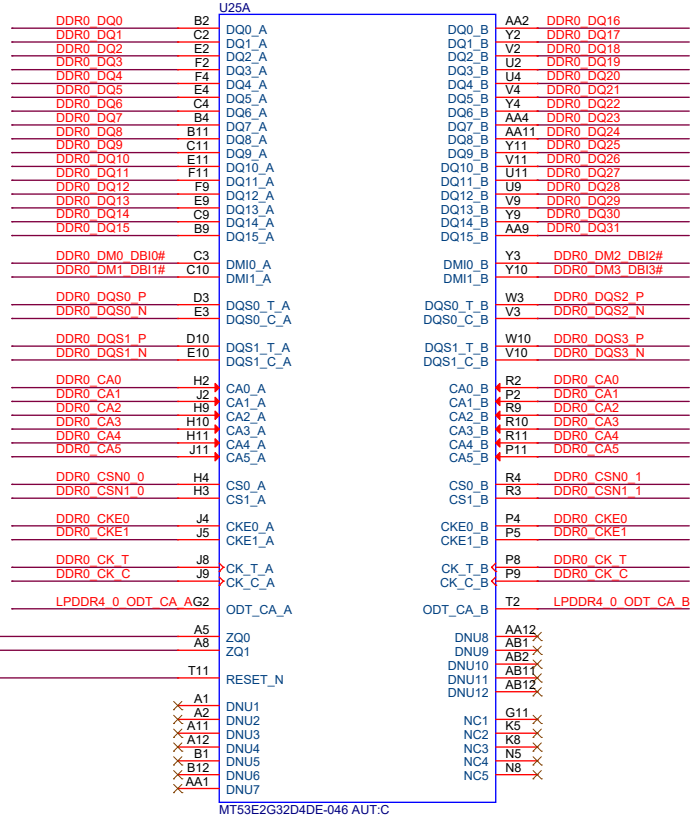
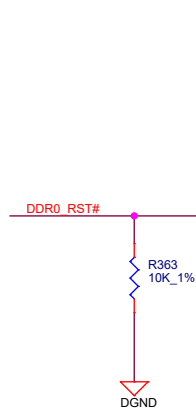
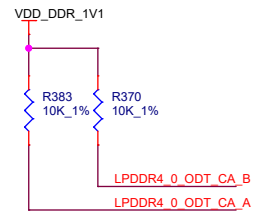
Size PROC154E3 001 SK AM69

Rev E3

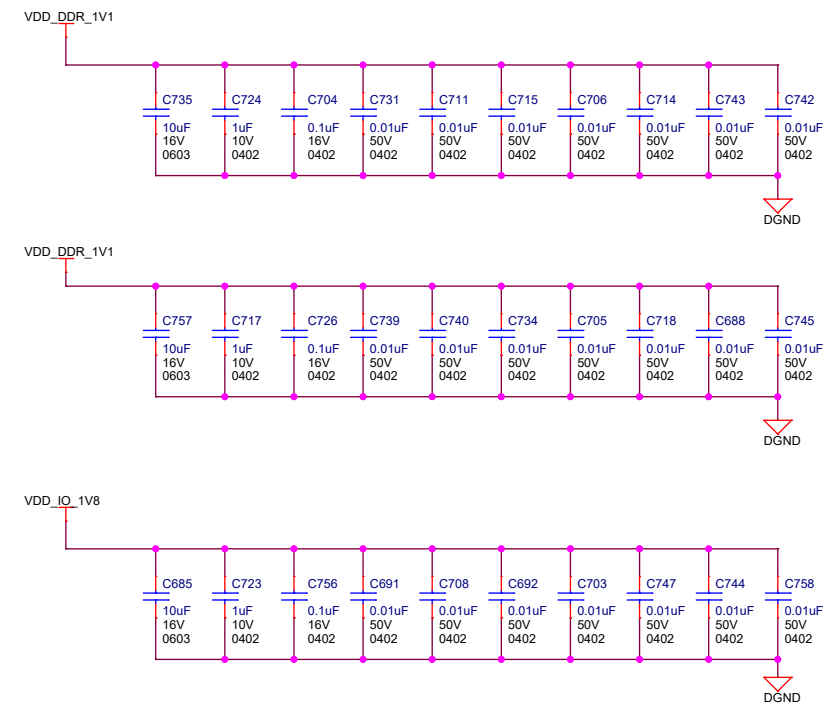
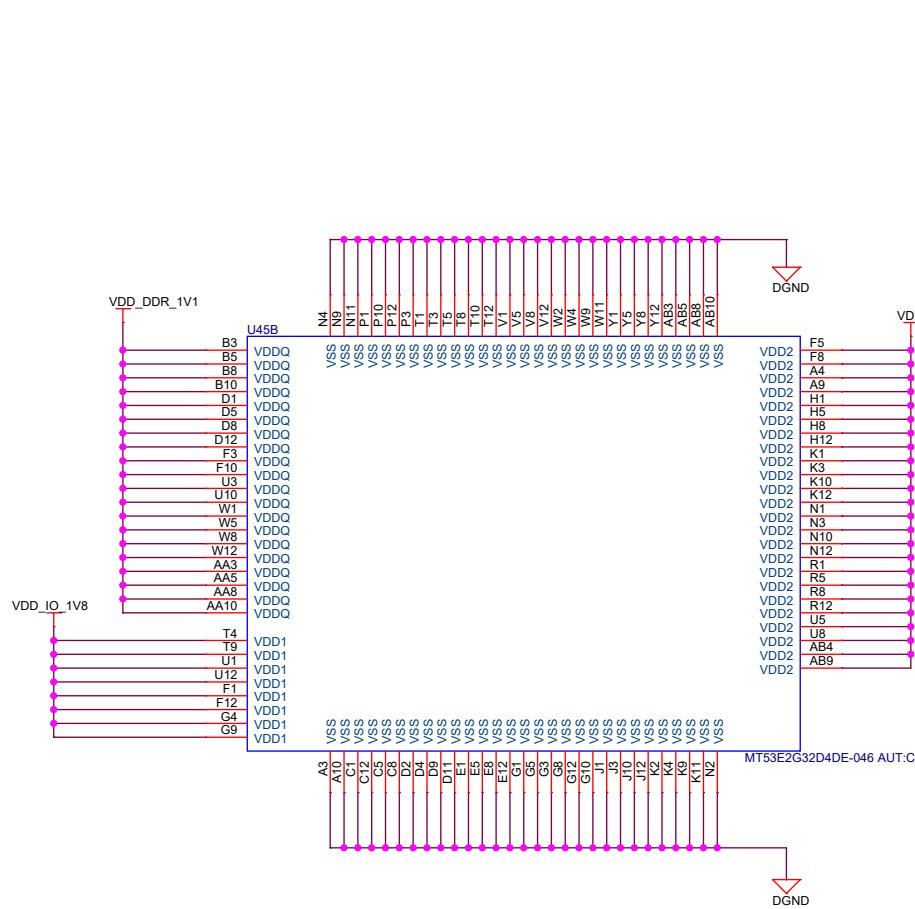
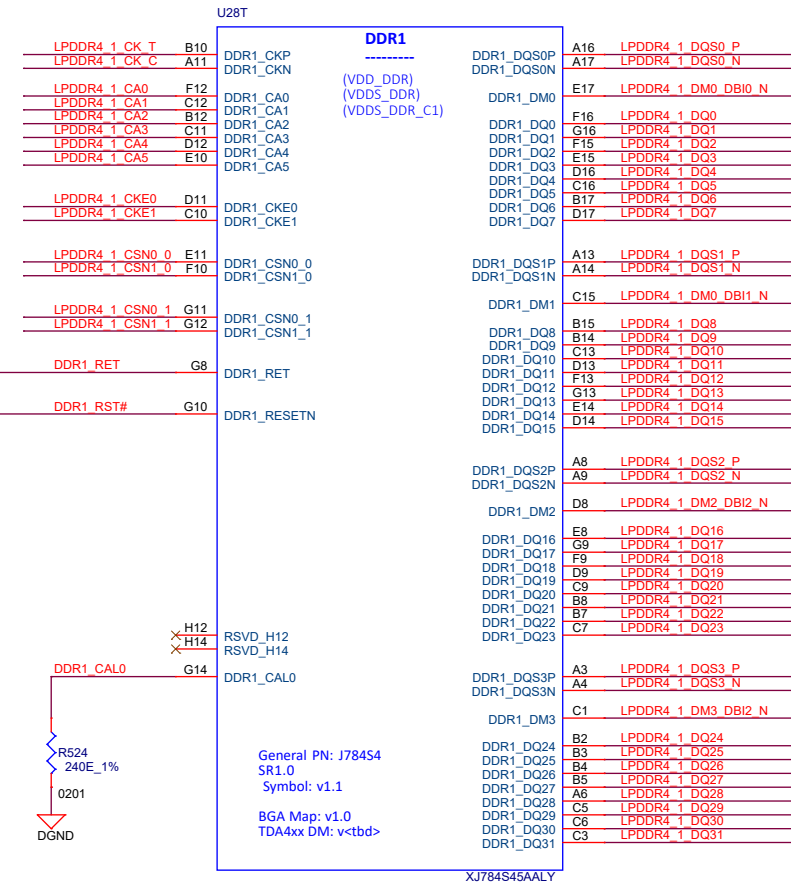
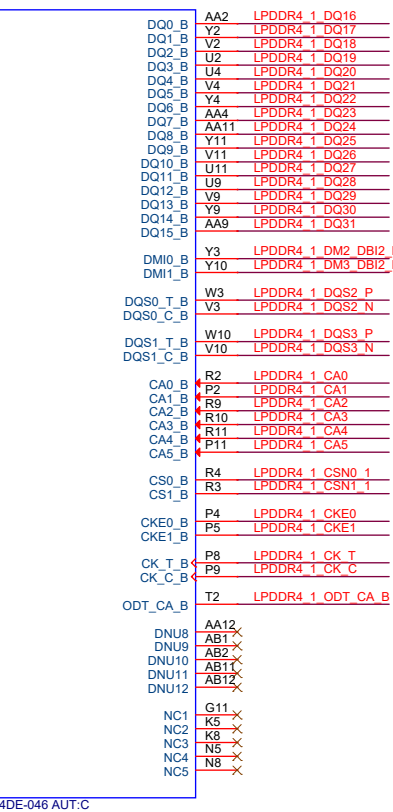
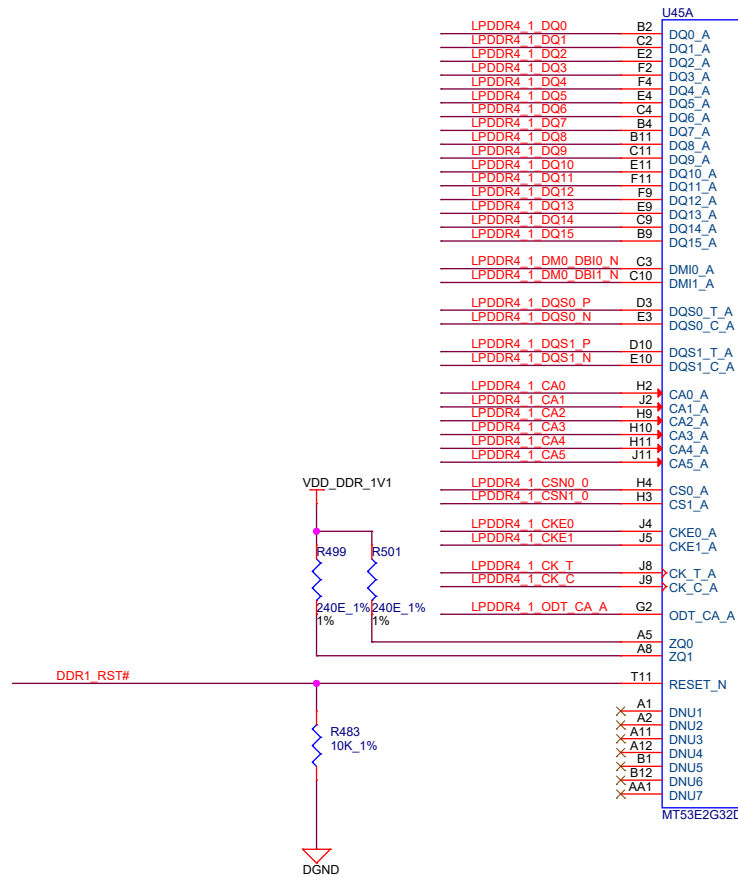
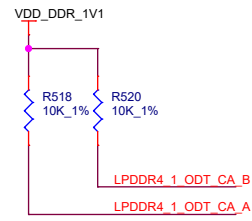
Date: Monday, March 20, 2023

Sheet 11 of 62

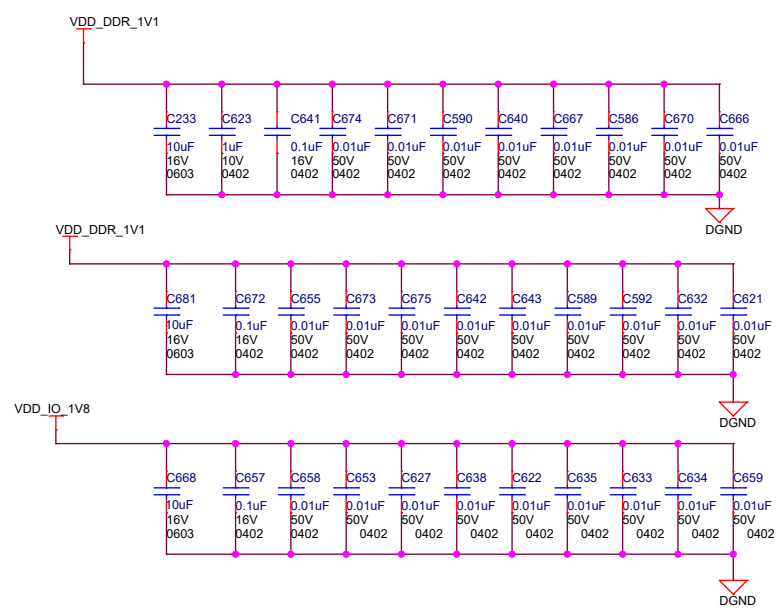
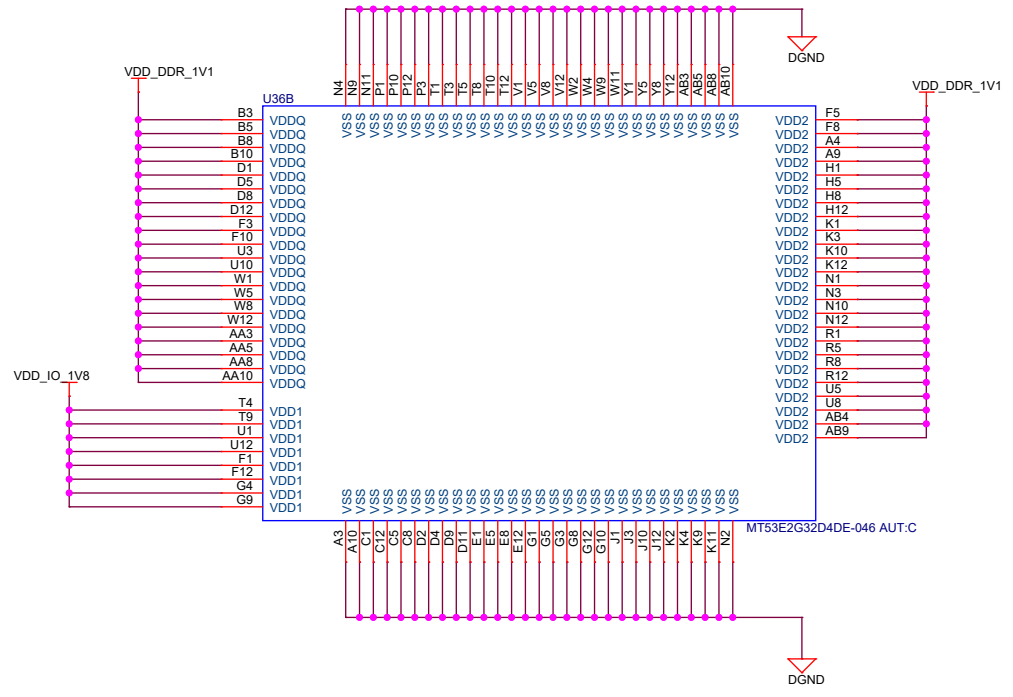
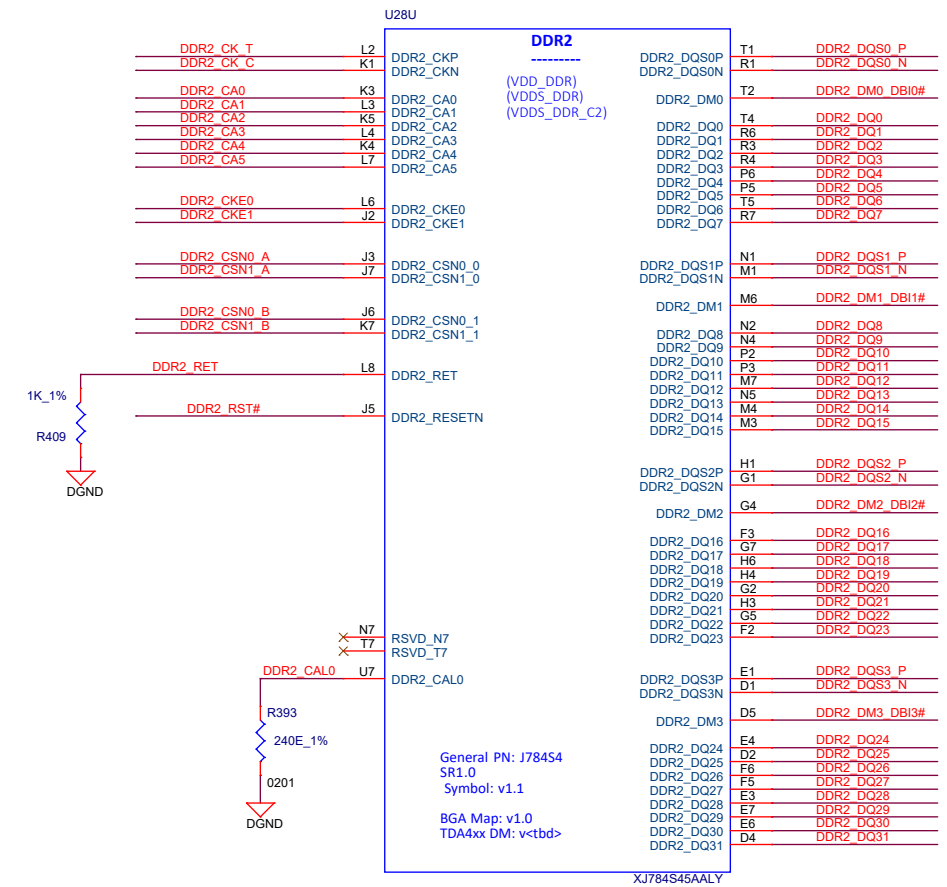
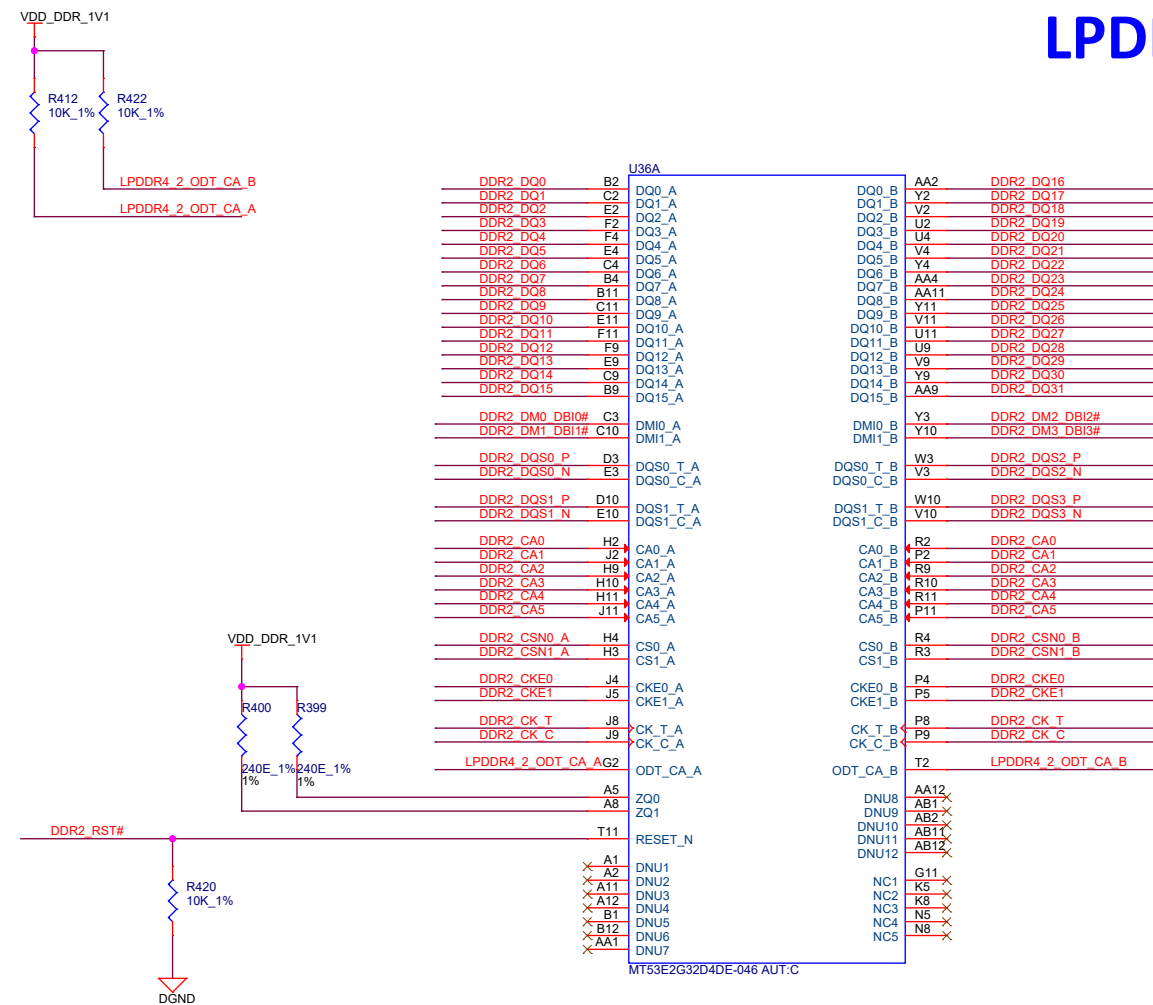
LPDDR4 - DDR0



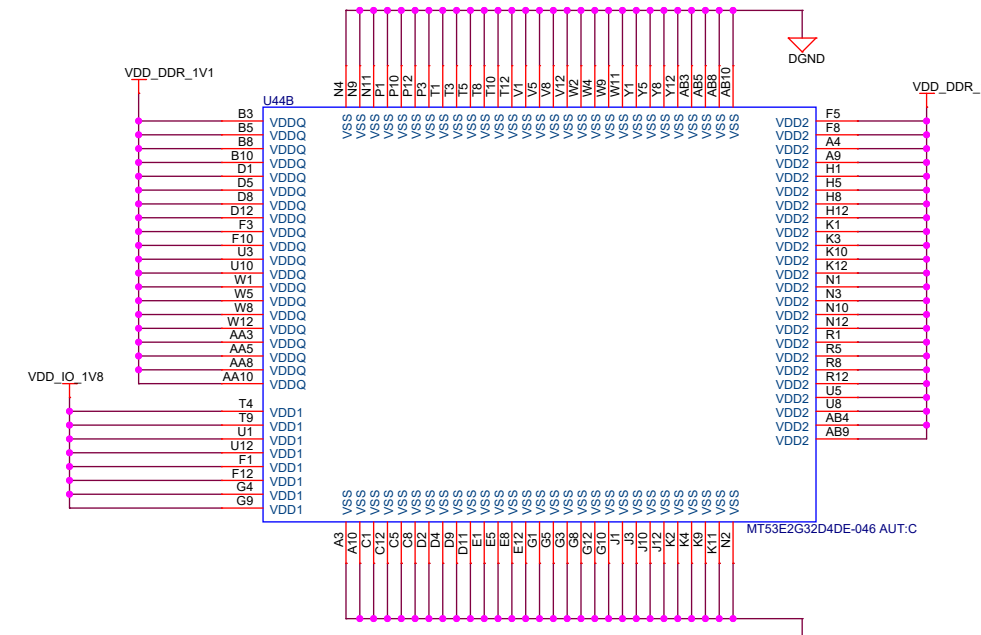
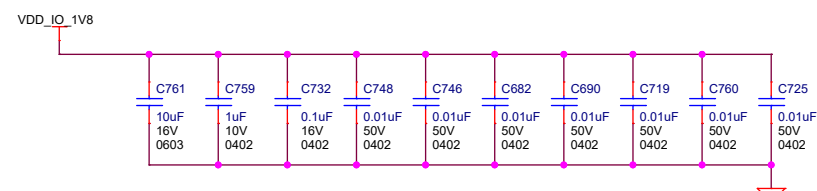
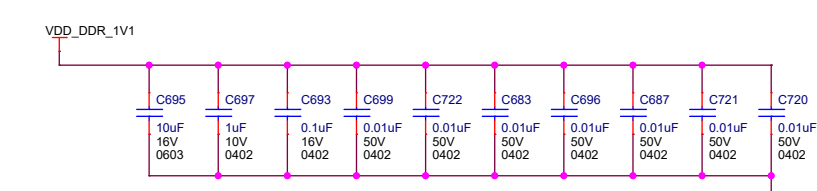
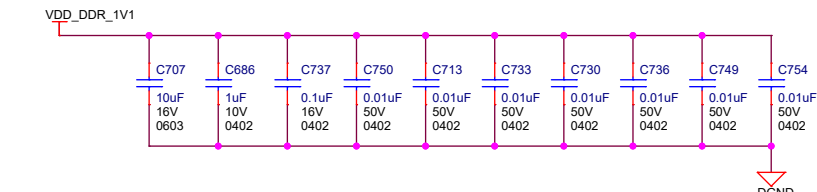
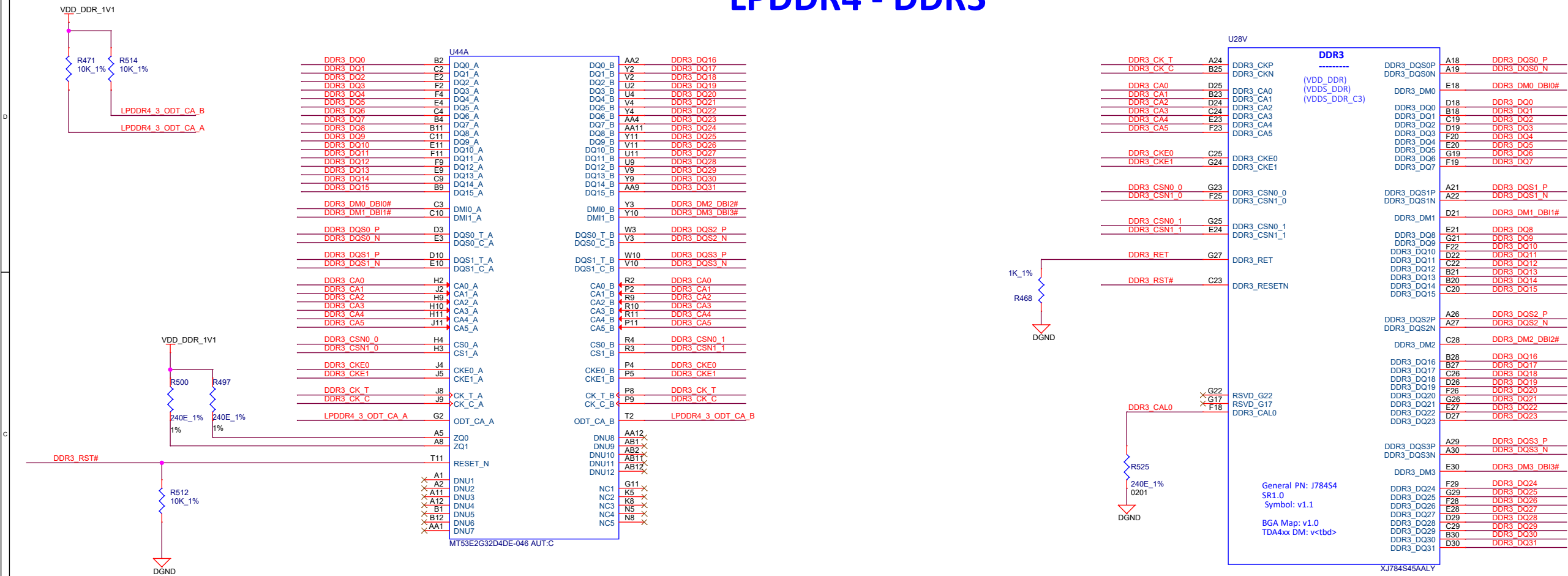
LPDDR4 - DDR1



LPDDR4 - DDR2

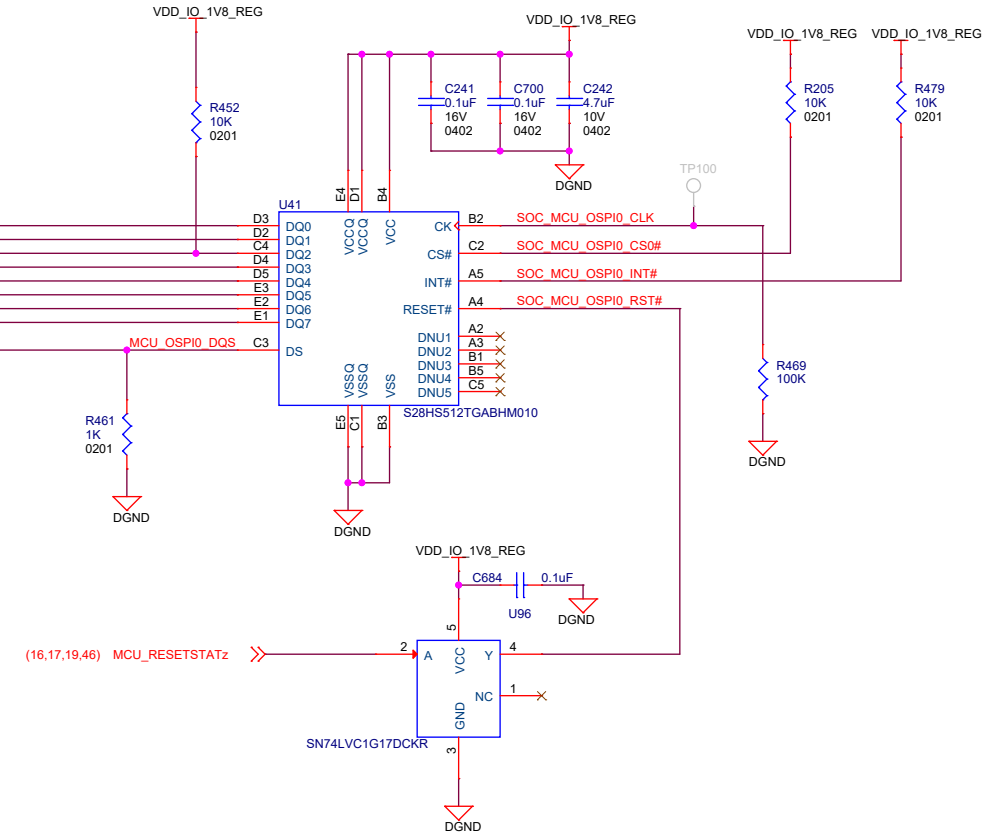
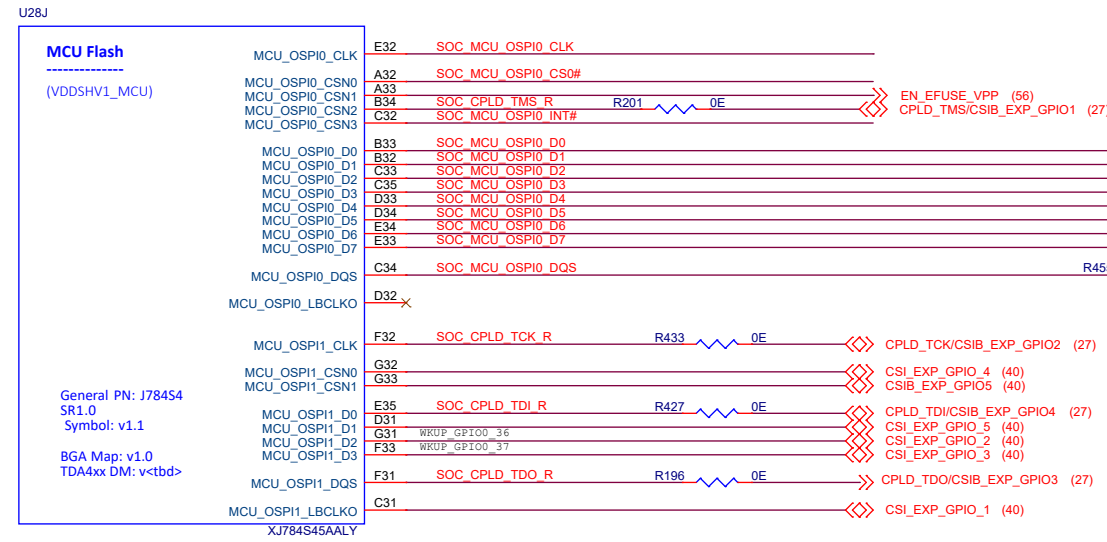


LPDDR4 - DDR3



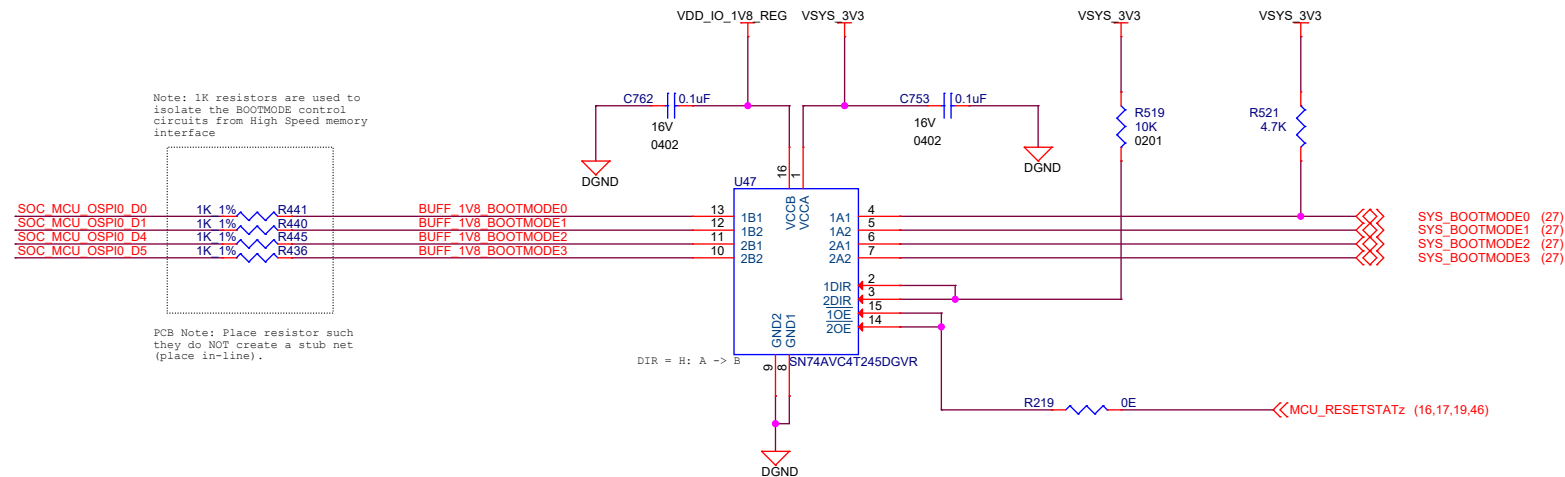
MCU FLASH

OSPI FLASH



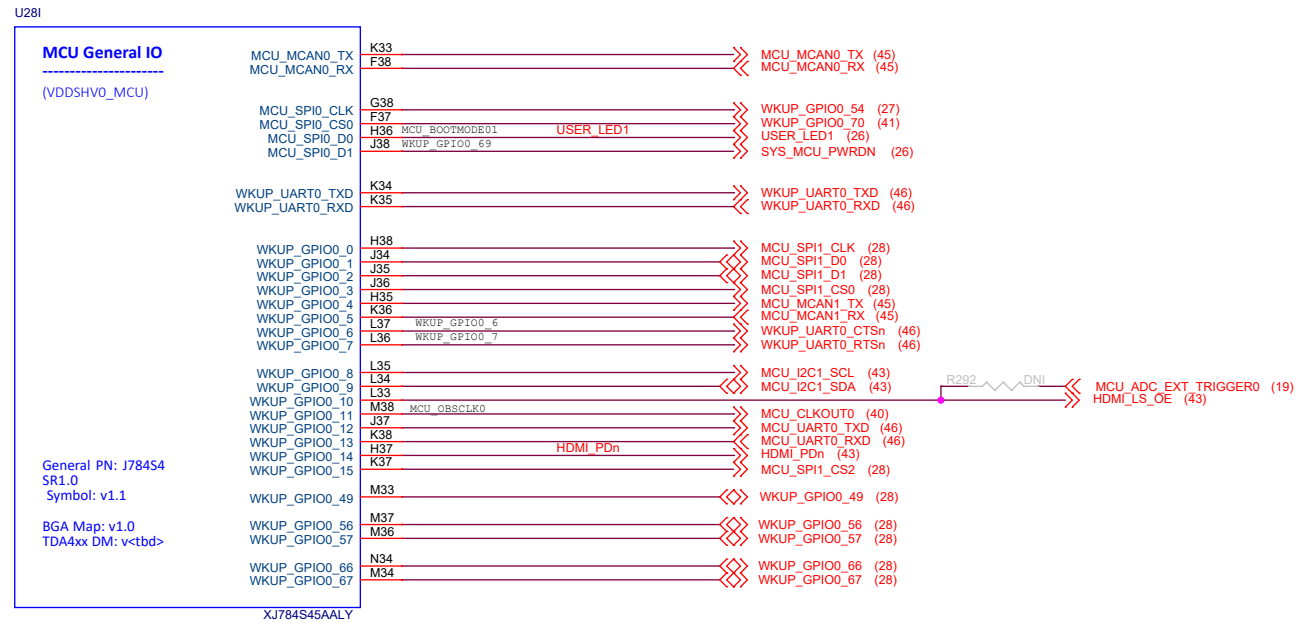
BOOTMODE Control Logic

Note: Logic used to configure BOOTMODE settings during reset. This is four (4) of a total of eighteen (18) boot pins. Specific value is user configured (dip switch).

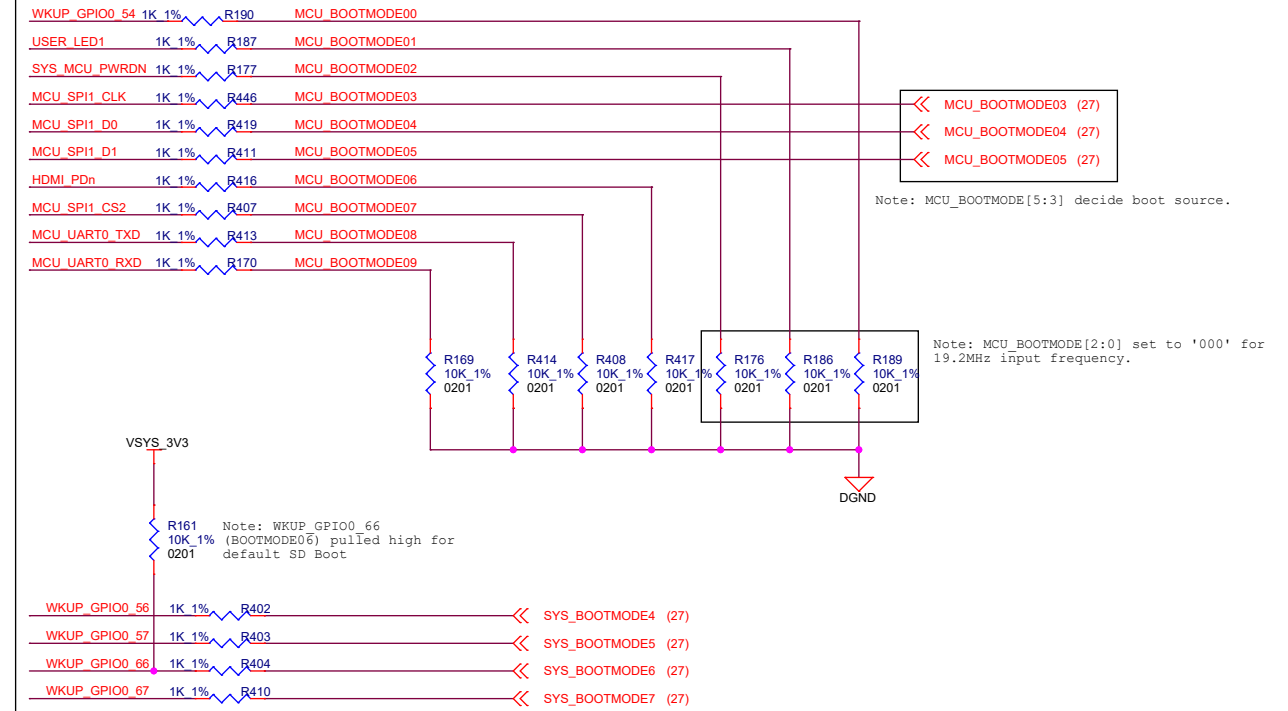


Project :		Title SOC - MCU OSPI FLASH	
AM69 Edge AI Kit		Size	Rev
		C	E3
		Date: Monday, March 20, 2023	Sheet 16 of 62

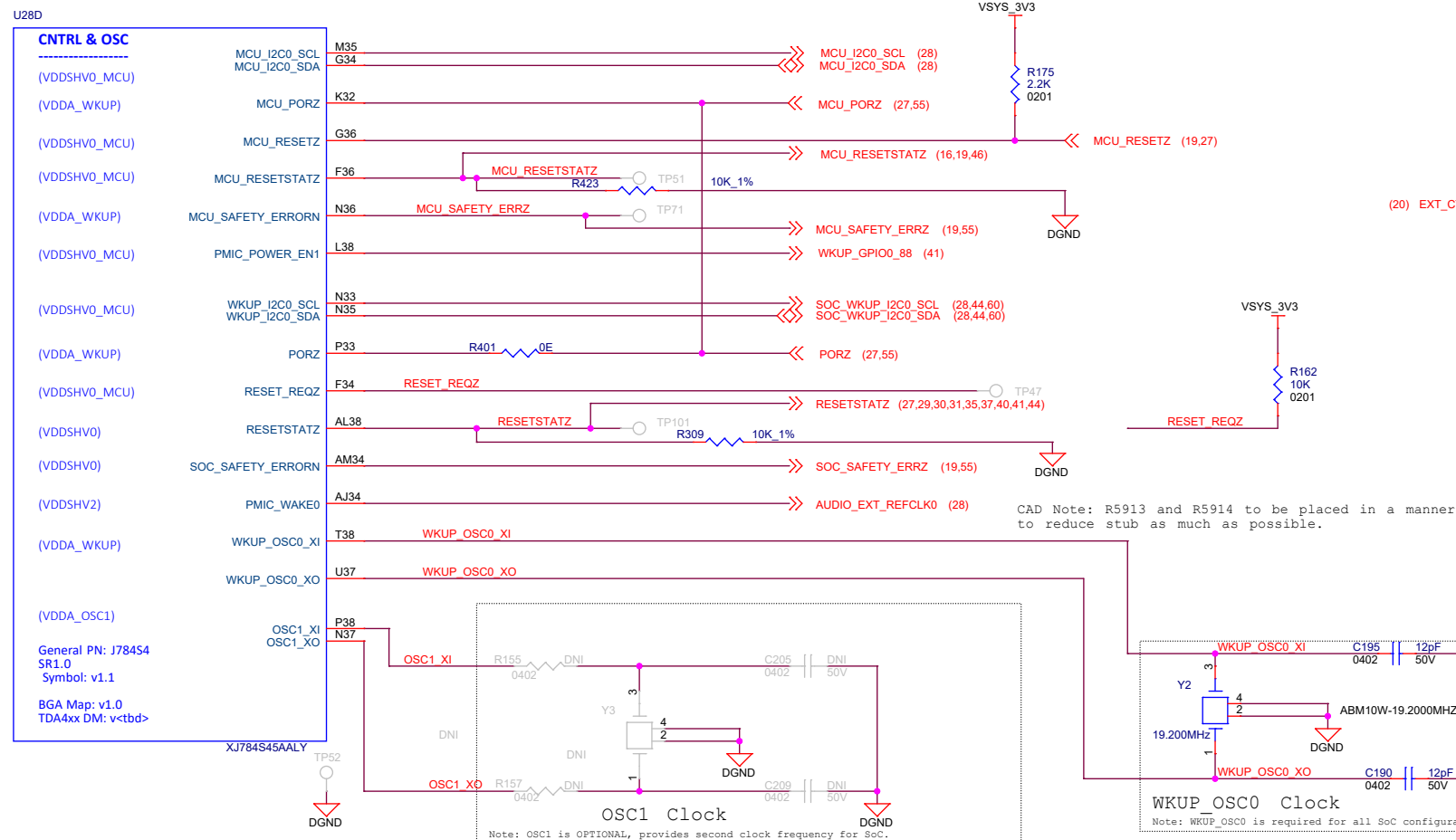
MCU & MAIN GENERAL IO, OSC CLKS



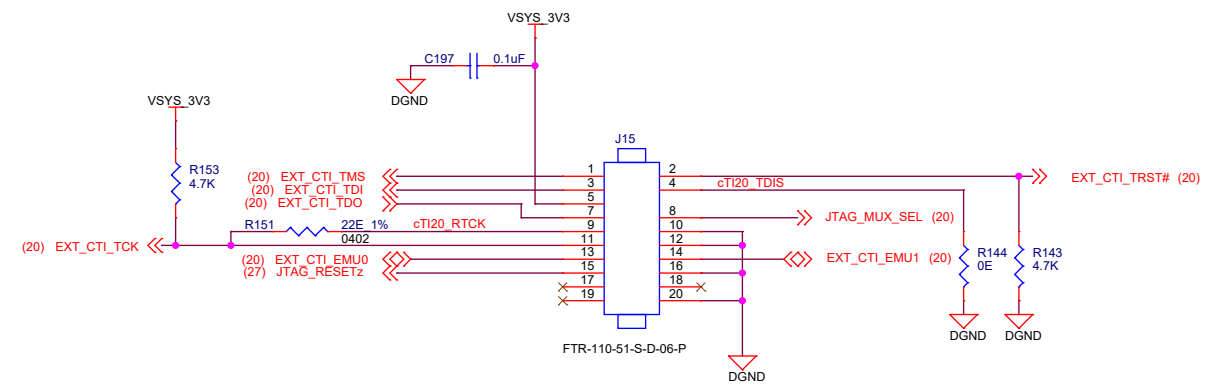
BOOTMODE



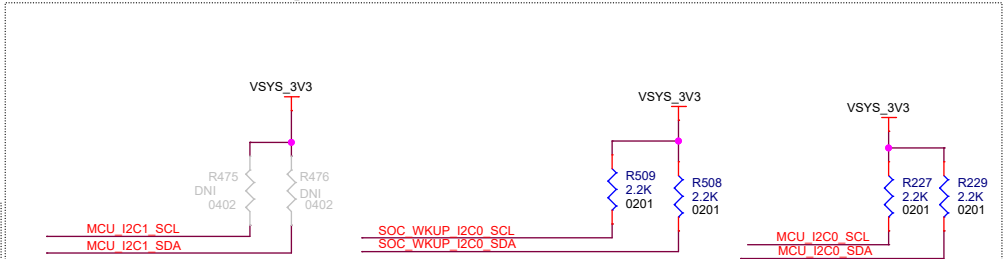
CONTROL & OSC



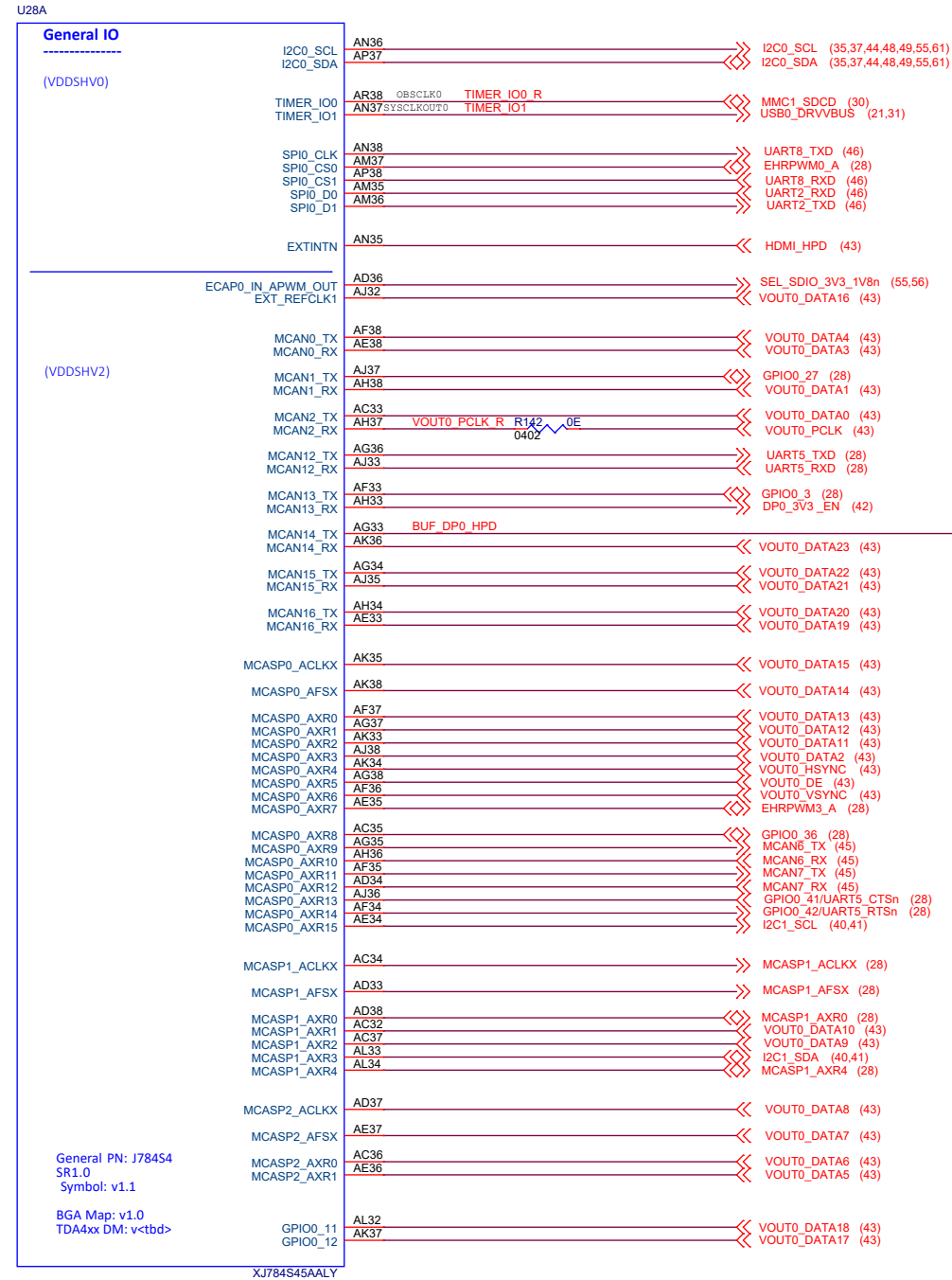
CTI 20PIN JTAG HEADER



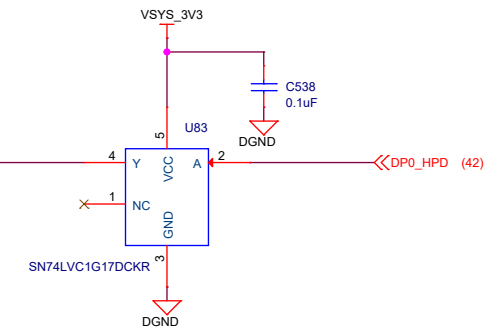
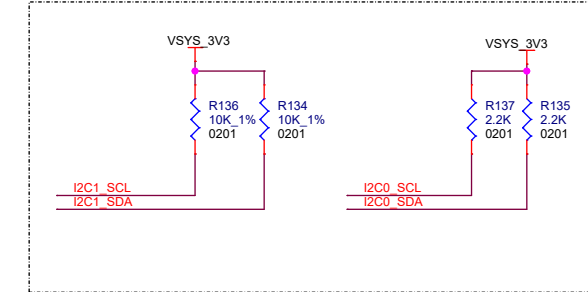
MCU/WKUP I2C Pull-ups



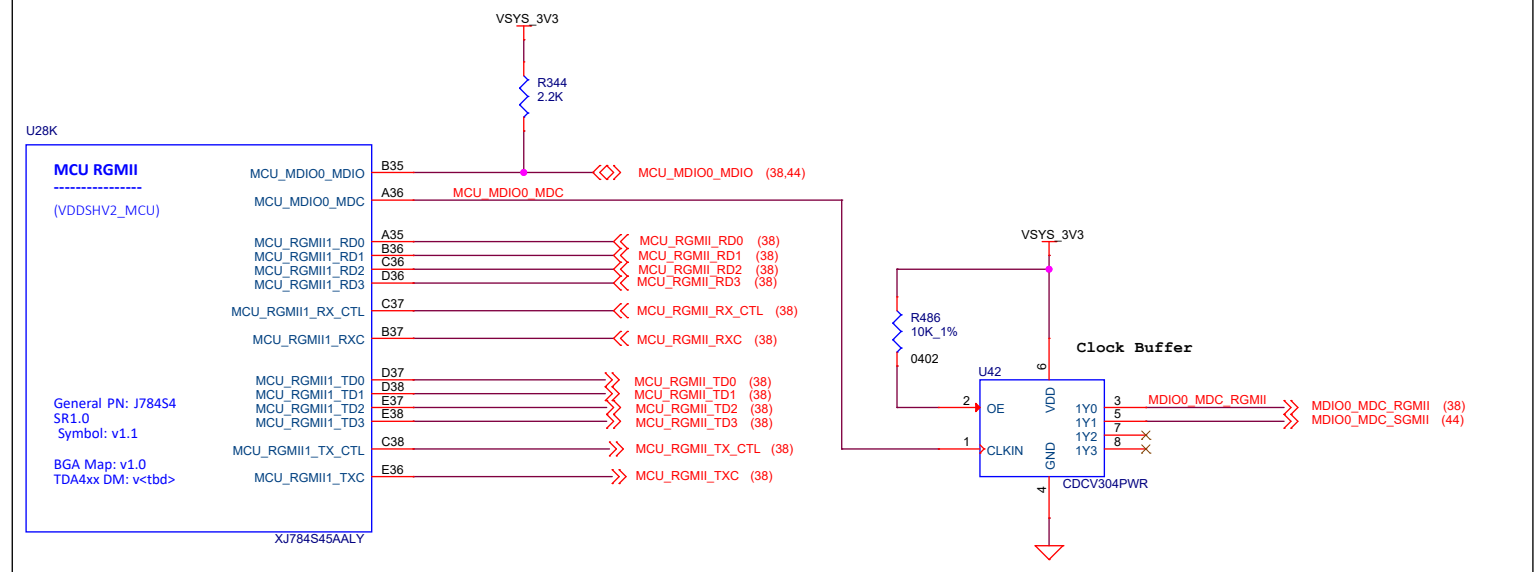
GENERAL IO



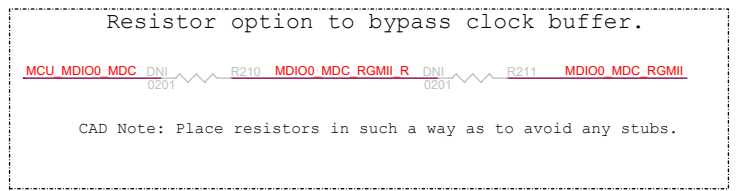
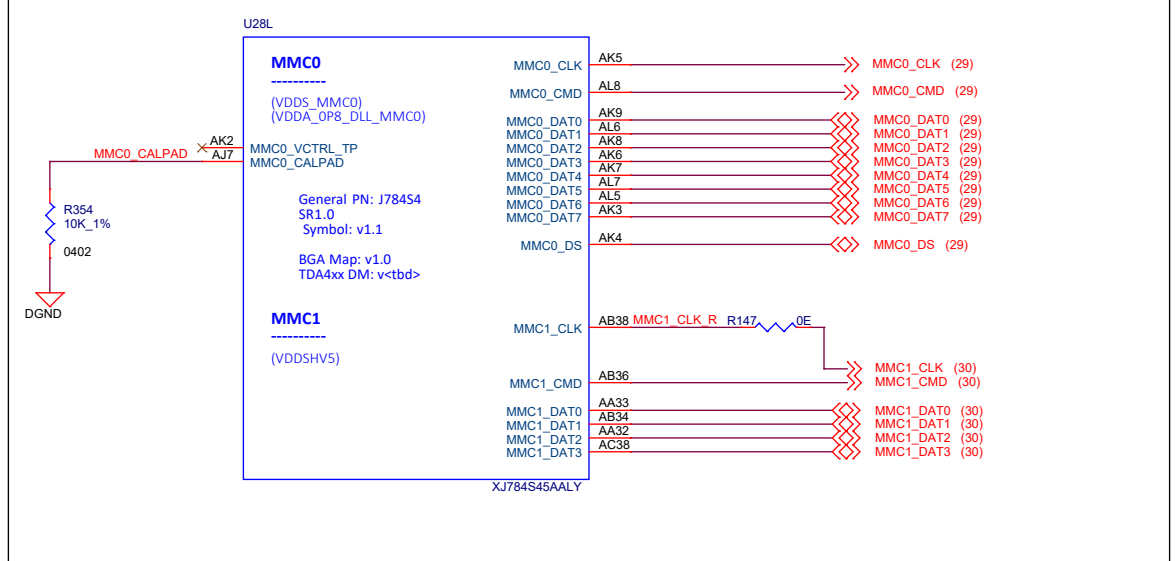
I2C Pull Ups



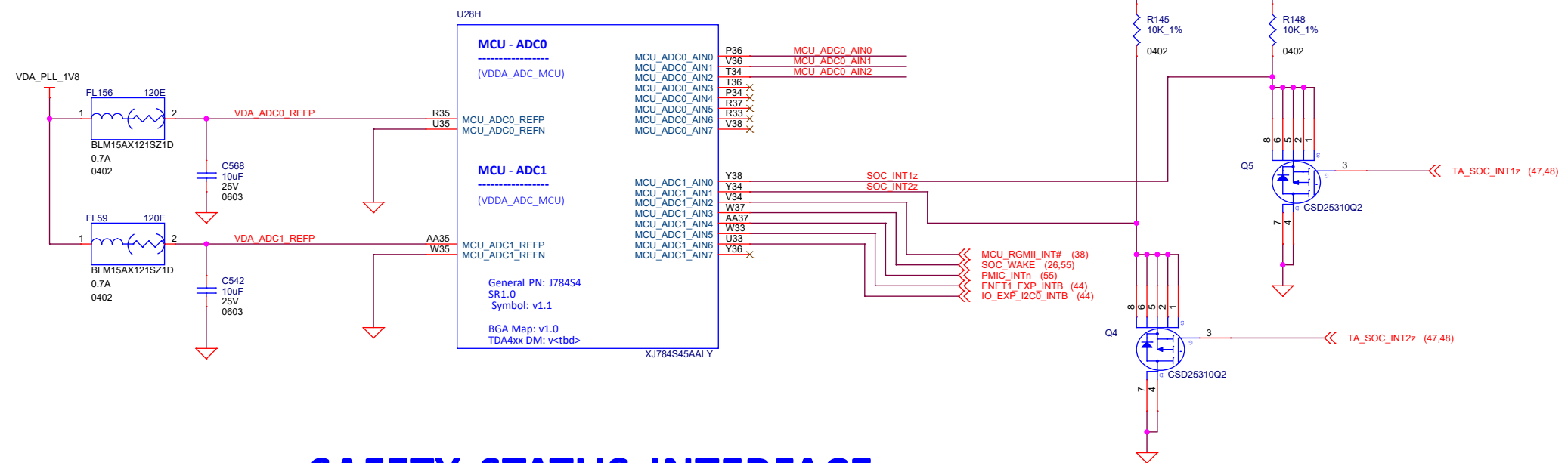
MCU_RGMII



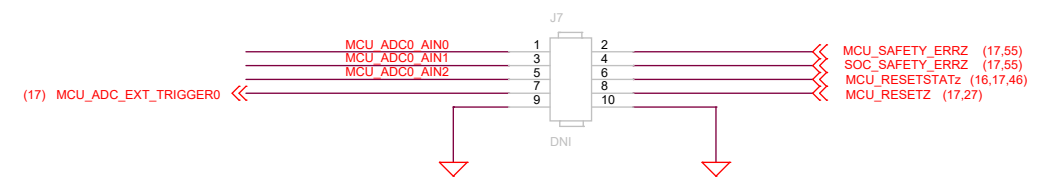
MMC0 and MMC1



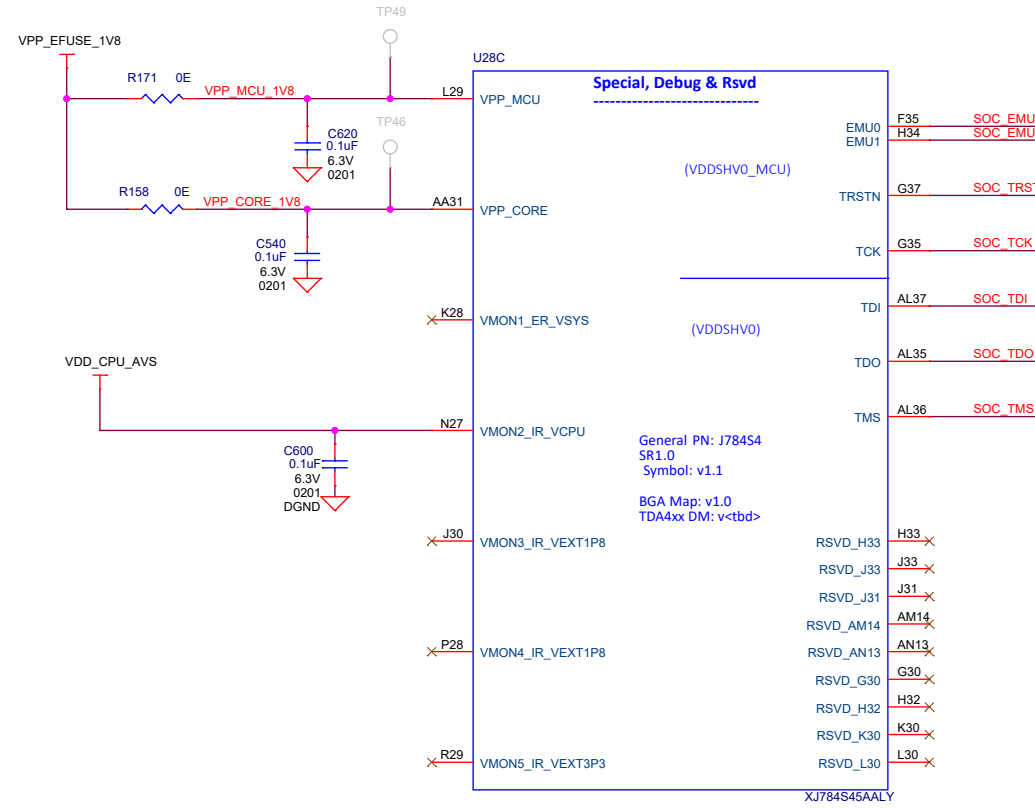
MCU_ADC



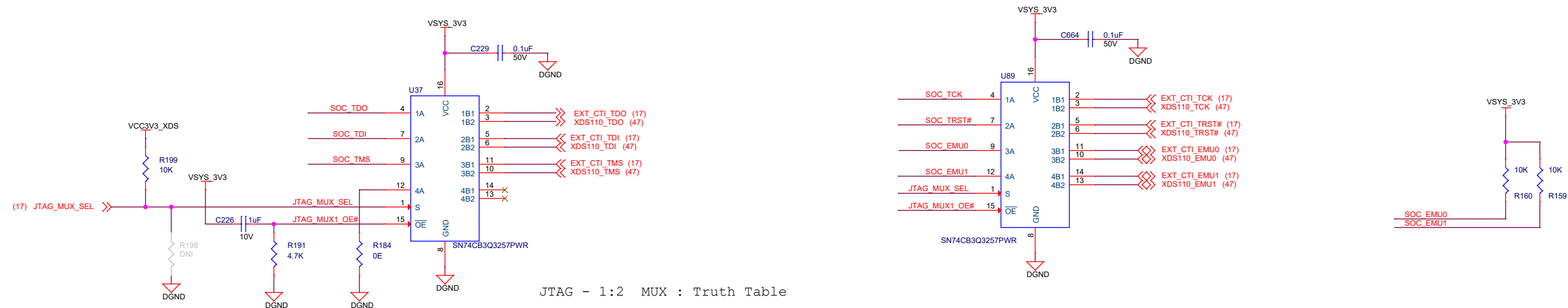
SAFETY STATUS INTERFACE



SPECIAL, DEBUG & RSVD



JTAG CONNECTOR AND XDS110 MUX

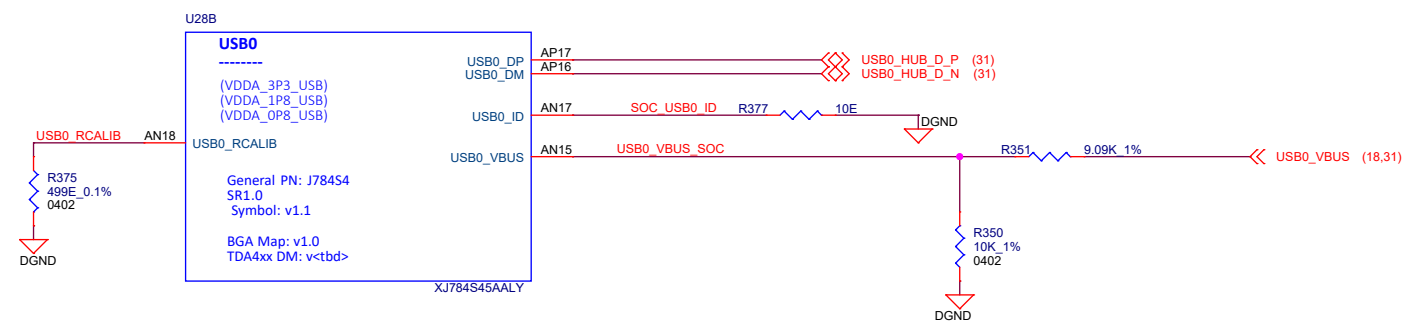


JTAG - 1:2 MUX : Truth Table

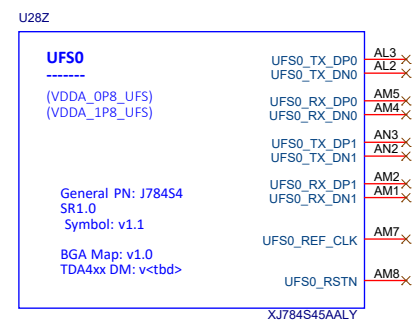
MUX_SEL	CONDITION	FUNCTION
LOW	External Emulator attached & No Power to XDS110	A-->B1 port [EXTERNAL EMU] (default)
HIGH	No External Emulator attached & XDS110 Powered via USB	A-->B2 port [ON Board EMU]

USB 2.0

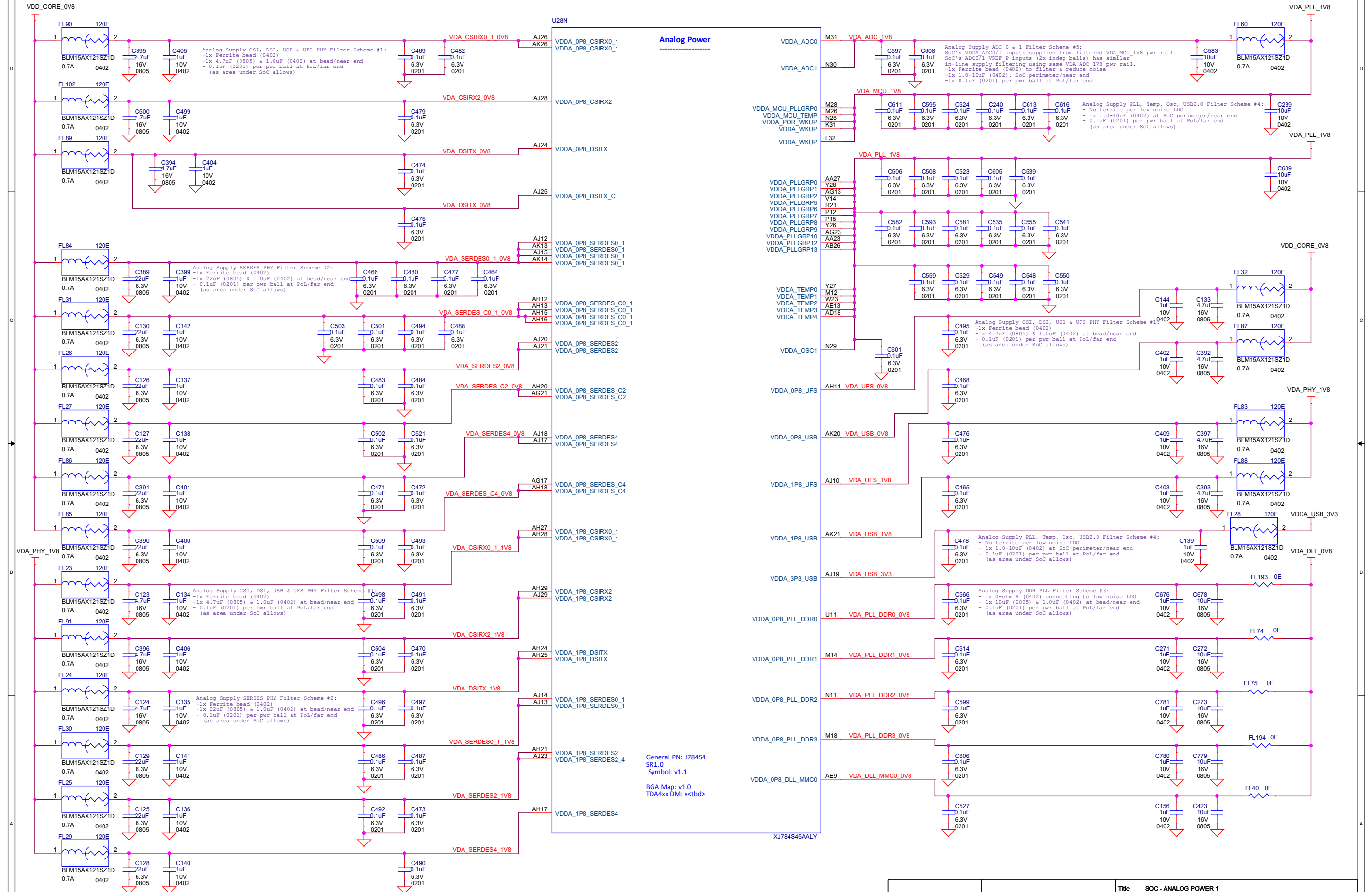
USB VBUS Resistor divider circuit



UFS FLASH

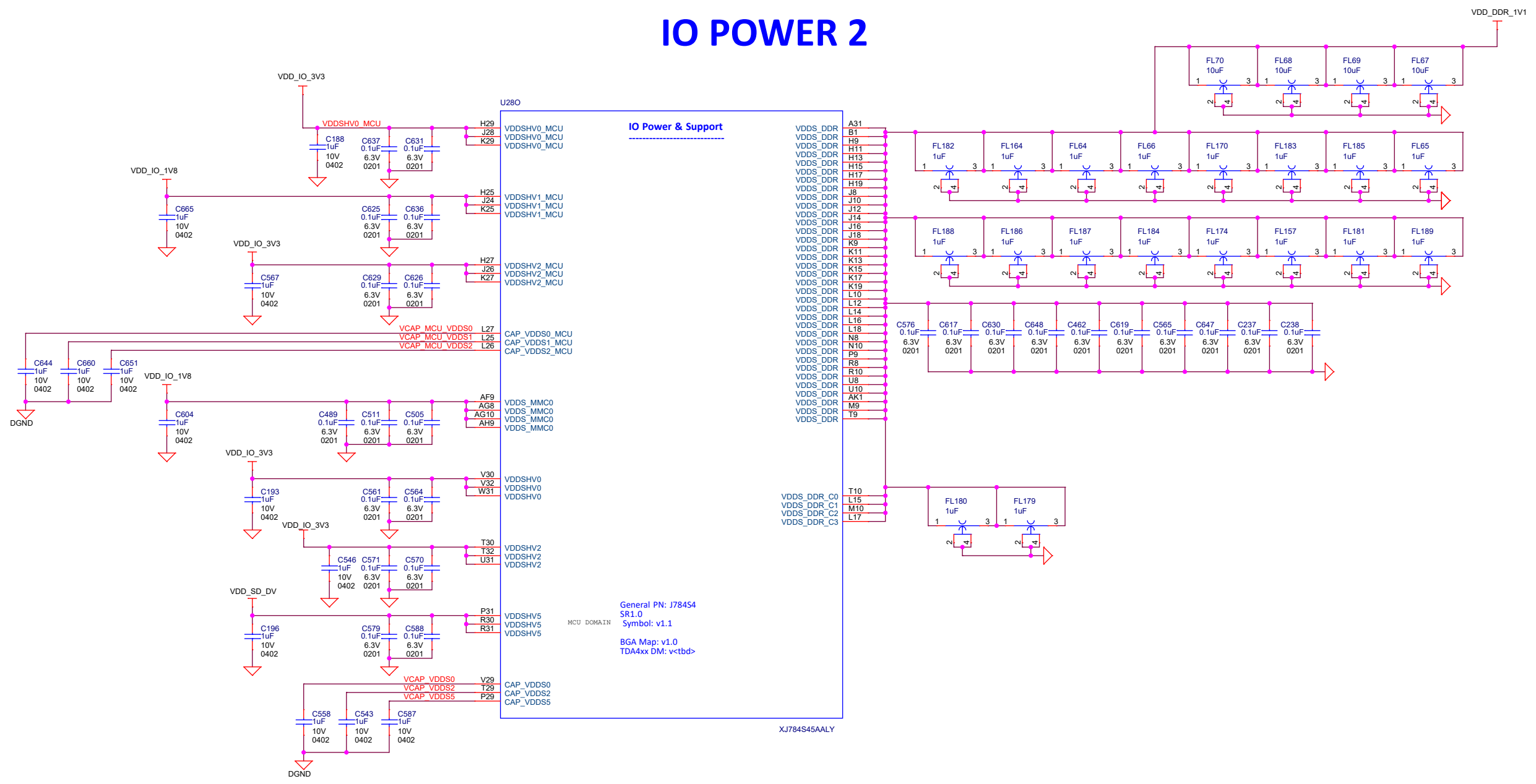


ANALOG POWER 1

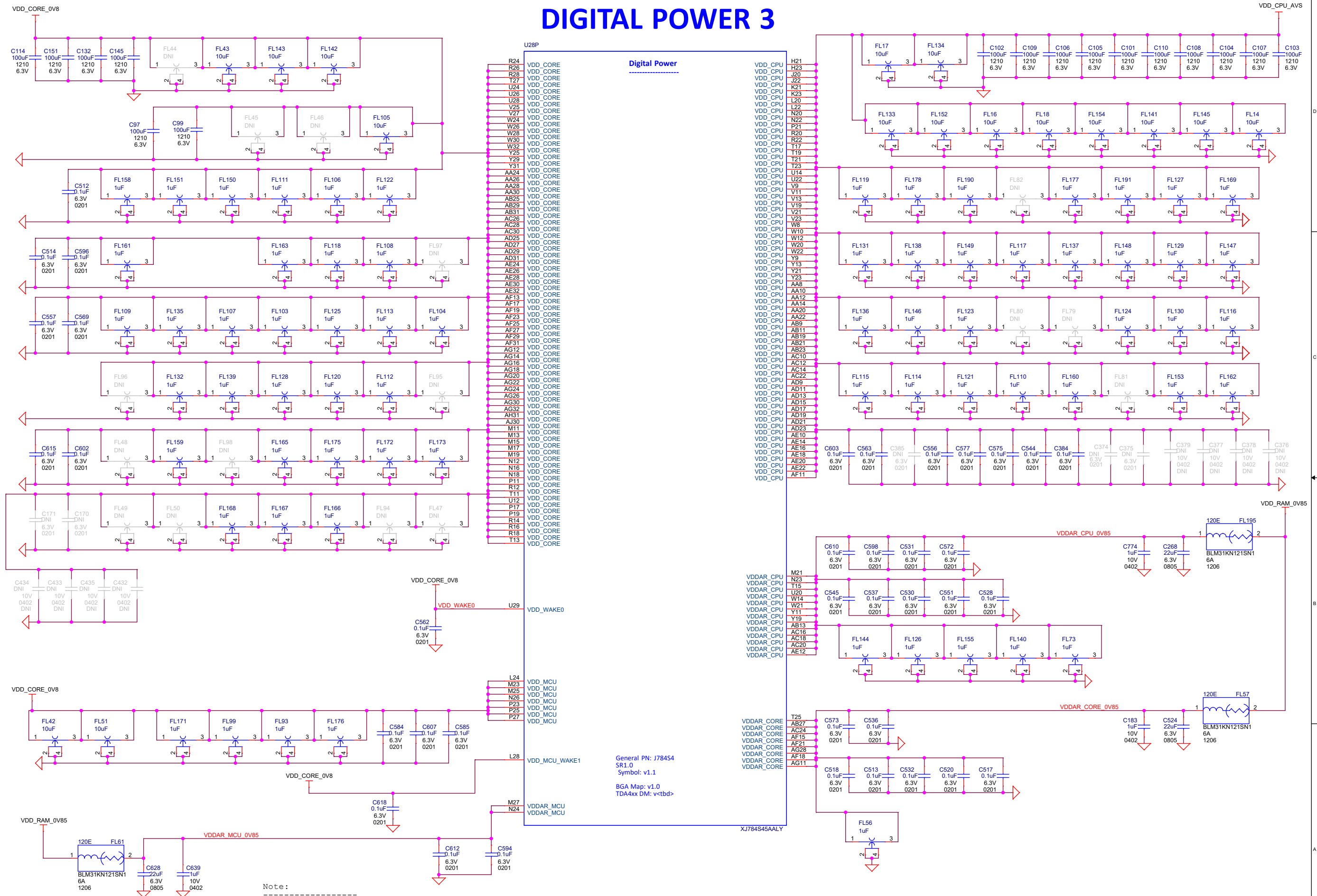


Project :		Title	
AM69 Edge AI Kit		SOC - ANALOG POWER 1	
Size	PROC154E3 001 SK AM69	Rev	E3
Date:	Monday, March 20, 2023	Sheet	22 of 62

IO POWER 2



DIGITAL POWER 3

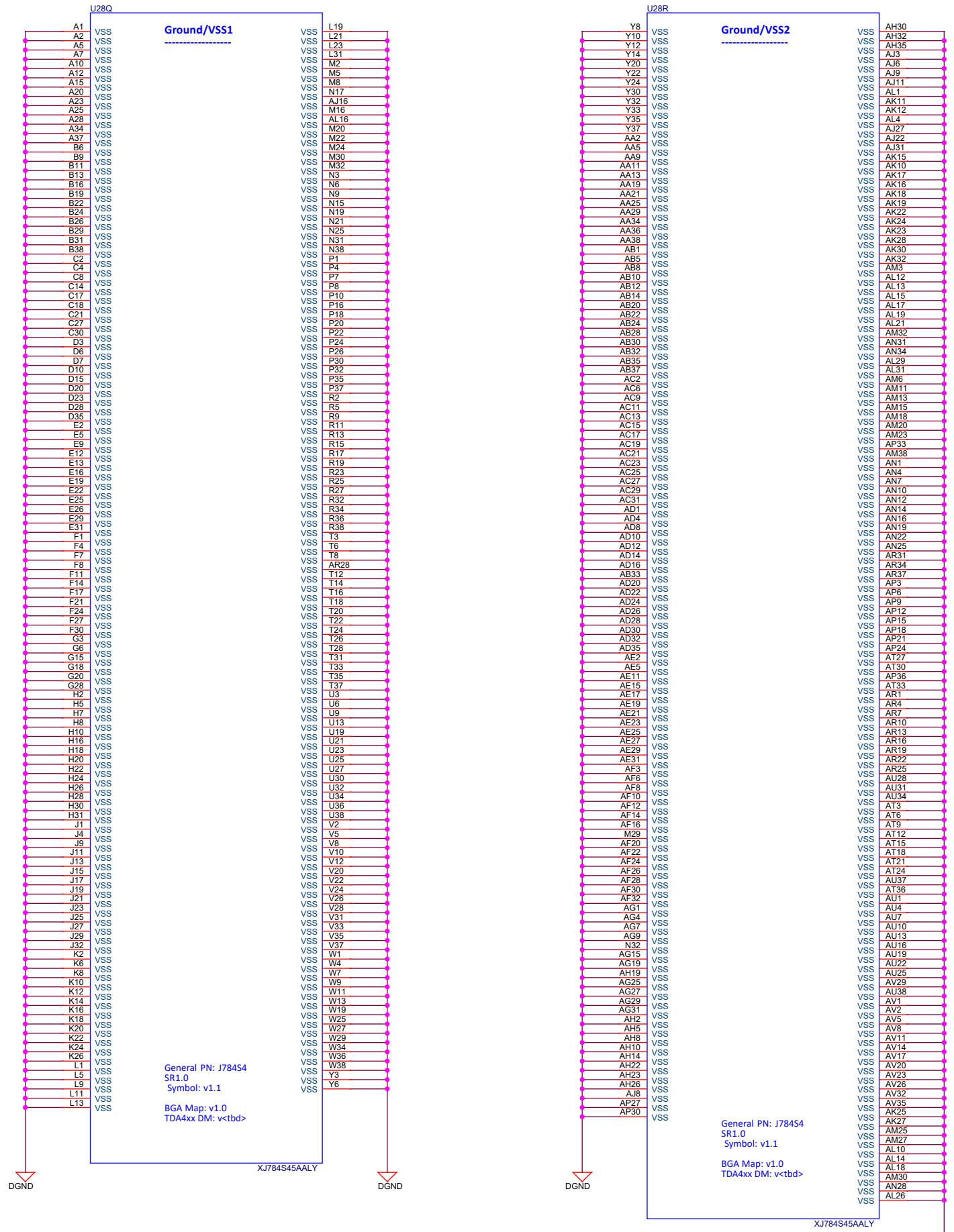


General PN: J78454 SR1.0
Symbol: v1.1
BGA Map: v1.0
TDA4xx DM: vctbd>

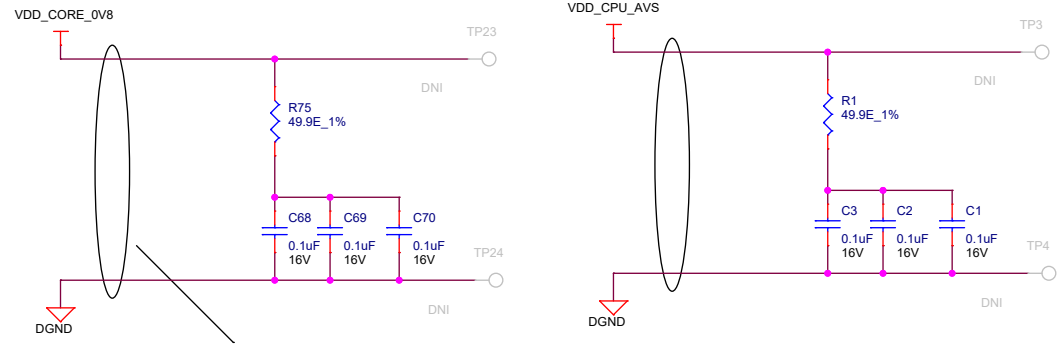
Note:
A few Dcaps shown here have been provisioned on PCB layout underneath SoC at individual power ball vias & around perimeter in case additional high-freq decoupling might be needed.
Some Dcaps may be shown as "Do Not Install" (DNI) components if Power Integrity (PI) simulation results for a particular power rail on this SK PCB design combined with Dcap scheme (value, pkg type, ESL, Loop-Inductance, etc.) results in an impedance response below or equal to the desired target impedance (Zt).

Project : AM69 Edge AI Kit		Title SOC - DIGITAL POWER 3	
		Size PROC154E3 001 SK AM69	Rev E3
Date: Monday, March 20, 2023	Sheet 24 of 62		

SOC GROUND



SoC Supply Noise Kelvin Sensing

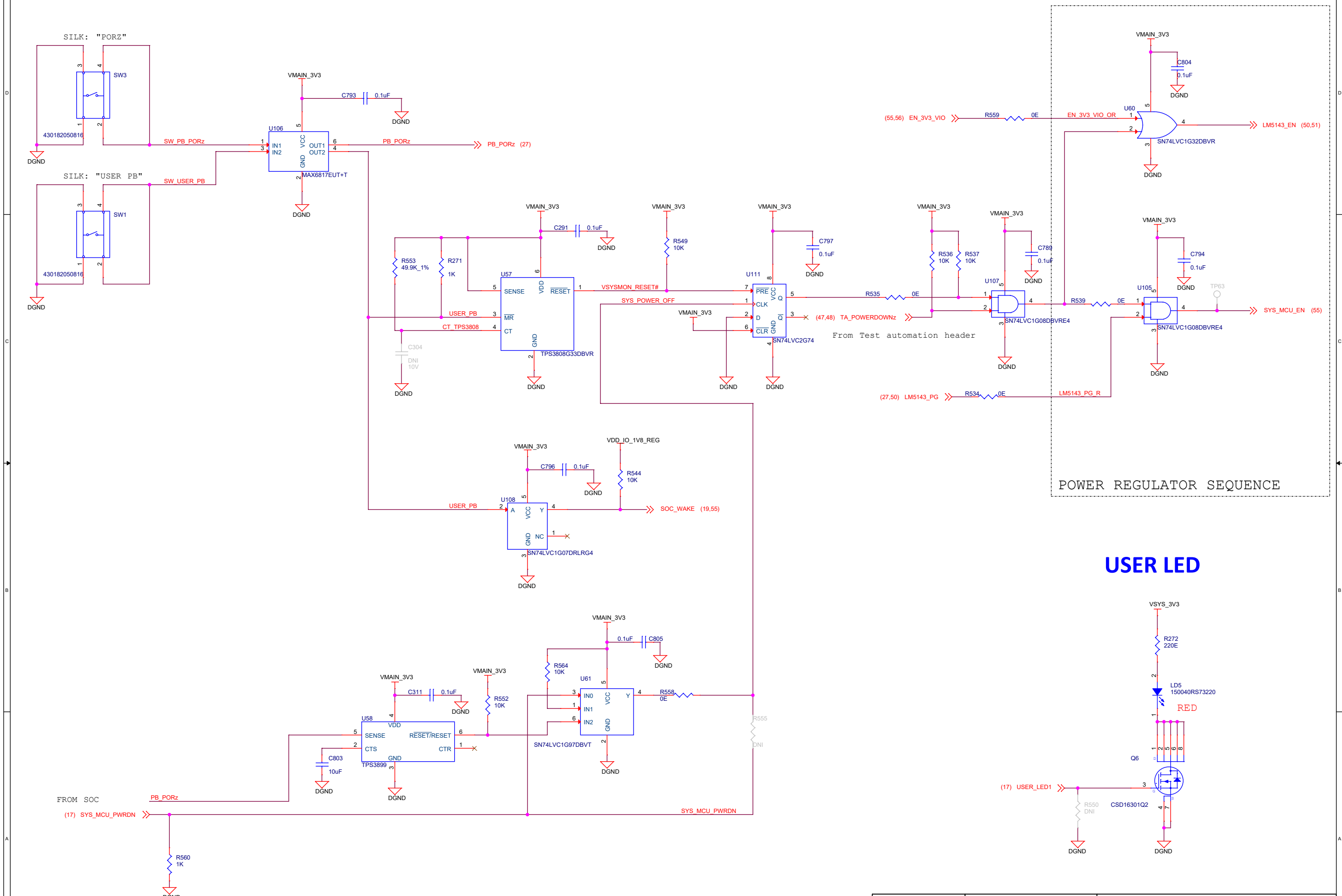


Route supply & Gnd connections from SoC PoL as a pseudo differential pair to TPs near R & C termination for easy access

Project :		Title SOC - GROUND & KELVIN SENSING	
AM69 Edge AI Kit		Size PROC154E3 001 SK AM69	
		Rev E3	
Date: Monday, March 20, 2023		Sheet 25 of 62	



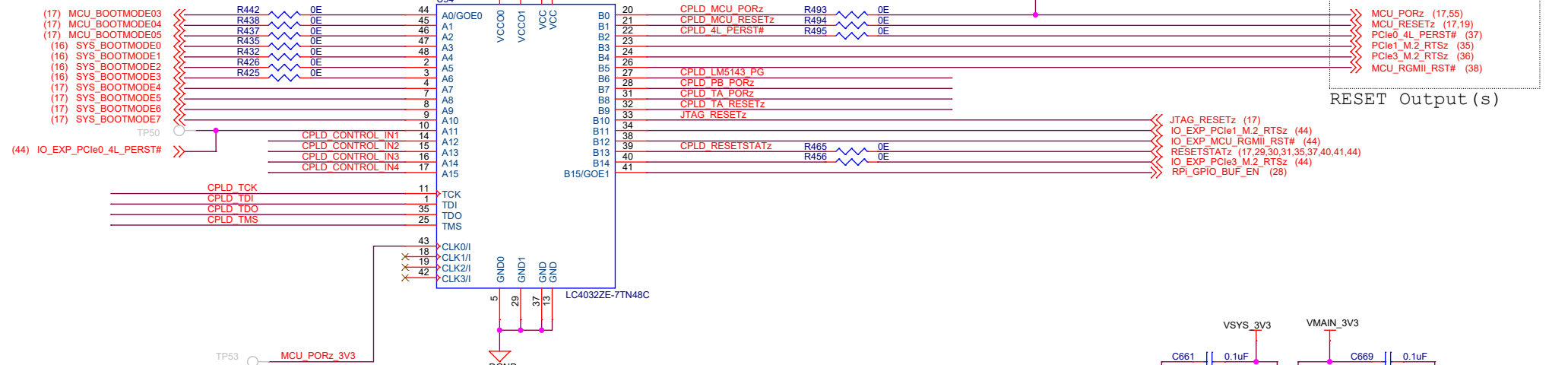
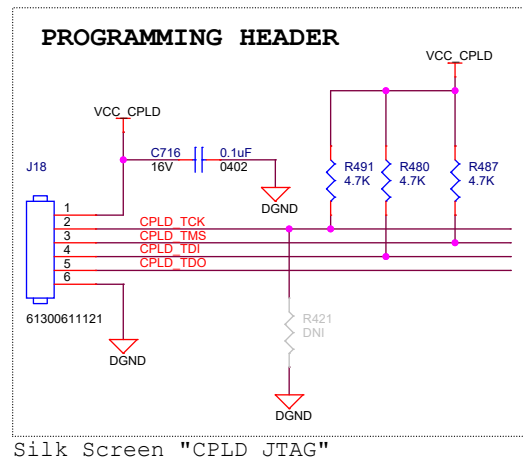
RESET BUTTONS



Project : AM69 Edge AI Kit		Title RESET BUTTONS	
Size C		PROC154E3 001 SK AM69	
Date: Monday, March 20, 2023		Rev E3	
Sheet 26 of 62			

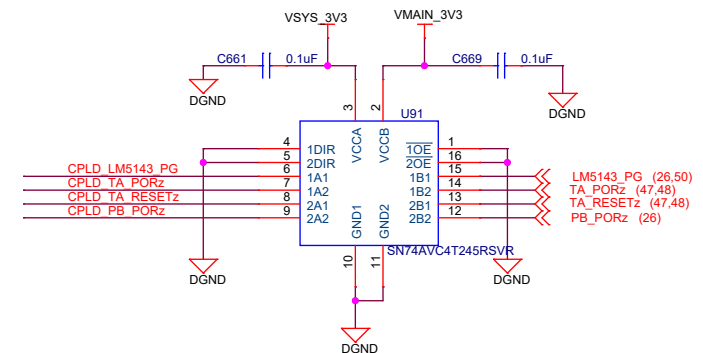
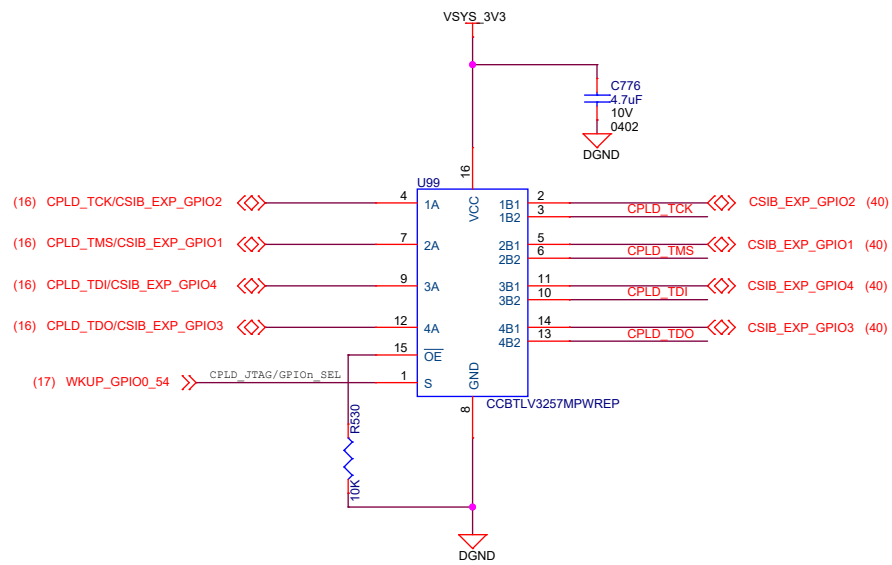
CPLD

Default termination on IOs is Pull down, when the CPLD is not programmed.



Note: MCU_PORz is open-drain output (pulled to 1.8V)

RESET Output (s)

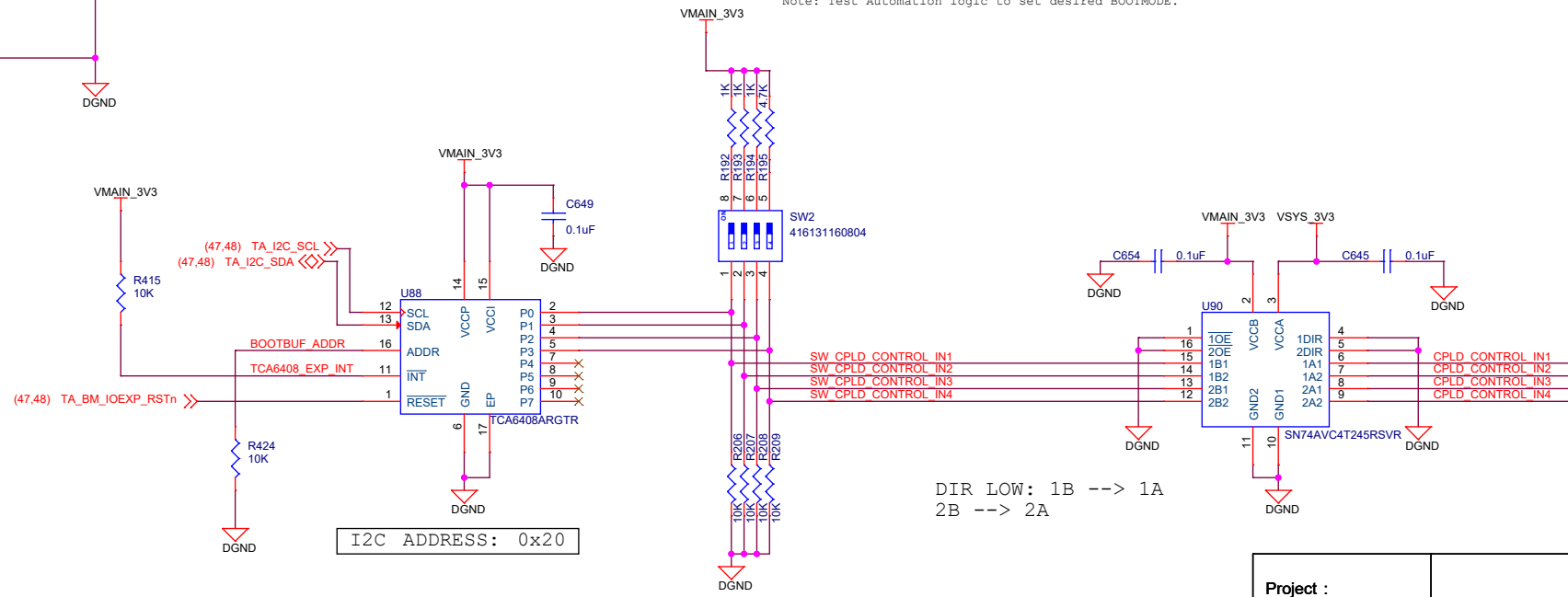


Bootmode Table

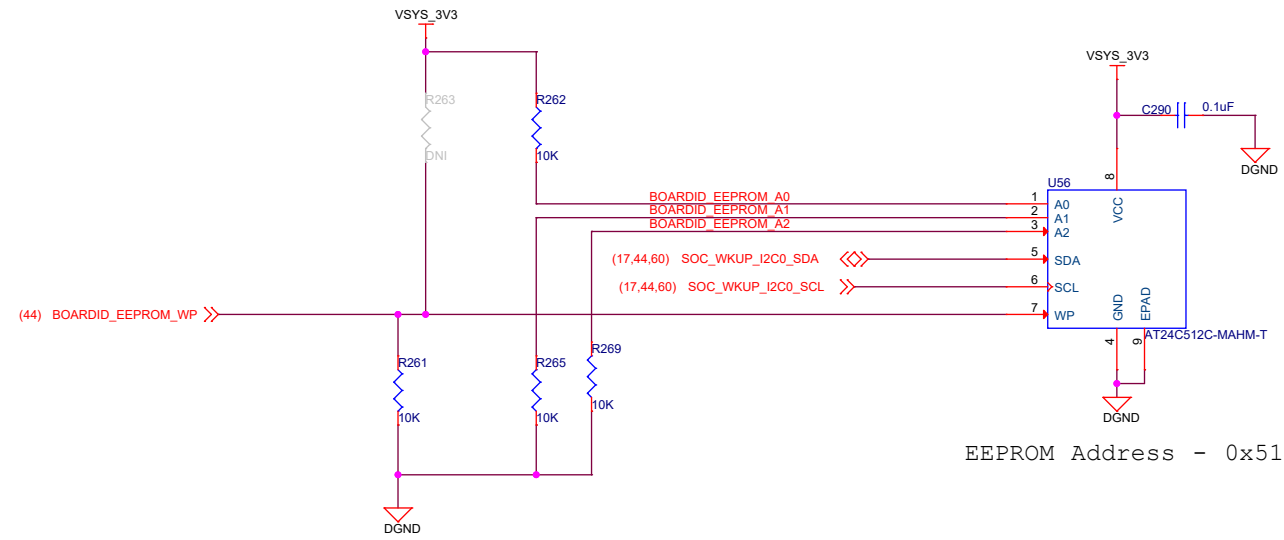
SW2.3	SW2.2	SW2.1	BOOTMODE
0	0	0	SD
0	0	1	NO Boot
0	1	0	Ethernet
0	1	1	USB
1	0	0	xSPI - 1S
1	0	1	UART
1	1	0	eMMC
1	1	1	xSPI SFDP

Test Automation BOOTMODE Logic

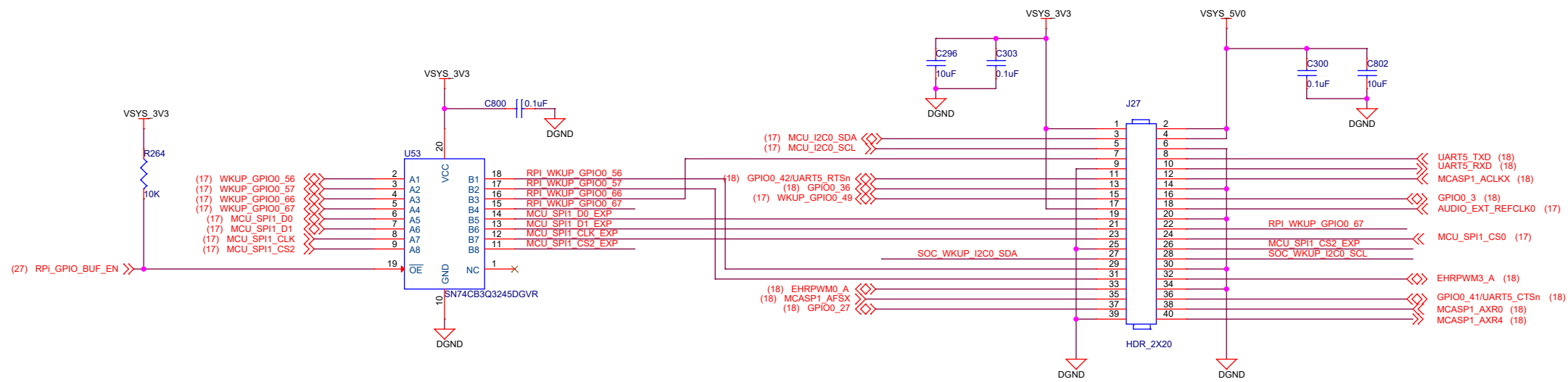
Note: Test Automation logic to set desired BOOTMODE.



BOARD ID EEPROM



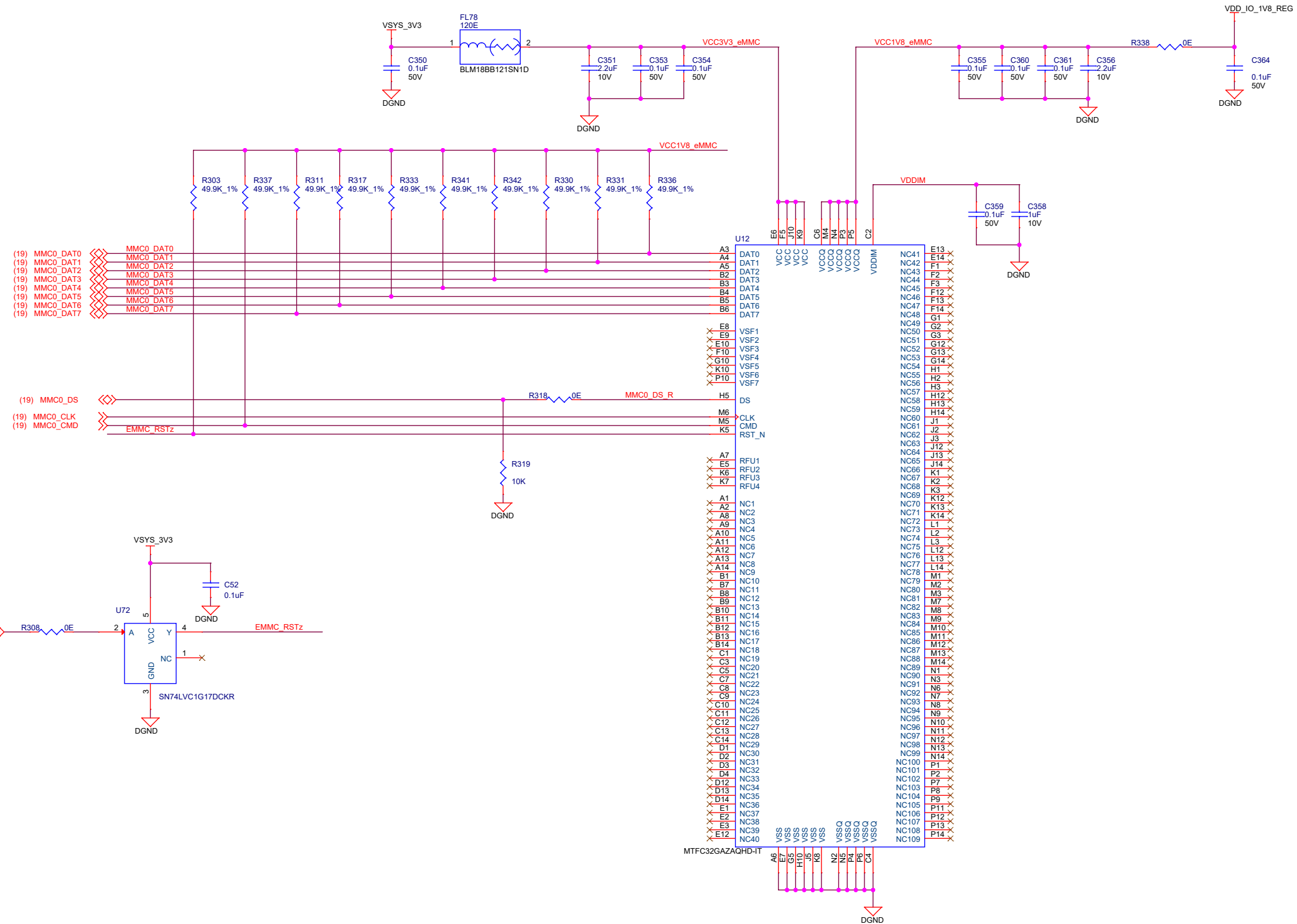
40Pin Expansion Header



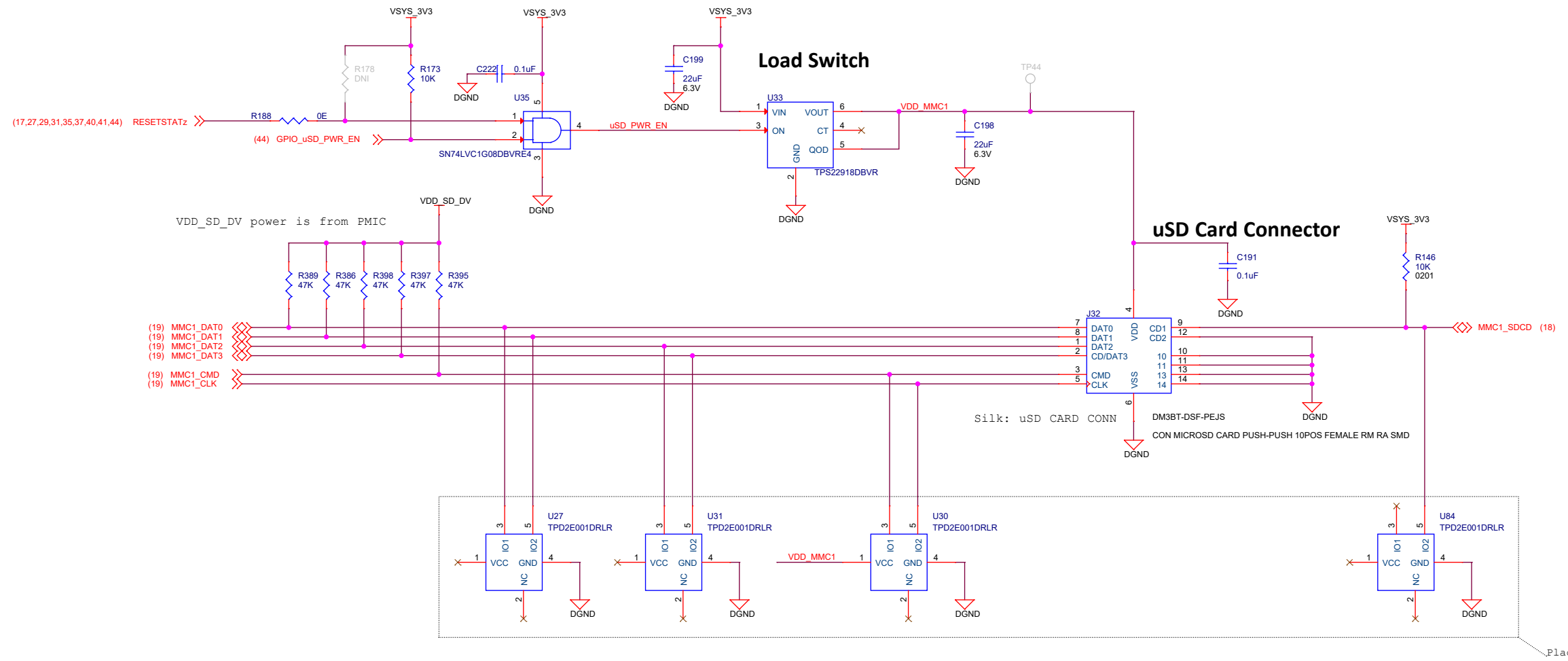
Silk Screen "40p EXP HDR"

Project :		Title BOARD ID EEPROM & 40 PIN EXP HEADER	
AM69 Edge AI Kit		Size PROC154E3 001 SK AM89	
		Rev E3	
Date: Monday, March 20, 2023		Sheet 28 of 62	

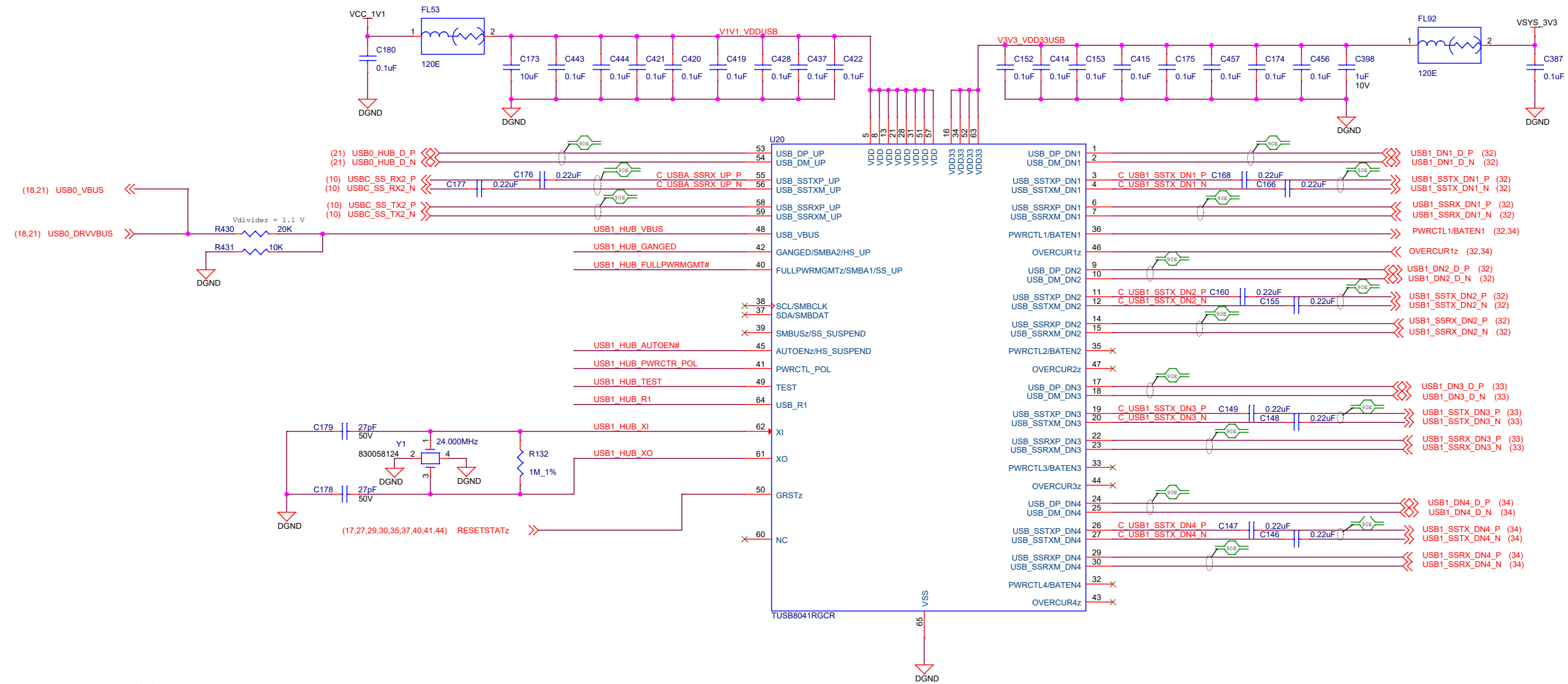
eMMC FLASH



Micro SD CARD INTERFACE



USB3.0 HUB



(18,21) USB0_VBUS

(18,21) USB0_DRVVBUS

(17,27,29,30,35,37,40,41,44) RESETSTATz

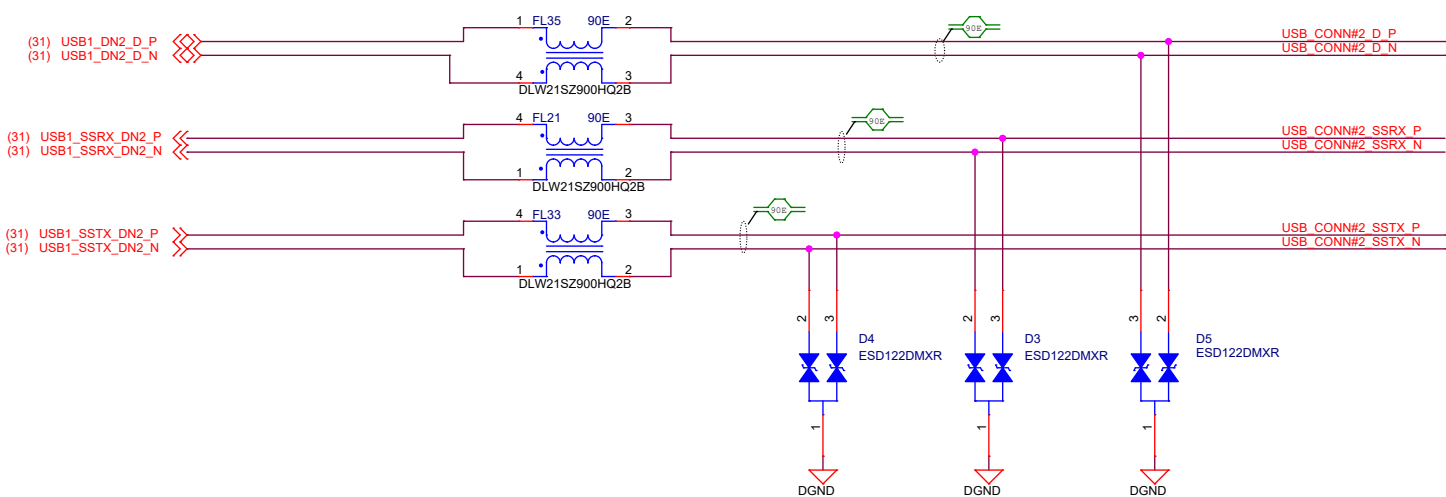
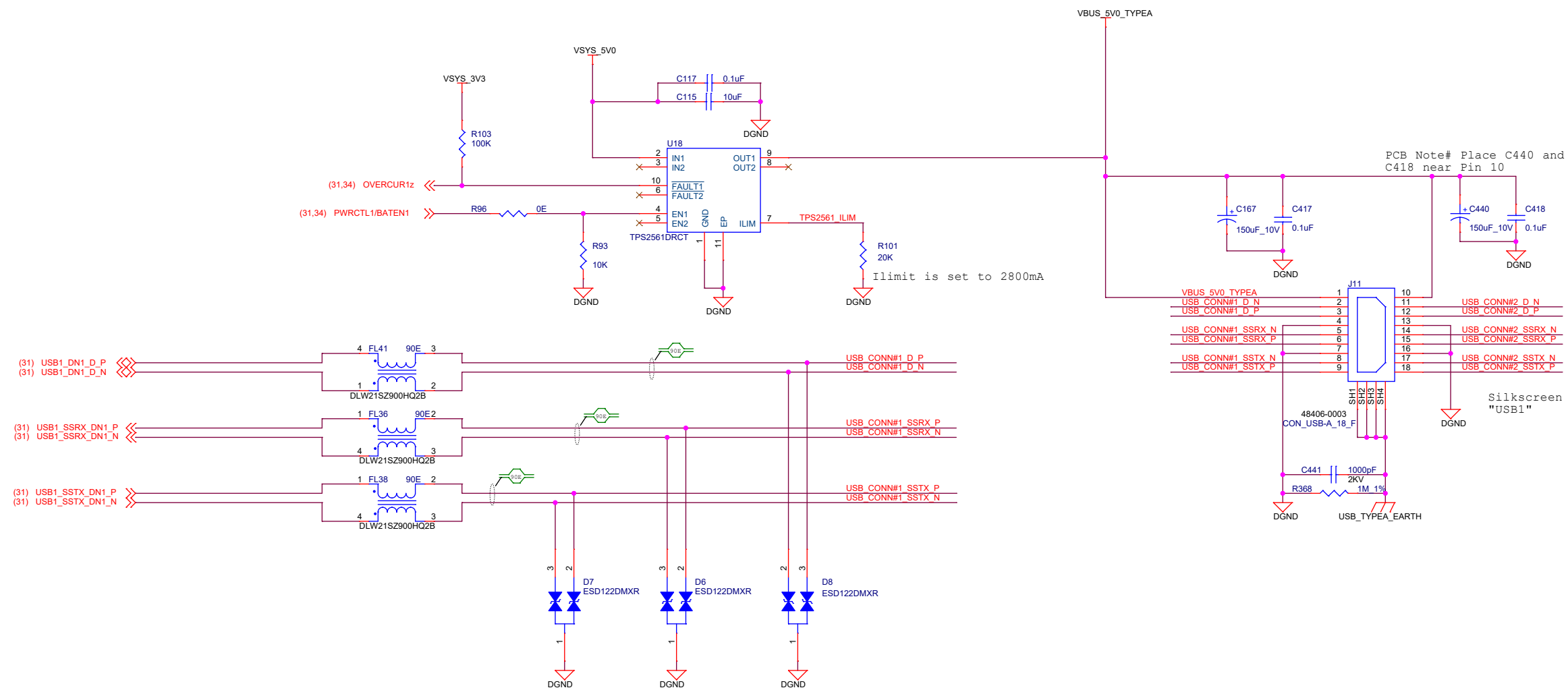
NOTE:

#1	USB1_HUB_AUTOEN#
#2	USB1_HUB_PWRCTR_POL
#3	USB1_HUB_FULLPWRMGMT#
#4	USB1_HUB_GANGED
	USB1_HUB_TEST
	USB1_HUB_R1

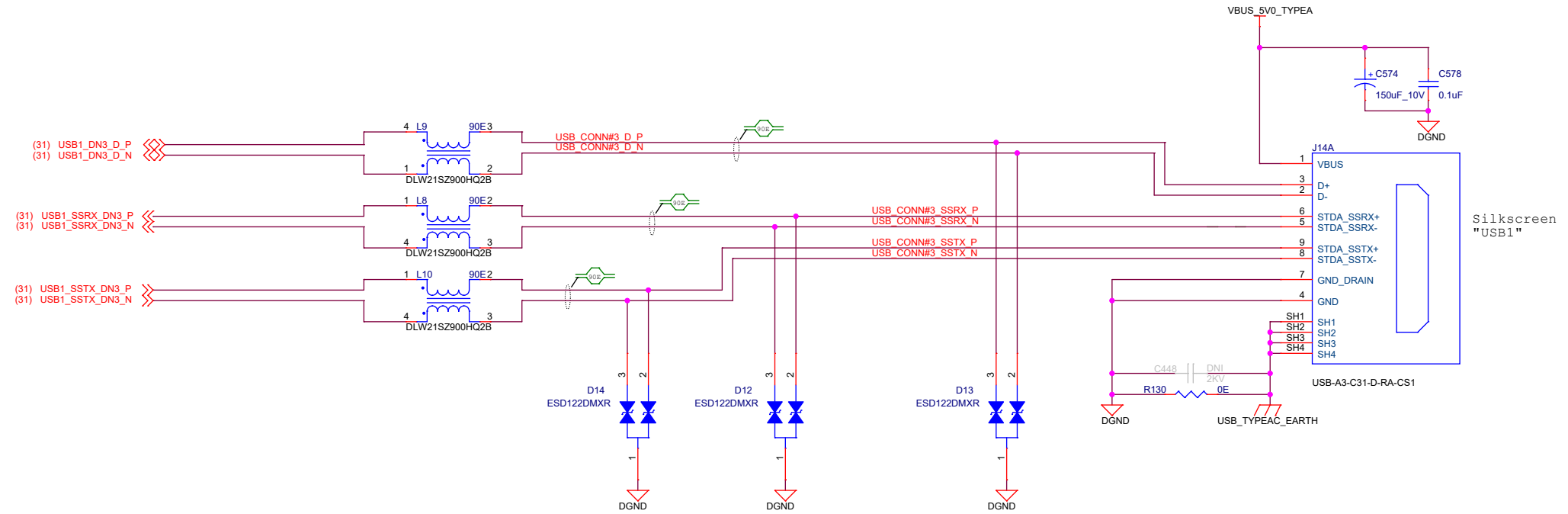
NOTE:

#1 Automatic Charge Mode Disabled
 #2 PWRCTL Polarity is Active High
 #3 Power Switching and Overcurrent Inputs Supported
 #4 Ganged Power Control Enabled

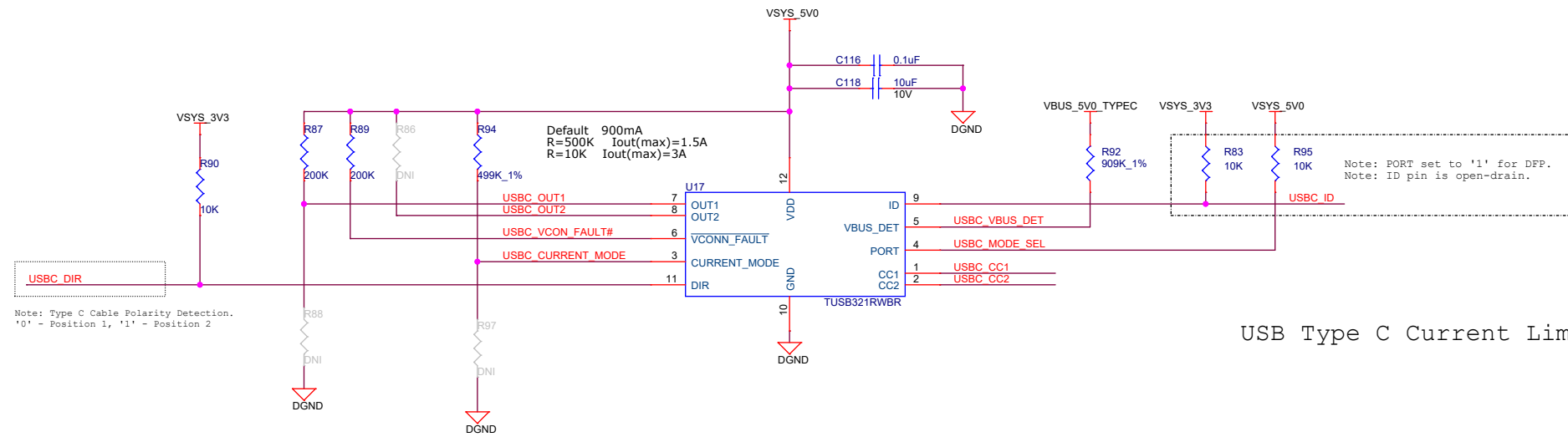
USB 3.0 TYPE-A CONNECTORS - 1



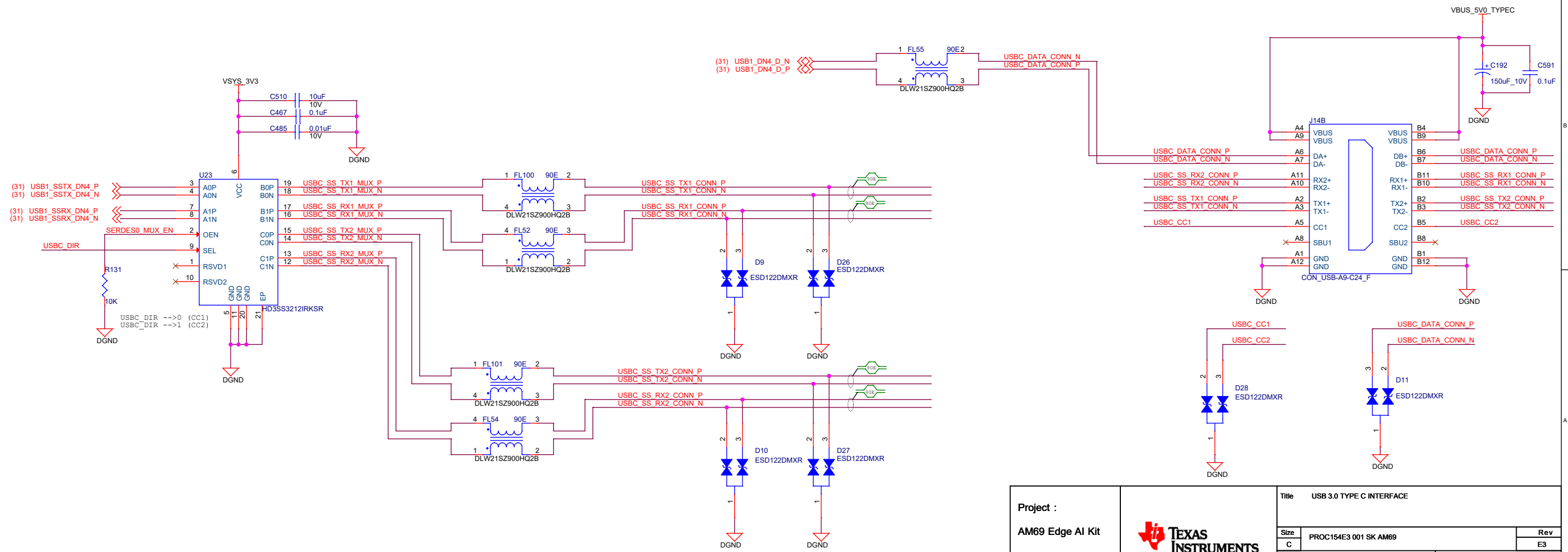
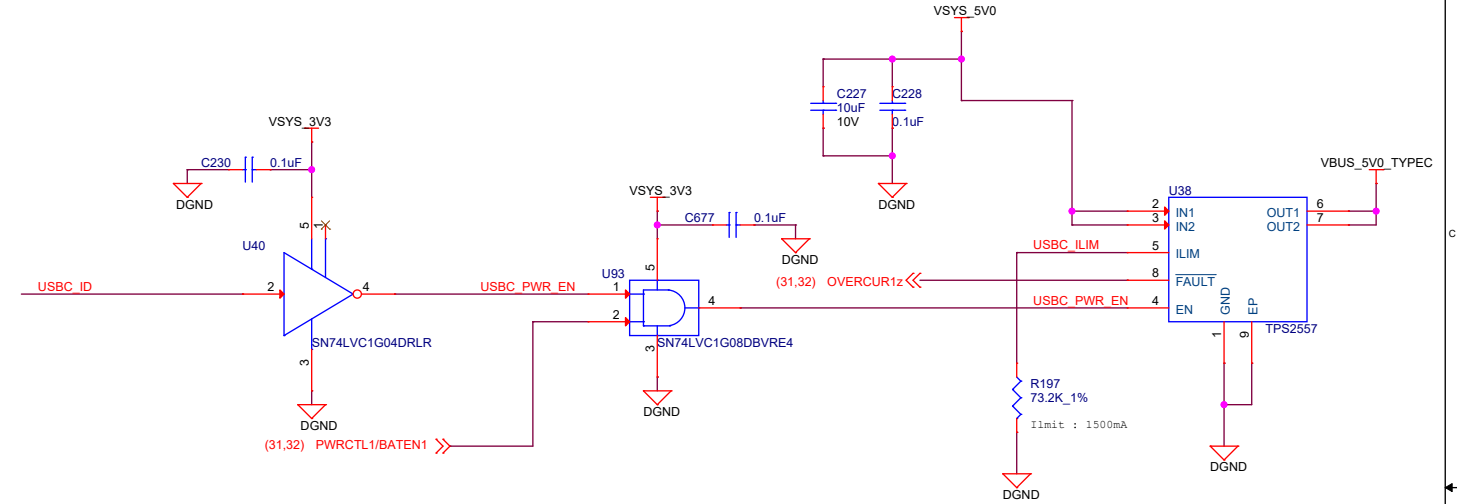
USB 3.0 TYPE-A CONNECTORS - 2



USB 3.0 TYPE C INTERFACE

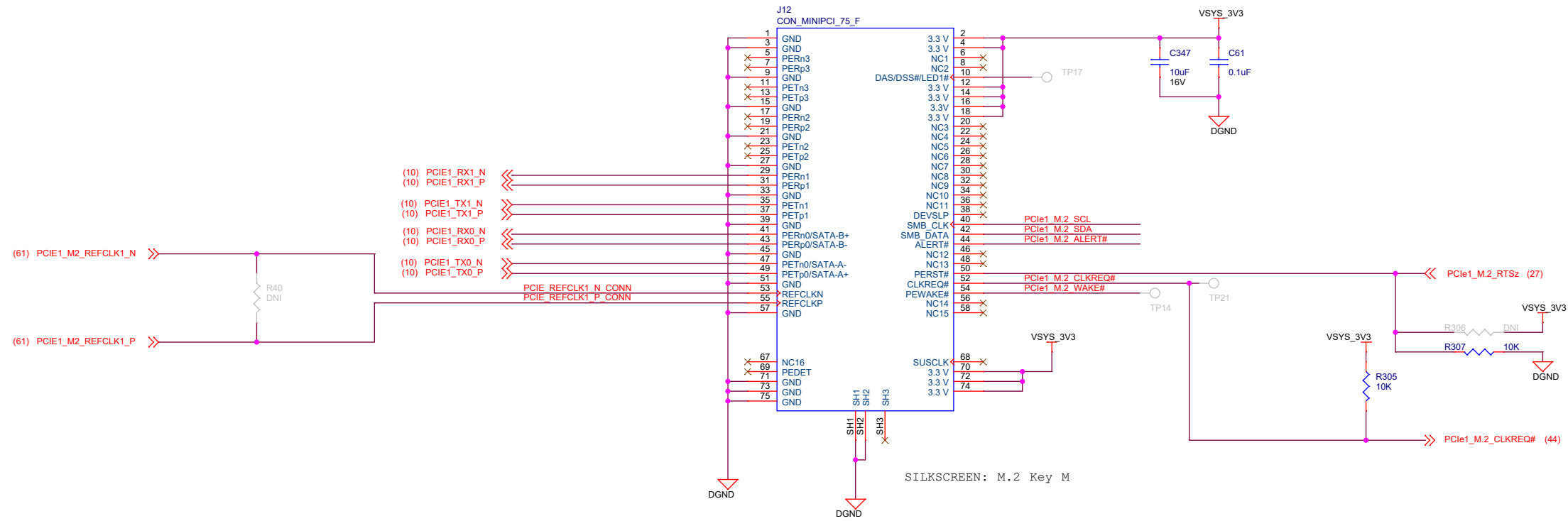


USB Type C Current Limit

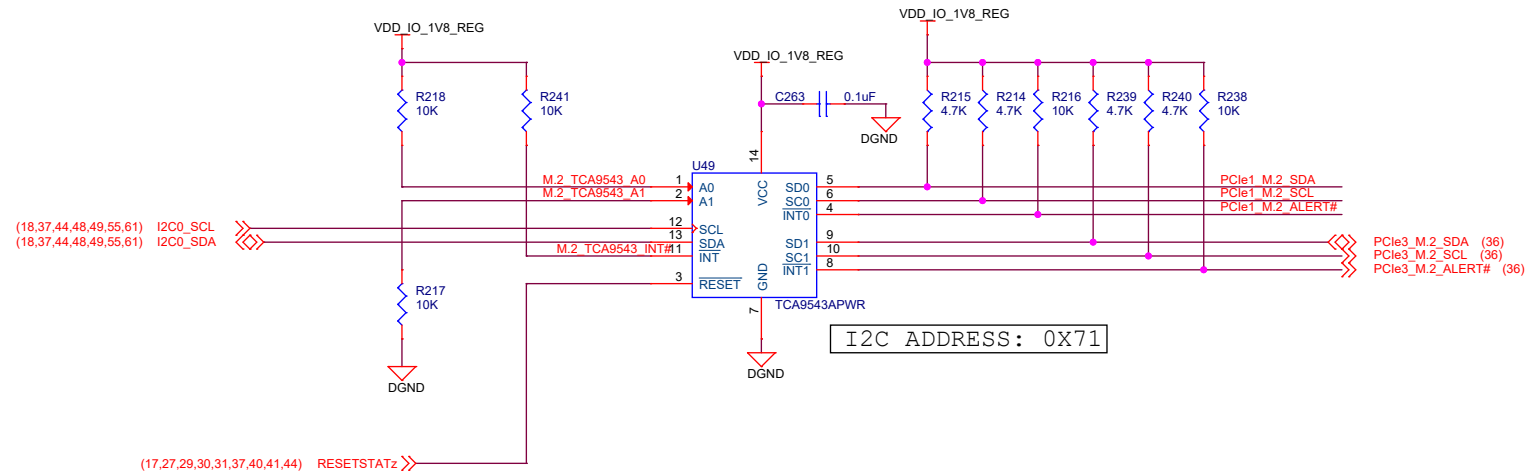


PCIe_M.2_INTERFACE SSD

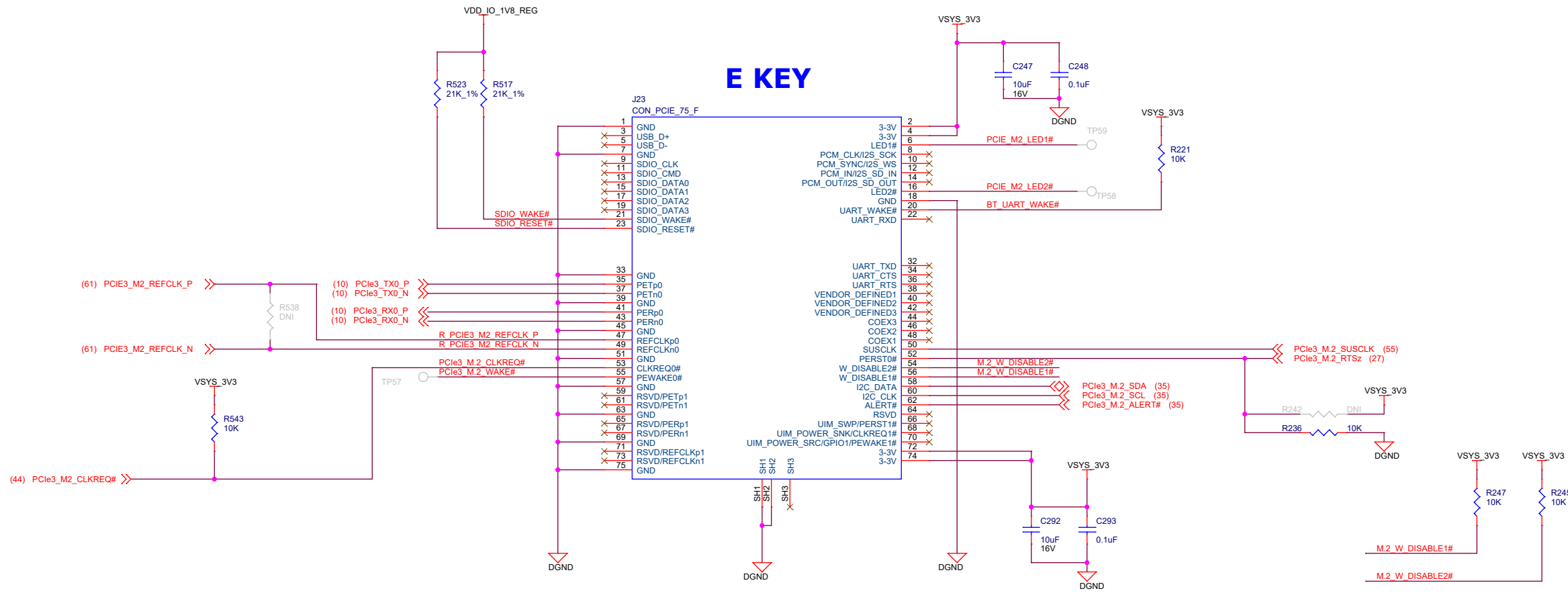
M KEY



3.3V To 1V8 Level translator



PCIe_M.2_INTERFACE - SDIO

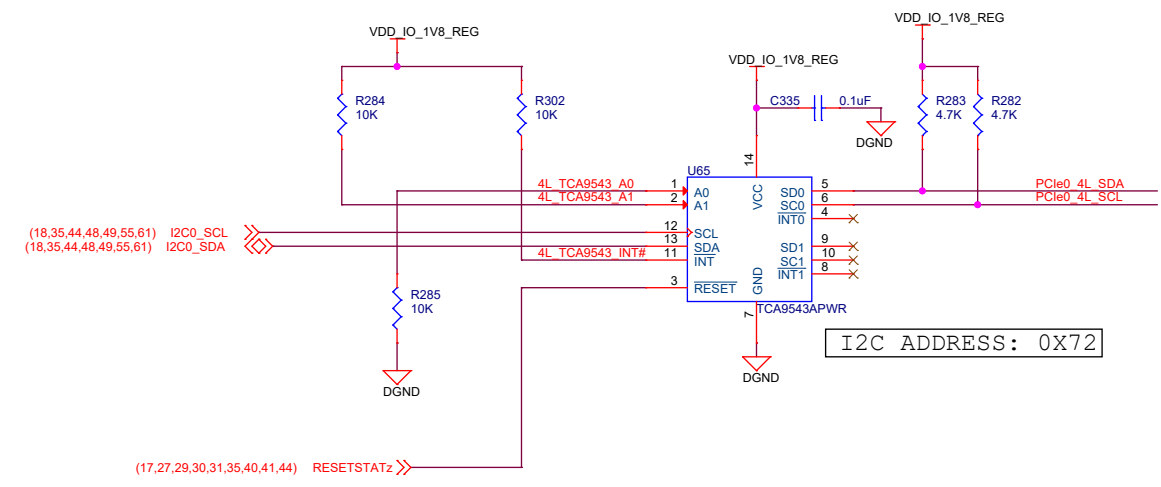
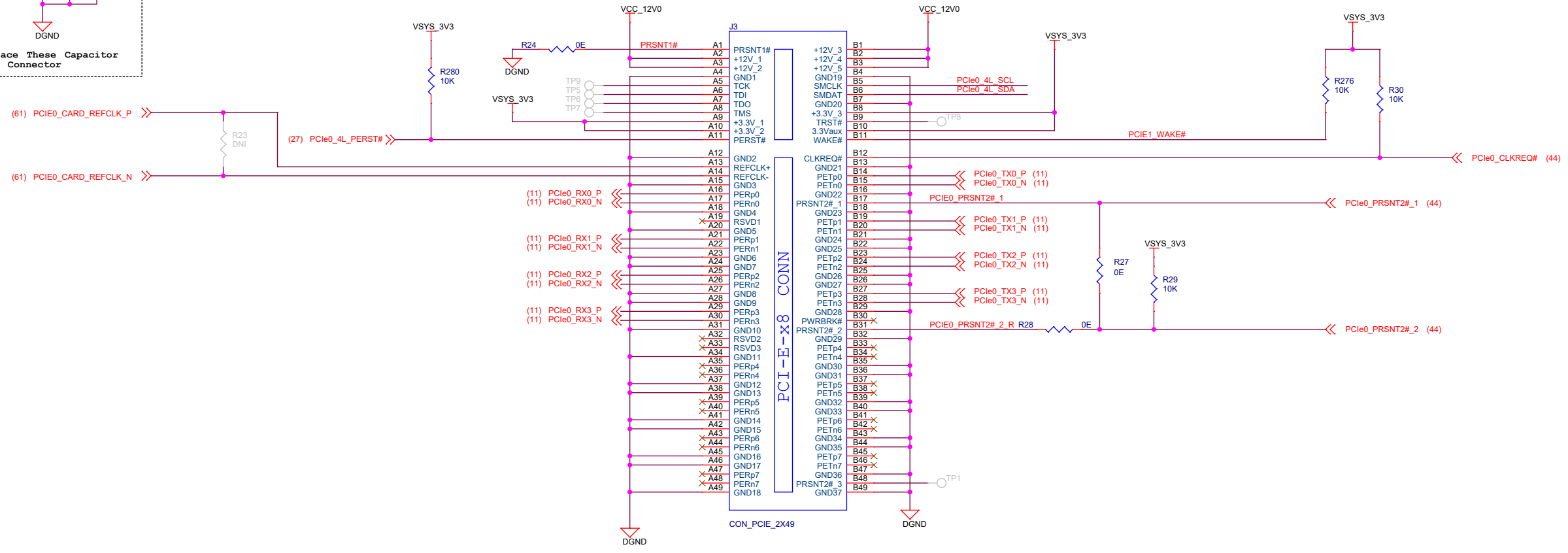
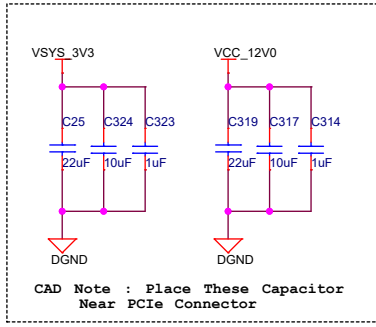


SILKSCREEN: M.2 Key E

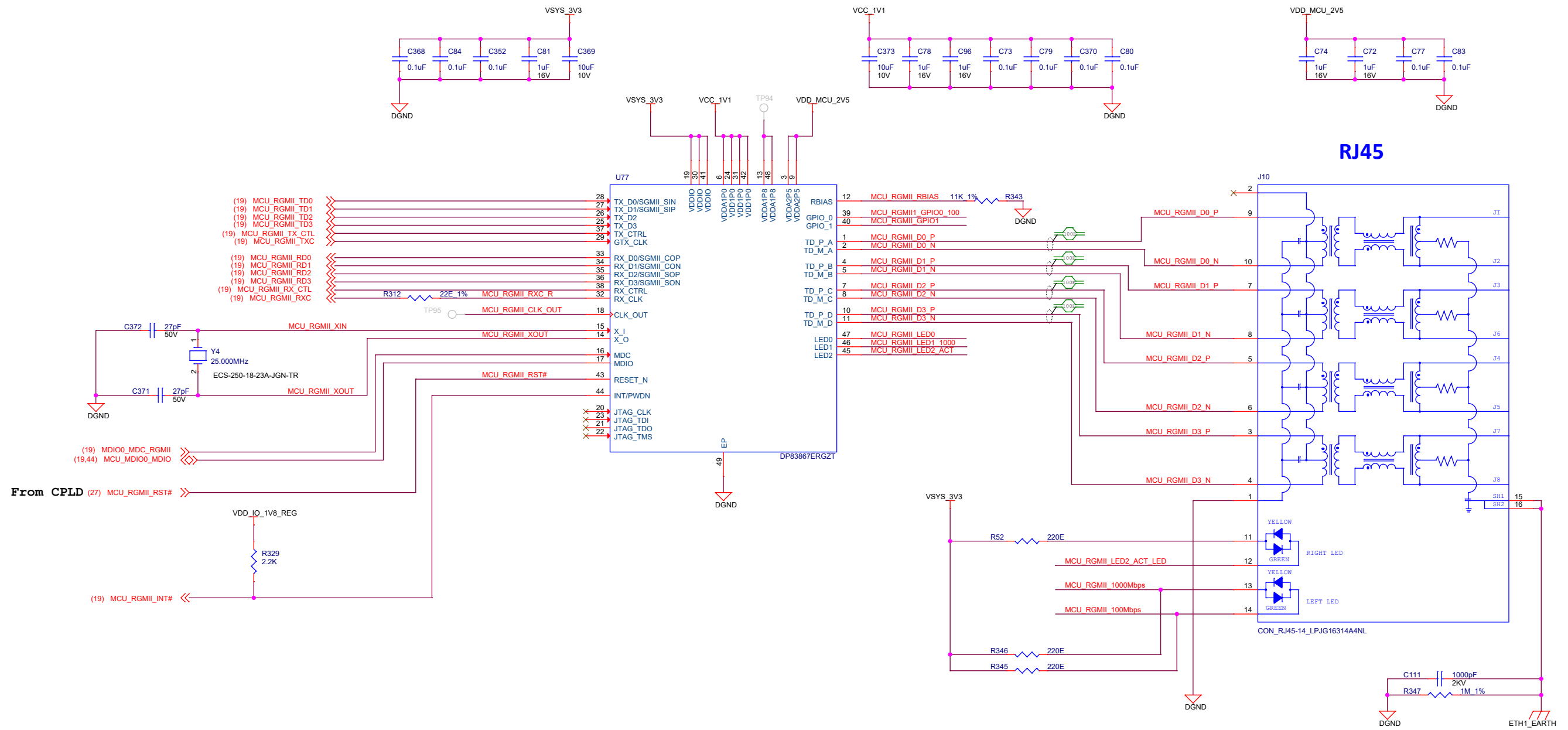
Project :		Title	
AM69 Edge AI Kit		PCIe_M.2_INTERFACE (E Key)	
Size	PROC154E3 001 SK AM69	Rev	E3
C		Date:	Monday, March 20, 2023
		Sheet	36 of 62



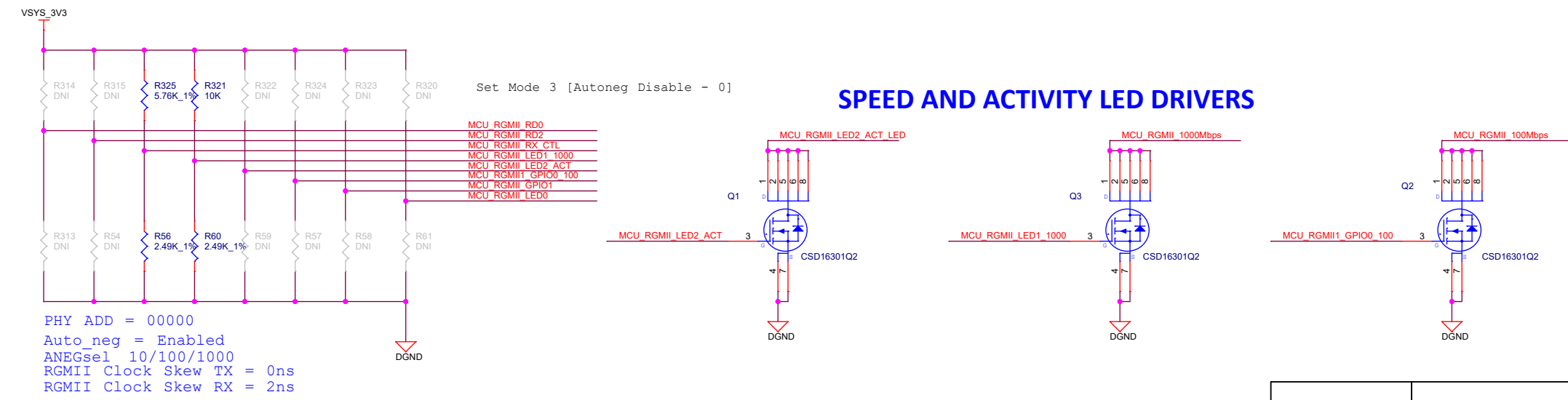
PCIe Card Slot



MCU GB ETHERNET



SPEED AND ACTIVITY LED DRIVERS

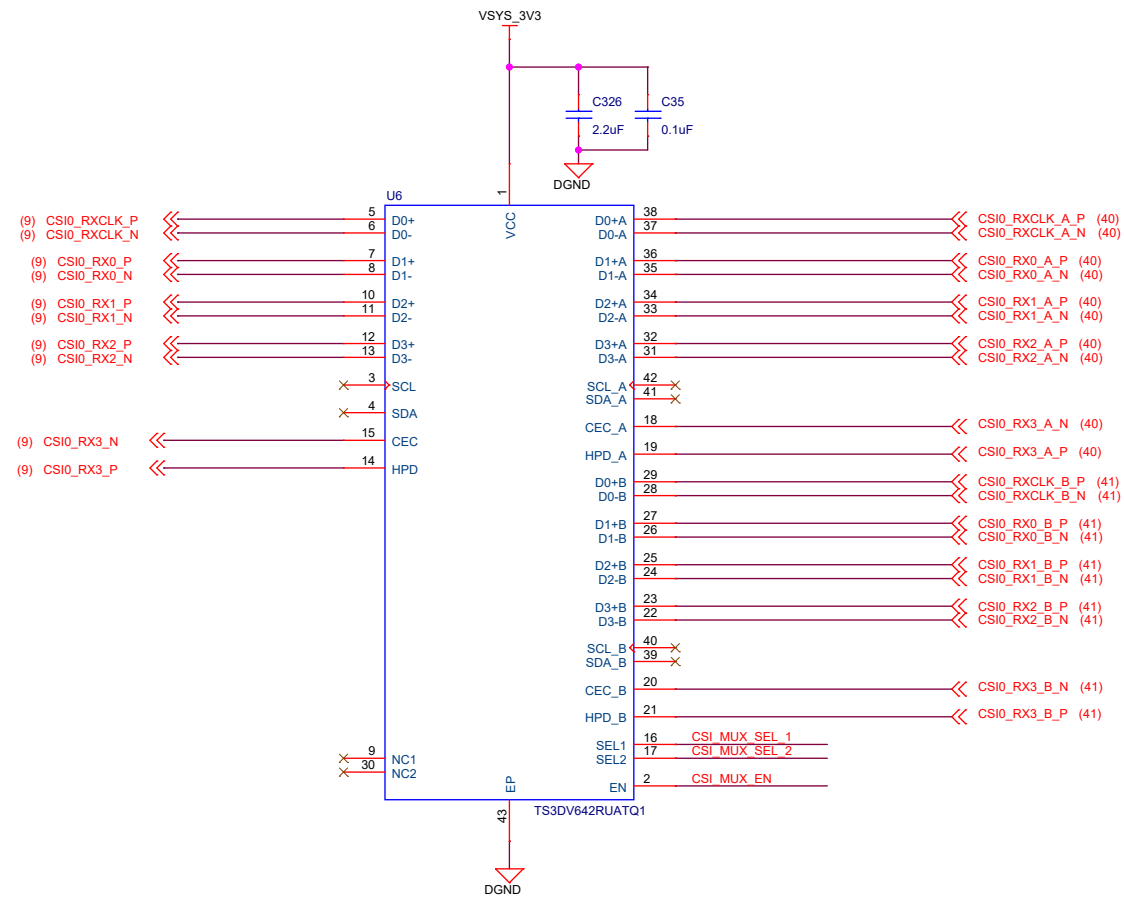


RJ45-LED	FUNCTION
RIGHT - GREEN	ACTIVITY
LEFT - GREEN	1000Mbps Speed
LEFT - YELLOW	100Mbps Speed

LED_2-MODE1 & LED_1-MODE2-TX SKEW=0ns
 GPIO0-MODE1 & GPIO1-MODE1-RX SKEW=2ns

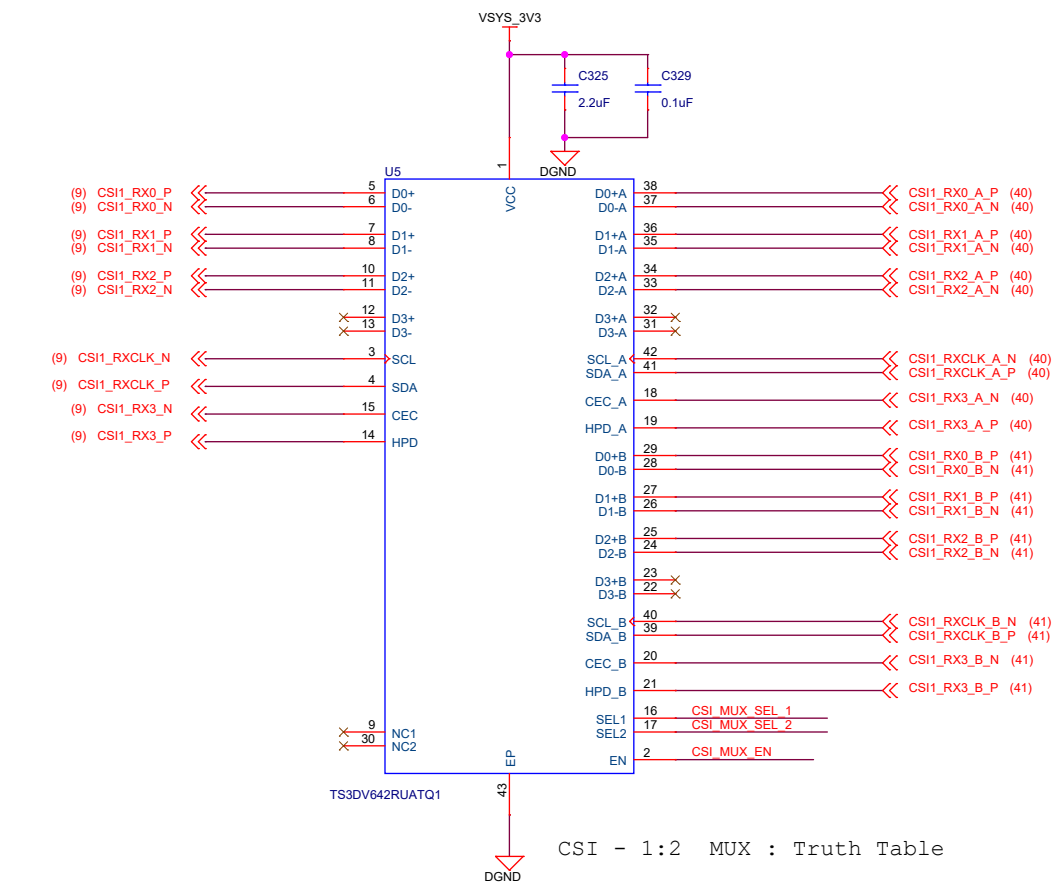
Project : AM69 Edge AI Kit		Title: MCU GB ETHERNET	
		Size: PROC154E3 001 SK AM69	Rev: E3
Date: Thursday, March 30, 2023		Sheet 38 of 62	

CSI MUX - DATA



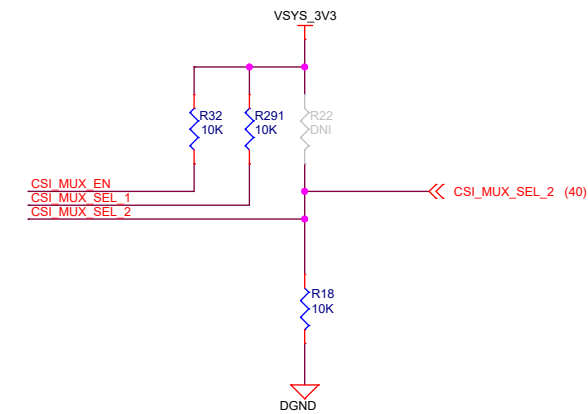
From CSI EXP Conn

From FPC Camera Conn



From CSI EXP Conn

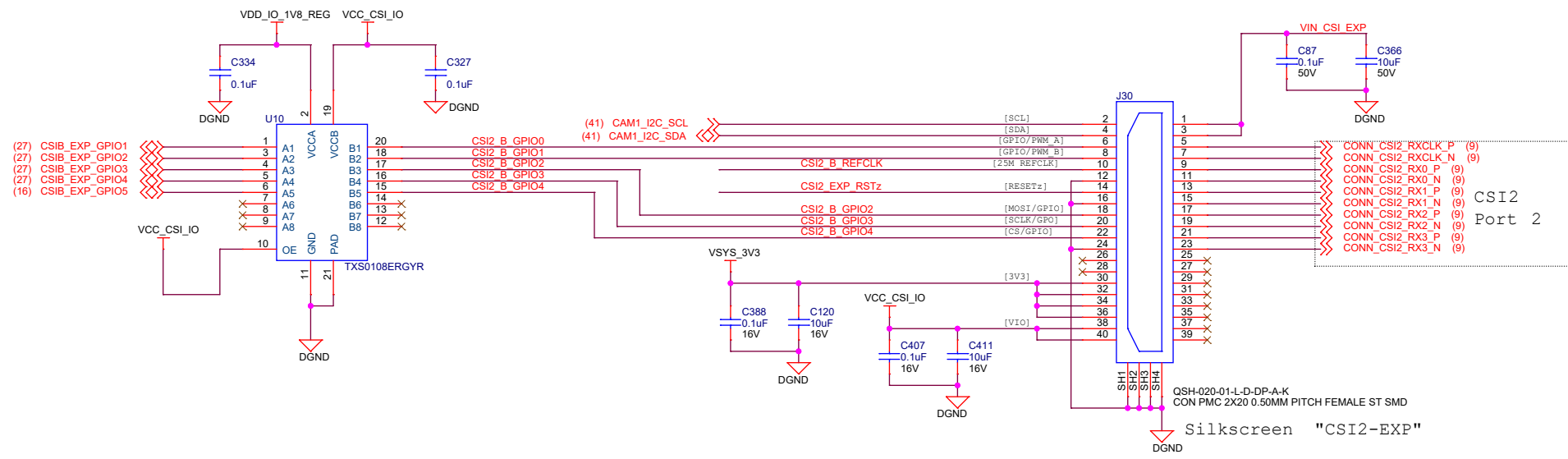
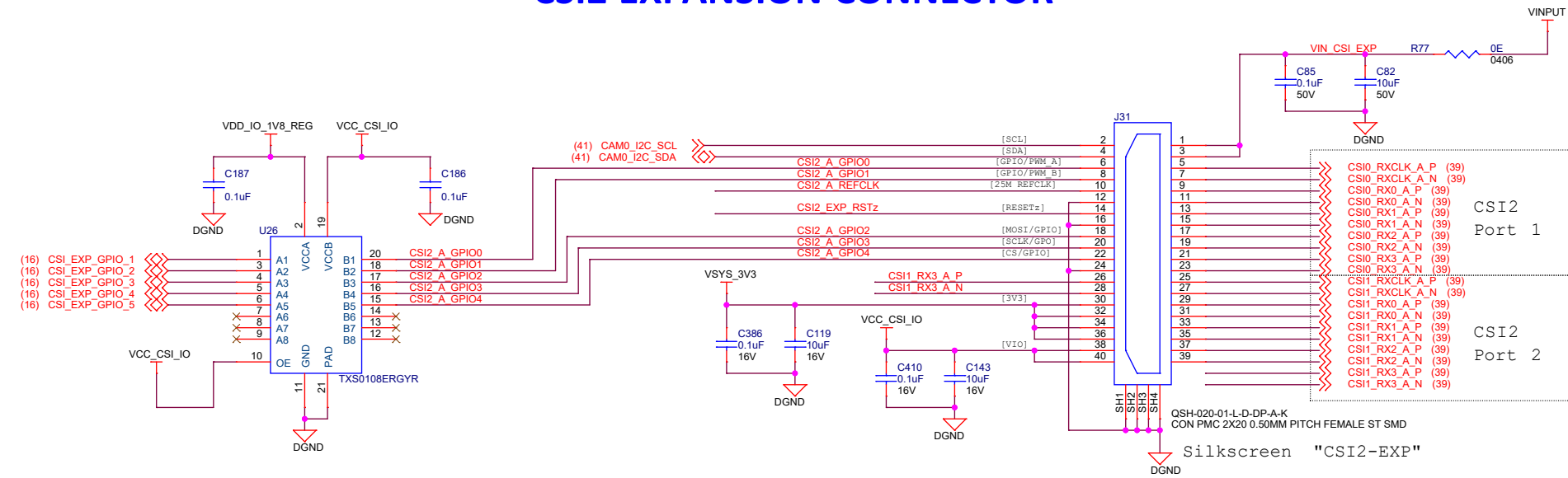
From FPC Camera Conn



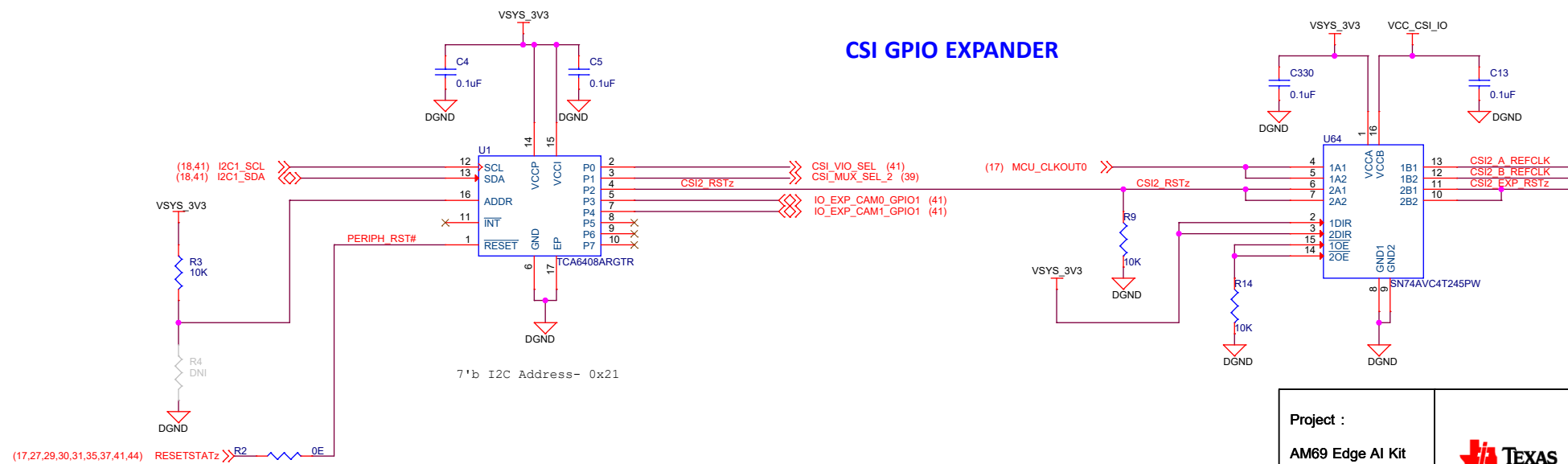
MUX_SEL_2	FUNCTION
LOW	INPUT<-- A Port [CSI2 Connector] (default)
HIGH	INPUT<--B port [FPC Camera Connector]

CSI - 1:2 MUX : Truth Table

CSI2 EXPANSION CONNECTOR



CSI GPIO EXPANDER

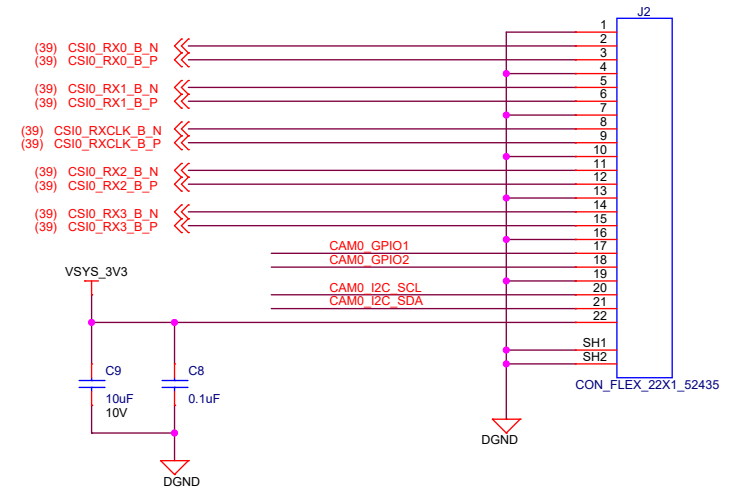
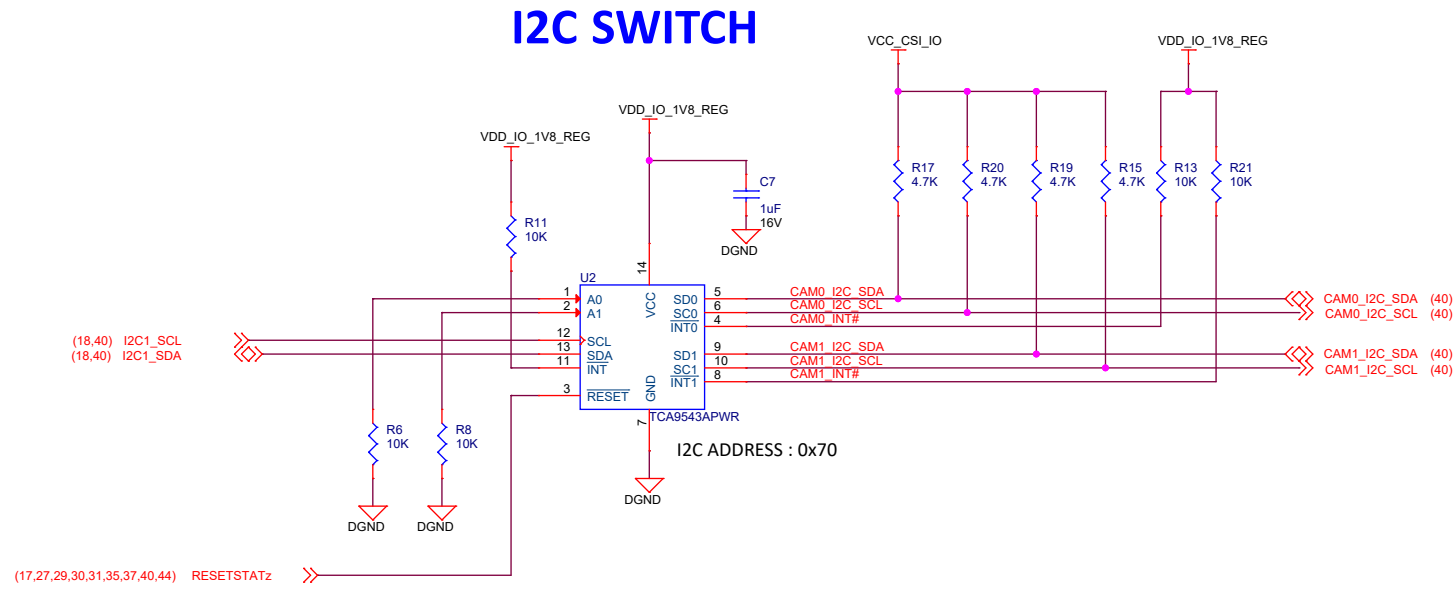


Project :		Title	
AM69 Edge AI Kit		CSI2 EXPANSION CONNECTOR	
Size	PROC154E3 001 SK AM89	Rev	E3
Date:	Monday, March 20, 2023	Sheet	40 of 62



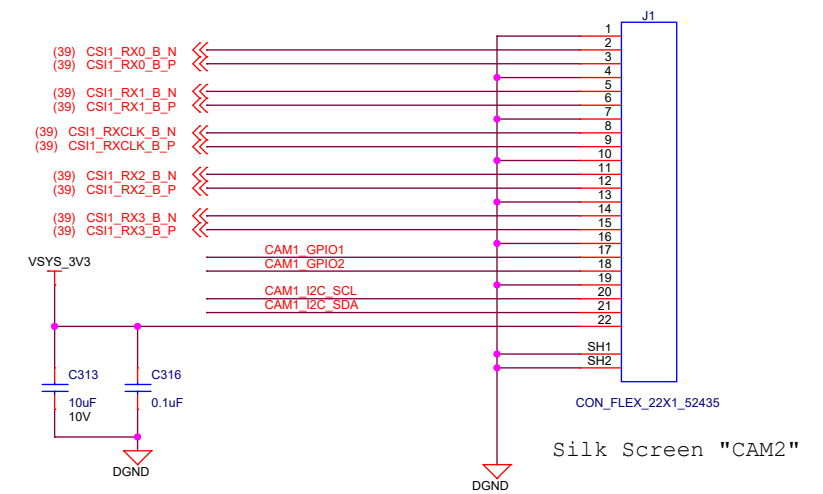
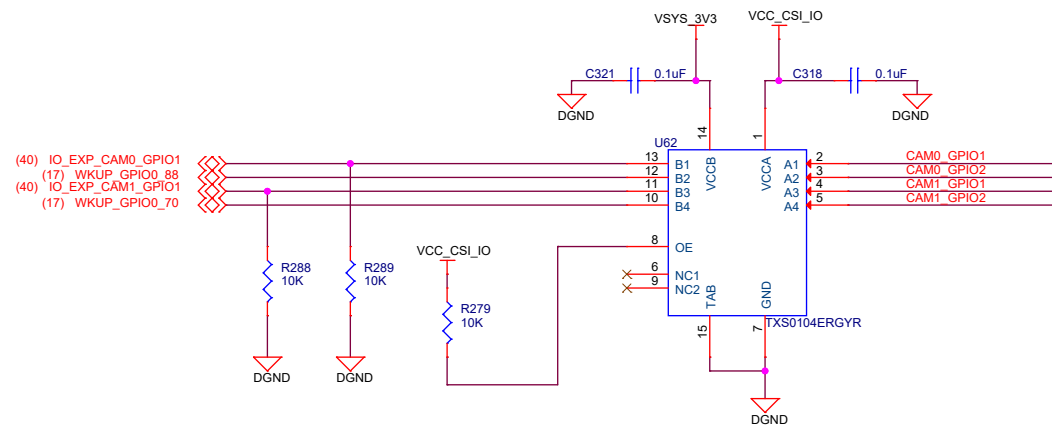
CSI FPC CAMERA CONNECTORS

Silk Screen "CAM1"
FPC Camera Connector -1

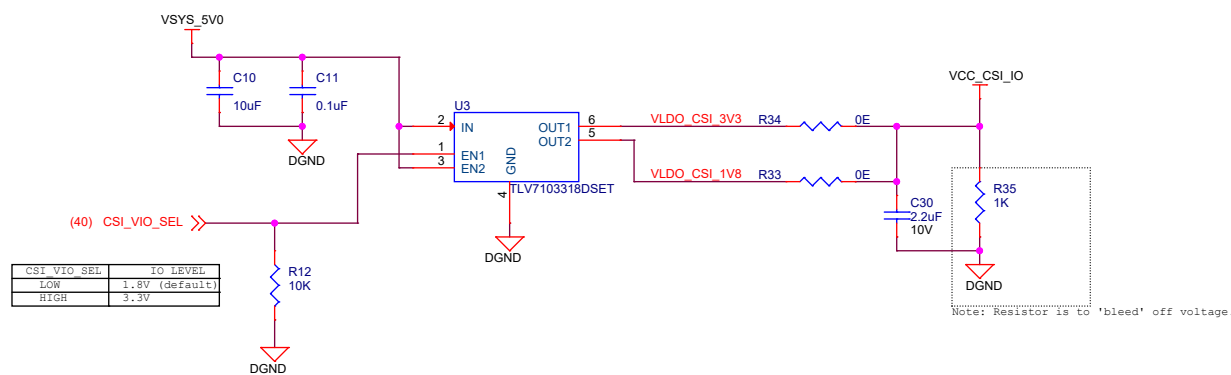


GPIO LEVEL TRANSLATOR

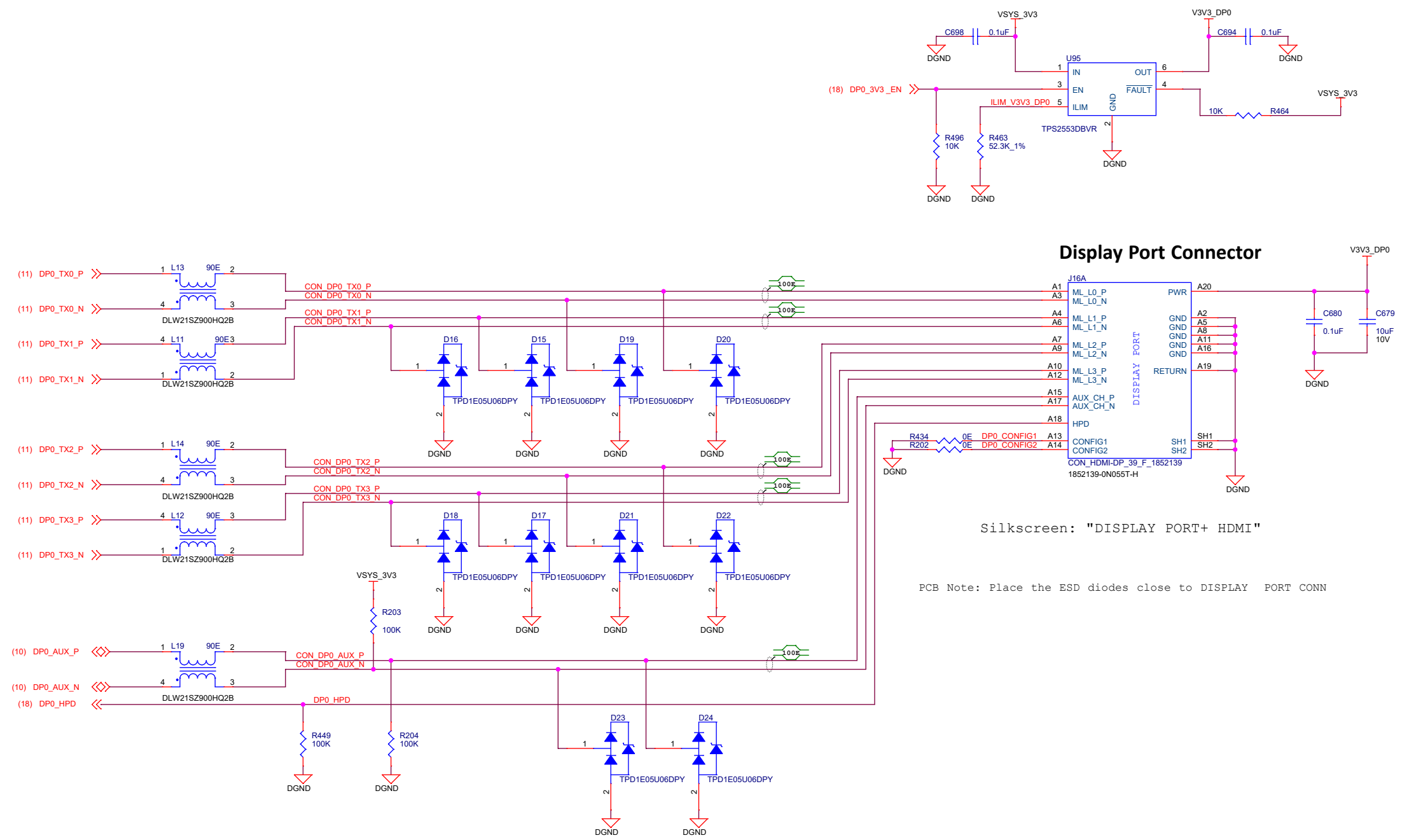
FPC Camera Connector -2



CAMERA IO SUPPLY

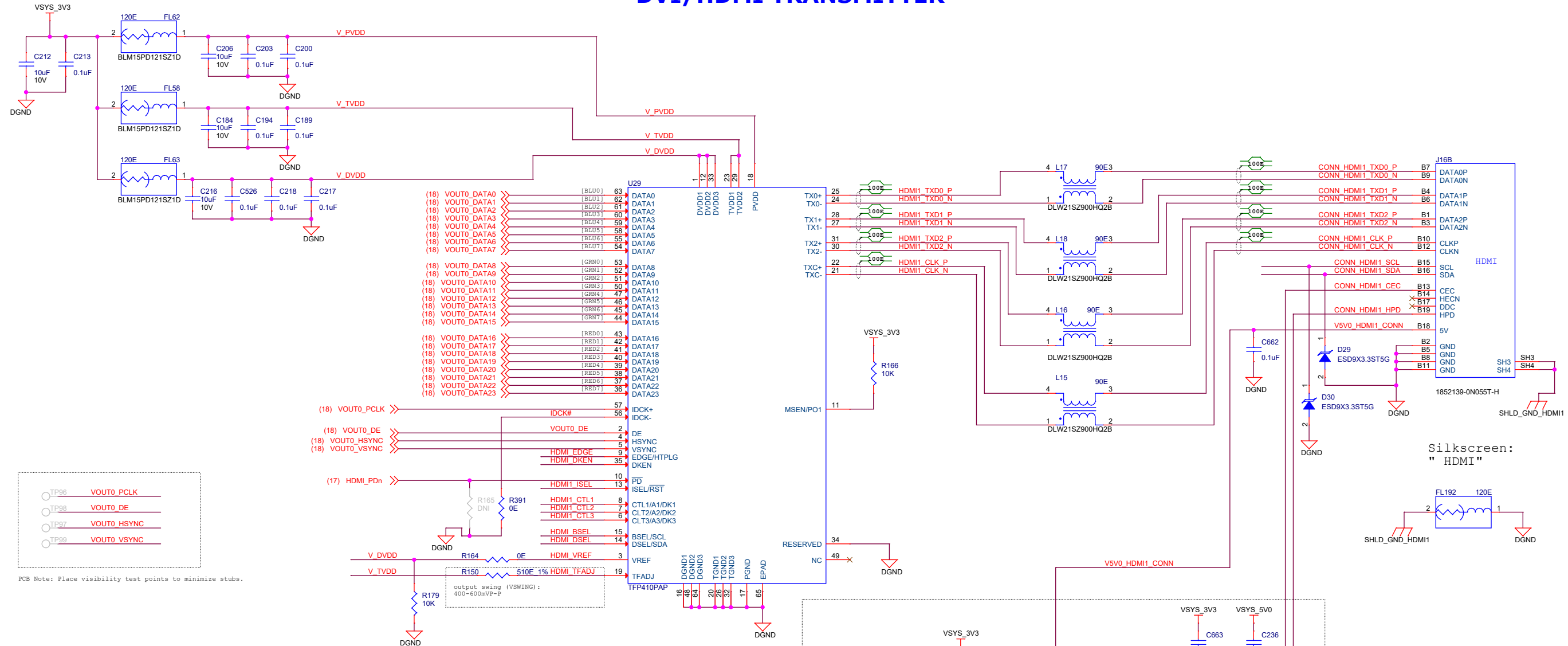


DISPLAY PORT INTERFACE



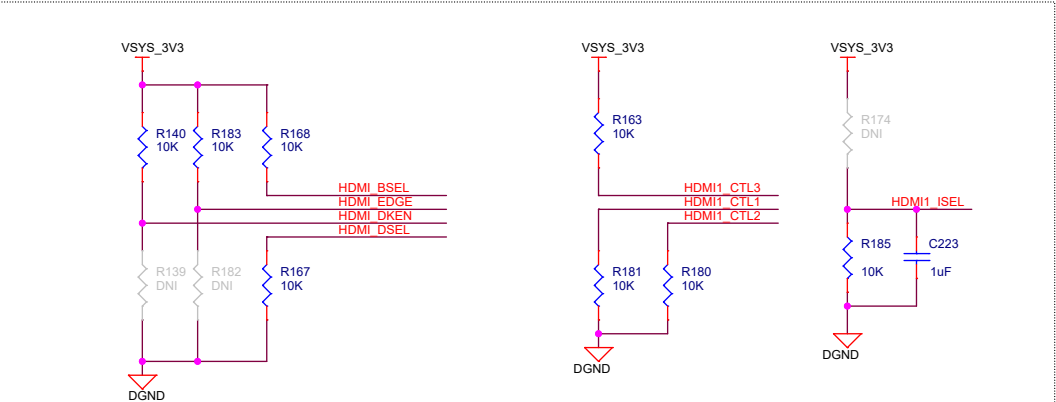
Project :		Title									
AM69 Edge AI Kit		DISPLAY_PORT_INTERFACE									
		<table border="1"> <tr> <td>Size</td> <td>PROC154E3 001 SK AM69</td> <td>Rev</td> <td></td> </tr> <tr> <td>C</td> <td></td> <td>E3</td> <td></td> </tr> </table>		Size	PROC154E3 001 SK AM69	Rev		C		E3	
Size	PROC154E3 001 SK AM69	Rev									
C		E3									
Date: Monday, March 20, 2023		Sheet 42 of 62									

DVI/HDMI TRANSMITTER



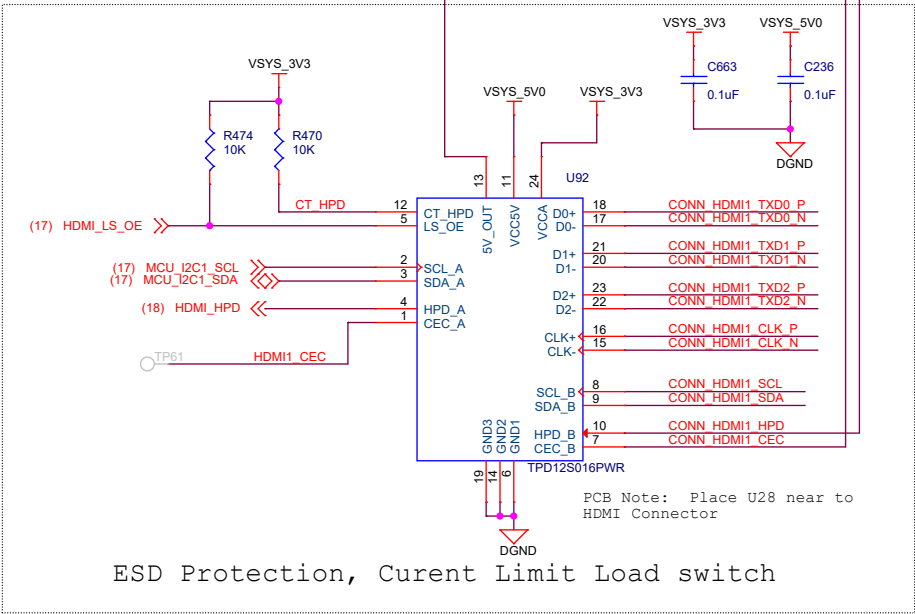
PCB Note: Place visibility test points to minimize stubs.

DVI Configuration Settings



VREF	BSEL	EDGE	DSEL	BUS WIDTH	LATCH MODE	CLOCK MODE	CLOCK EDGE
0.55V-0.9V	1	0	0	24-bit	Single-ended	Falling	Single-ended
Default	1	1	0	24-bit	Single-ended	Raising	Single-ended

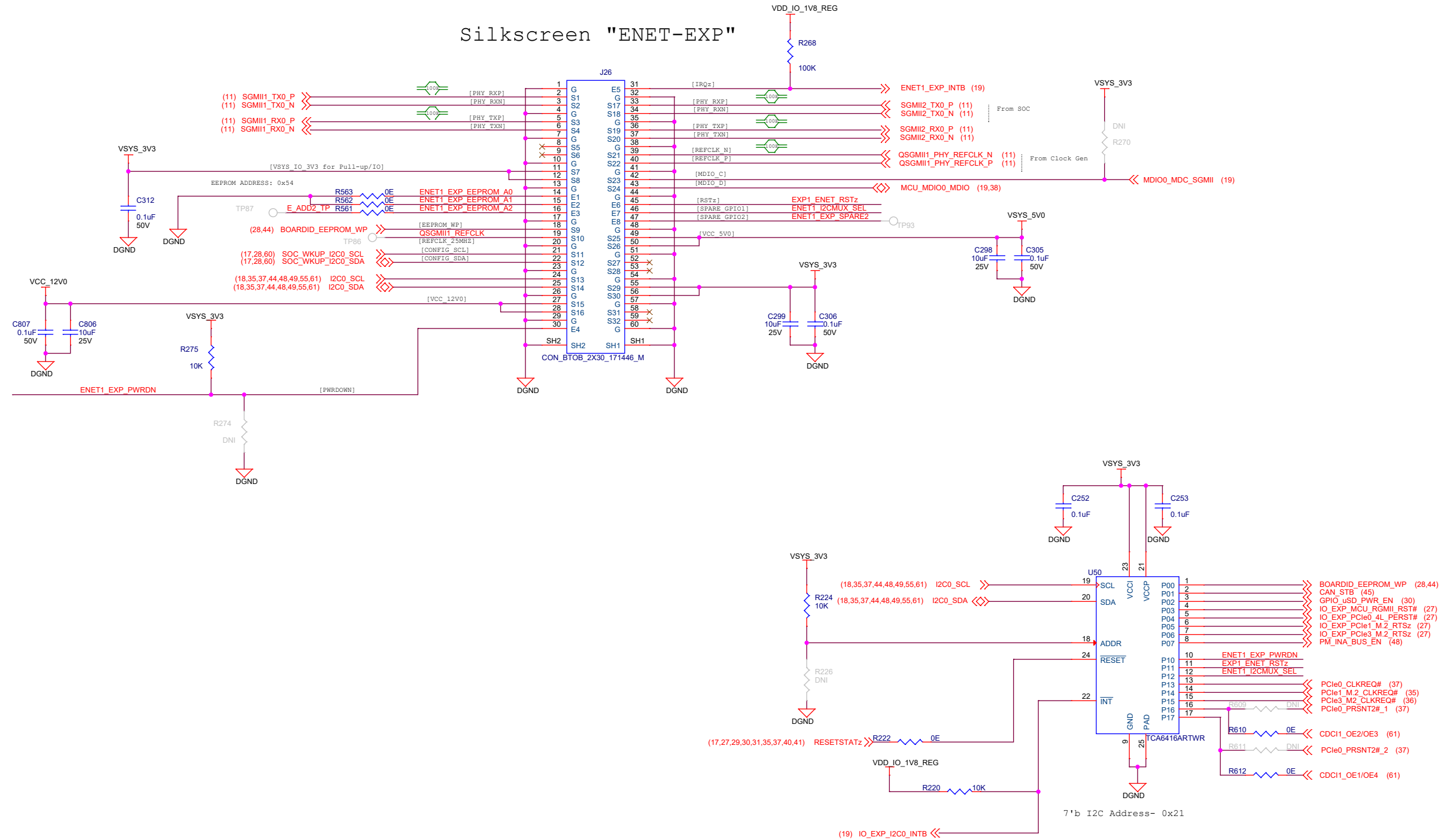
ISEL:- Low (default): I2C interface is disabled and chip configuration is specified by BSEL, DSEL, EDGE, VREF pins
 When ISEL: L, DSEL-H- enables de-skew function (default)



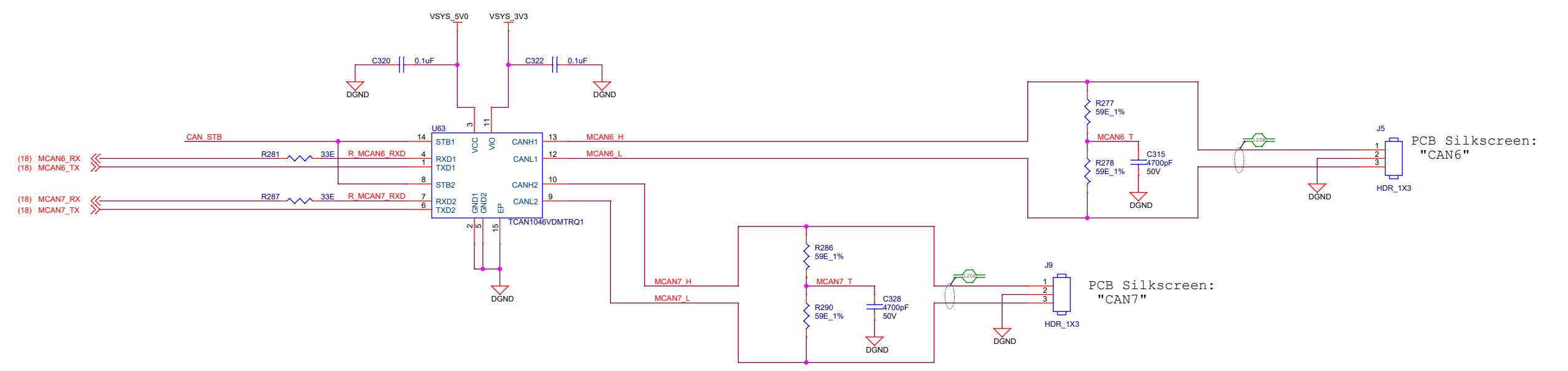
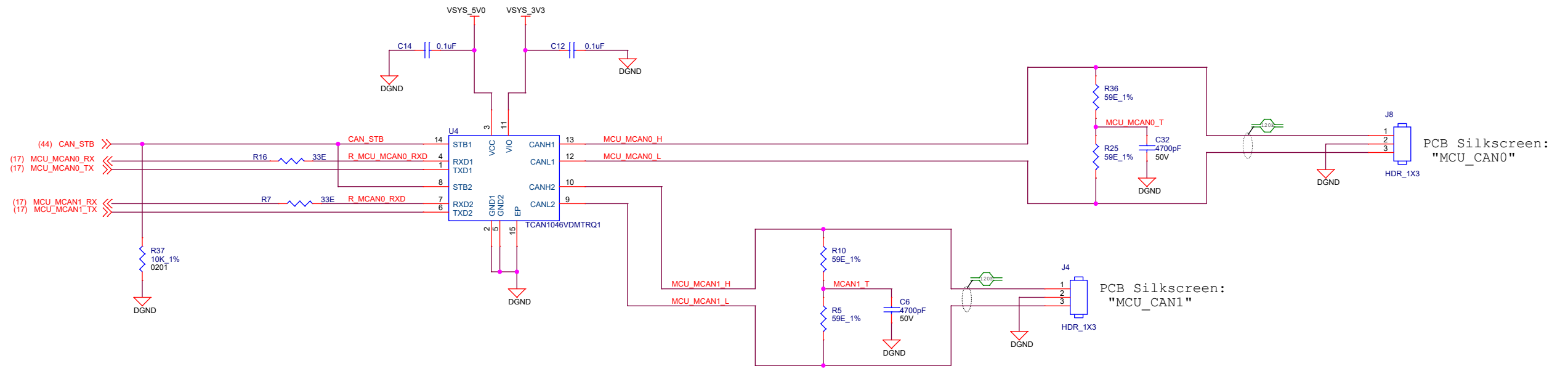
ESD Protection, Current Limit Load switch

ENET EXPANSION CONNECTOR

Silkscreen "ENET-EXP"

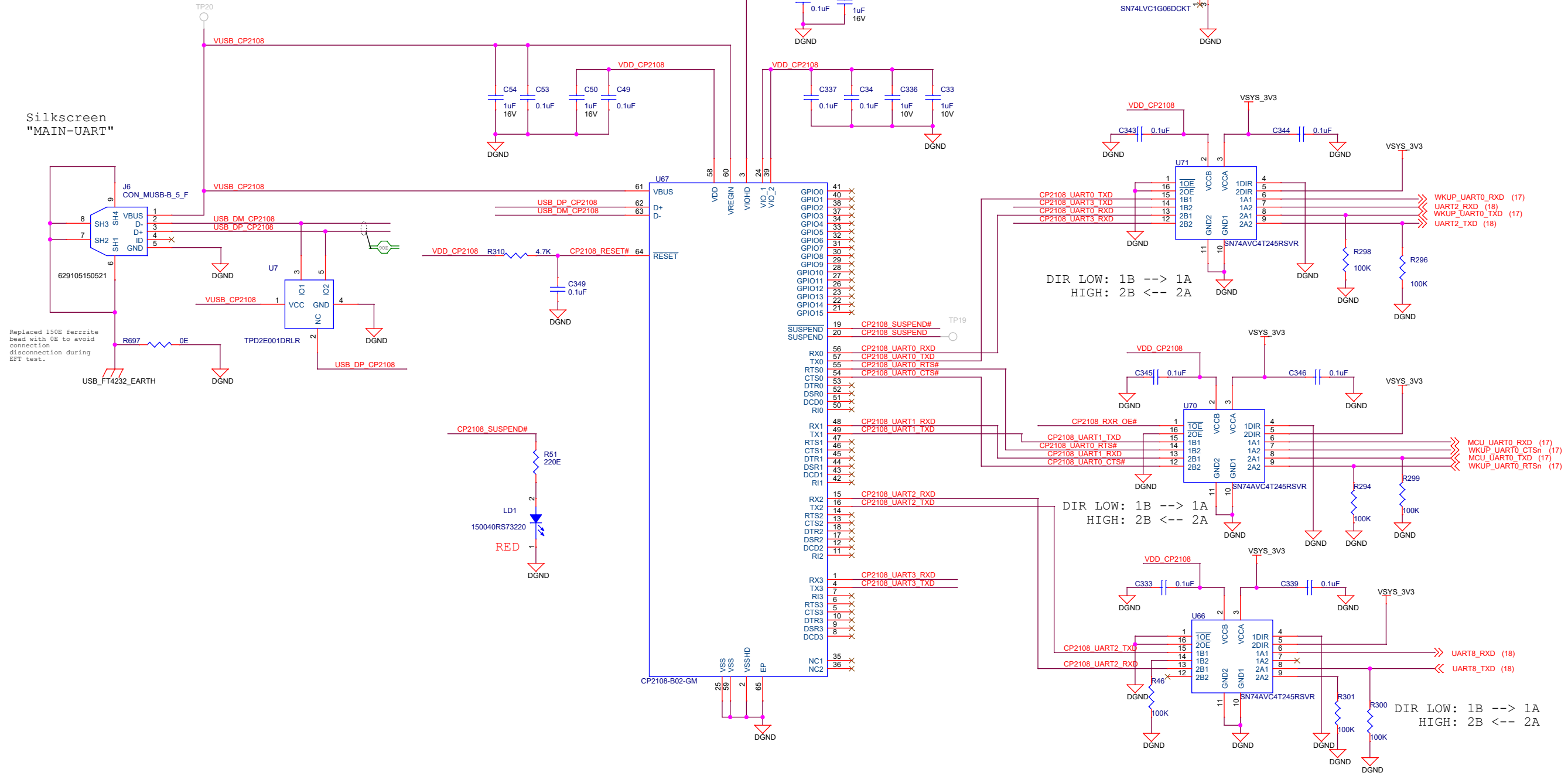


CAN TRANSCEIVERS



QUAD PORT CONSOLE

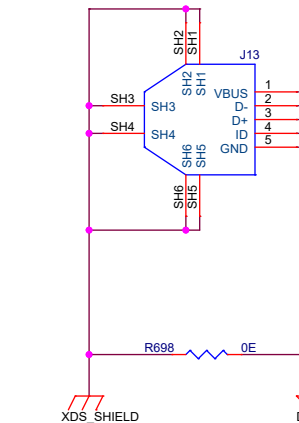
Silkscreen
"MAIN-UART"



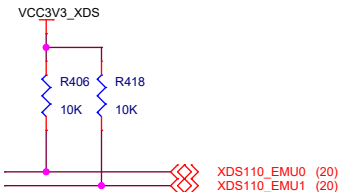
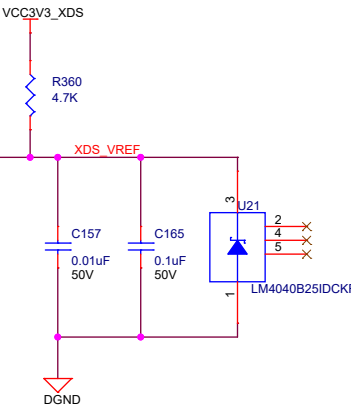
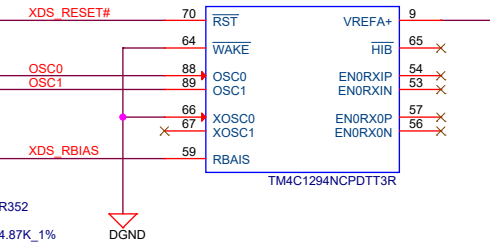
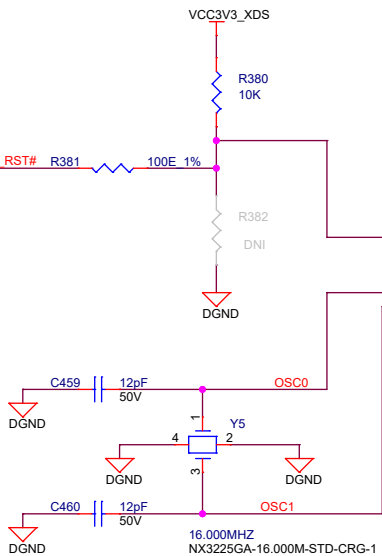
XDS110 DEBUGGER

Silkscreen "XDS110"

1051640001
CON MICRO USB-B TYPE 5POS FEMALE RT SMD



(26,48) TA_POWERDOWNz	0E	R439	0201	XDS_TA_POWERDOWNz
(27,48) TA_PORZ	0E	R444	0201	XDS_TA_PORZn
(27,48) TA_RESETz	0E	R448	0201	XDS_TA_RESETz
(19,48) TA_SOC_INT1z	0E	R454	0201	XDS_TA_SOC_INT1z
(19,48) TA_SOC_INT2z	0E	R480	0201	XDS_TA_SOC_INT2z
(48) TA_BOOTMODE_CNTL#	0E	R467	0201	XDS_TA_BOOTMODE_CNTL#
(27,48) TA_BM_IOEXP_RSTn	0E	R473	0201	XDS_TA_BM_IOEXP_RSTn

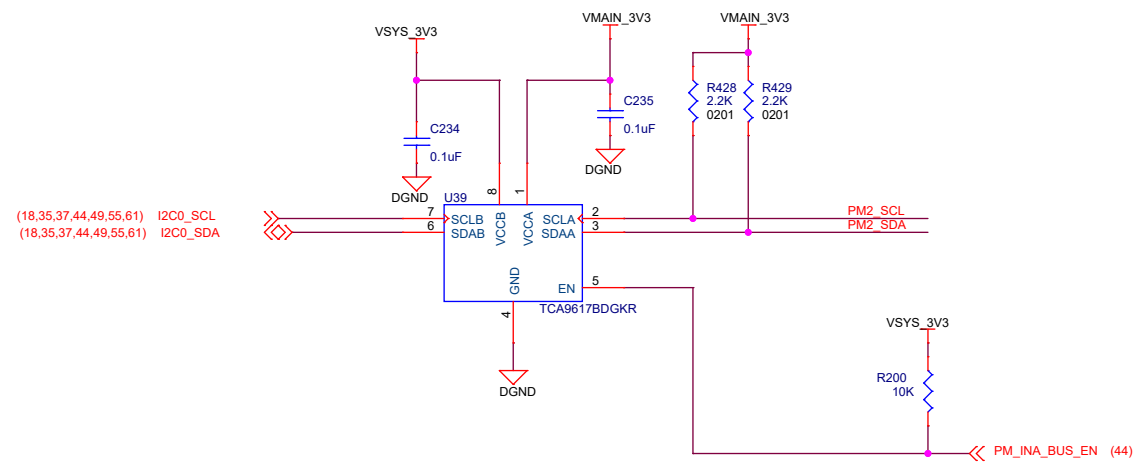
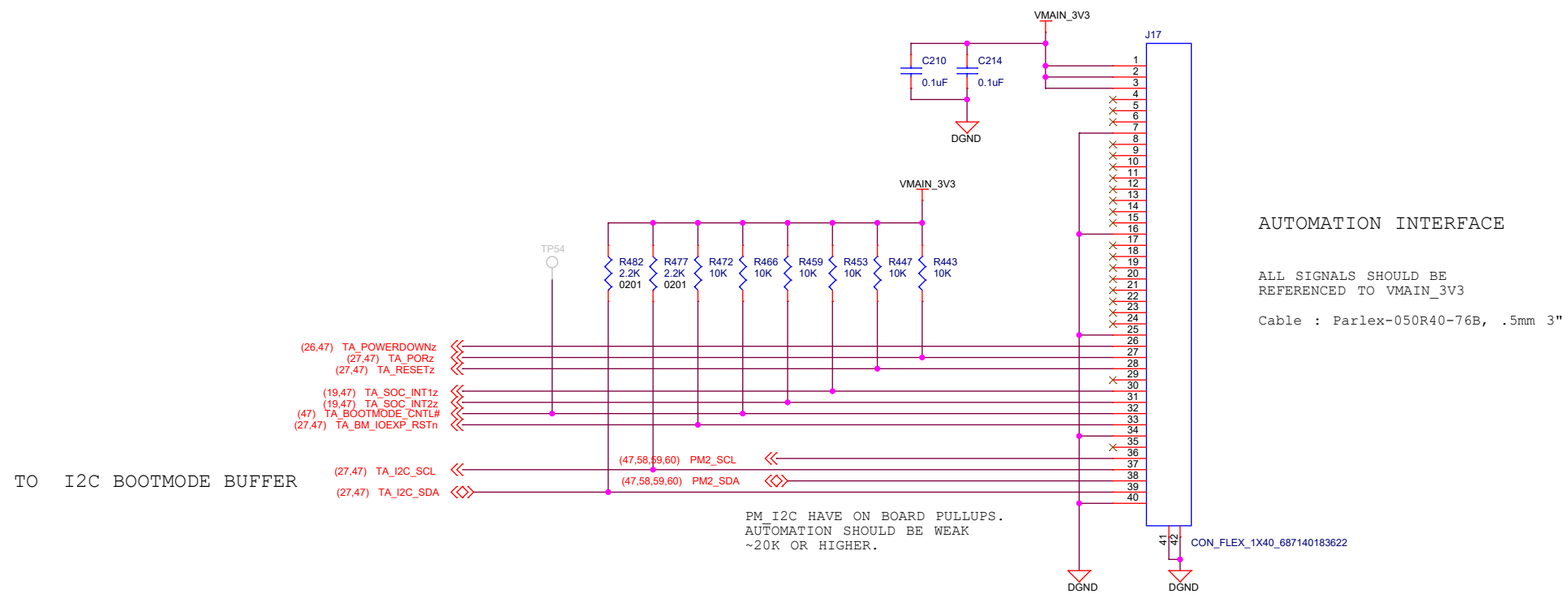


(20) XDS110_TCK	33	PA0/U0RX	100	PC0/TCK/SWCLK
(20) XDS110_TMS	34	PA1/U0TX	99	PC1/TMS/SWDIO
(20) XDS110_TMS	35	PA2/SSIOCLK	98	PC2/TDI
(20) XDS110_TDO	36	PA3/SSIOFSS	97	PC3/TDO/SWO
(20) XDS110_TDI	37	PA4/SSIOXDAT0	96	PC4/C1-
(20) XDS110_TDI	38	PA5/SSIOXDAT1	95	PC5/C1+
(20) XDS110_TRST#	39	PA6	94	PC6/CO+
	40	PA7	93	PC7/CO-
	41	PA7	92	
	42	PE0/AIN3	42	XDS110_EMU0
	43	PE1/AIN2	43	XDS110_EMU1
	44	PE2/AIN1	44	
	45	PE3/AIN0	45	
	46	PE4/AIN9	46	
	47	PE5/AIN8	47	
	48	PG0	48	XDS PM1_SCL
	49	PG1	49	XDS PM1_SDA
	50	PJ0	50	
	51	PJ1	51	
	52	PL0	52	XDS PM2_SDA
	53	PL1	53	XDS PM2_SCL
	54	PL2	54	
	55	PL3	55	
	56	PL4	56	
	57	PL5	57	
	58	PL6/USB0DP	58	XDS USB D P
	59	PL7/USB0DM	59	XDS USB D N
	60	PN0	60	
	61	PN1	61	
	62	PN2	62	
	63	PN3	63	
	64	PN4	64	
	65	PN5	65	
	66	PQ0	66	
	67	PQ1	67	
	68	PQ2	68	
	69	PQ3	69	
	70	PQ4	70	
	71	PP0/C2+	71	XDS110_EMU0 (20)
	72	PP1/C2-	72	XDS110_EMU1 (20)
	73	PP2	73	
	74	PP3	74	
	75	PP4	75	
	76	PP5	76	

Set the unique ID of the debugger

Project : AM69 Edge AI Kit		Title : XDS110 DEBUGGER	
Size : C	PROC154E3 001 SK AM69	Date : Wednesday, March 29, 2023	Rev : E3
		Sheet : 47	of : 62

TEST AUTOMATION HEADER

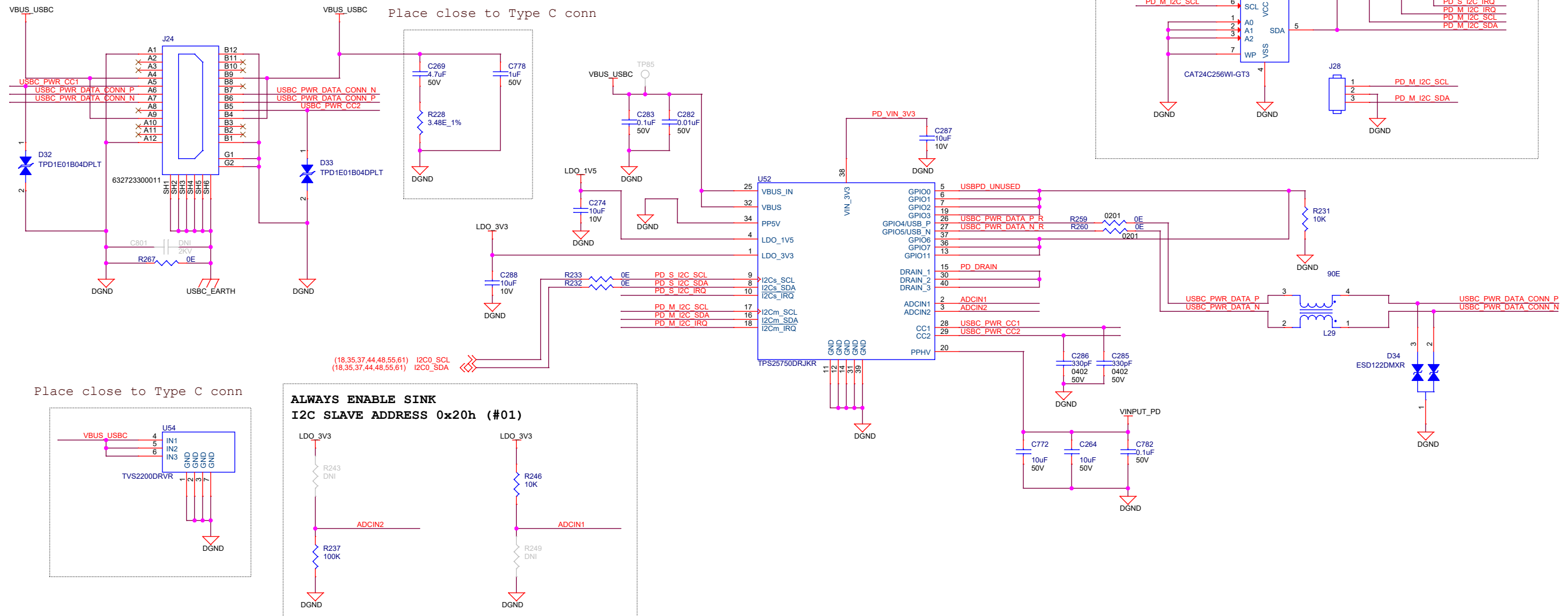
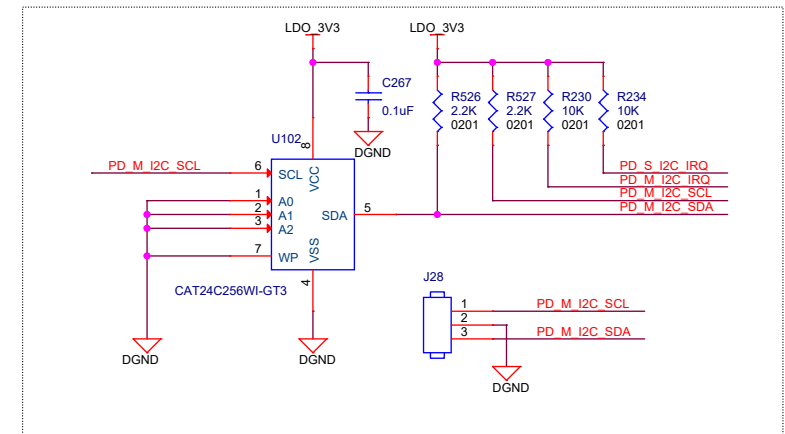


TEST AUTOMATION GPIO MAPPING

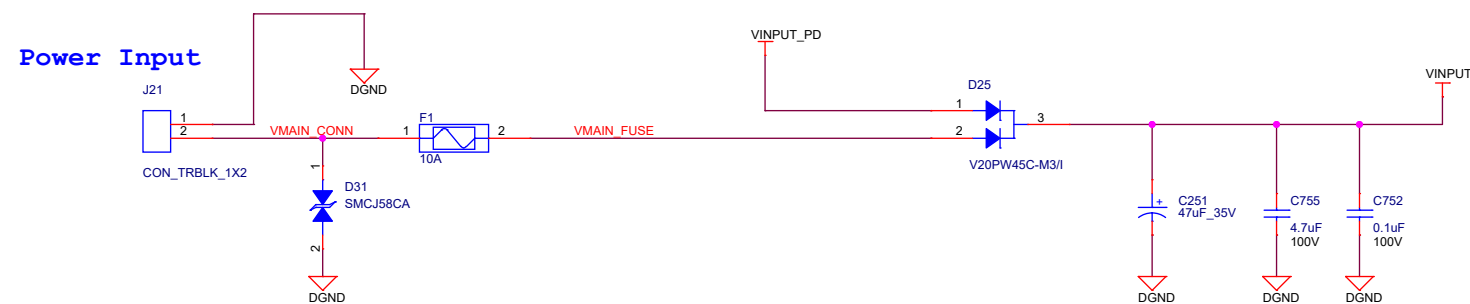
SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/External PU/PD states
TA_POWERDOWN	Used to Power down the system	OUTPUT	External Pullup
TA_PORzn	MCU & Main SoC domain Power ON Reset	OUTPUT	External Pullup
TA_RESETz	SoC Warmreset	OUTPUT	External Pullup
TA_SOC_INT1z	Interrupt to SOC	OUTPUT	External Pullup
TA_SOC_INT2z	Interrupt to SOC	OUTPUT	External Pullup
TA_BM_IOEXP_RSTn	Used to Reset the Bootmode IO Expander	OUTPUT	External Pullup

USB-C Power

EEPROM & PROGRAMMING HEADER

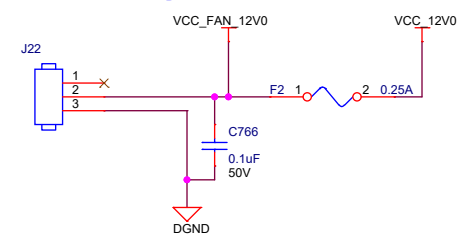


OPTIONAL POWER INPUT



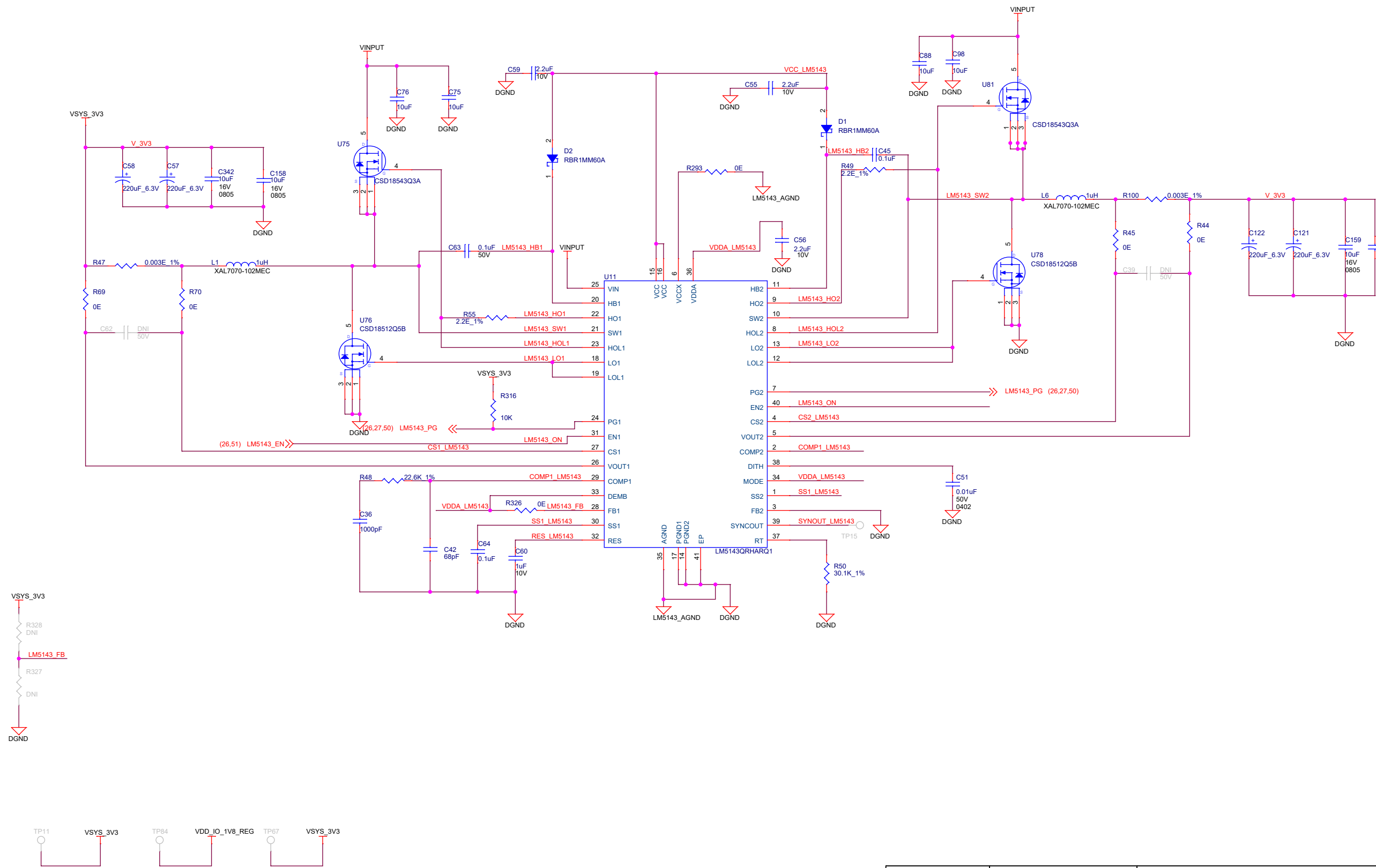
Normal operation Range for VINPUT 20V to 25V.
SILK: POWER IN

Cooling FAN Header



POWER SUPPLY #1

TI WEBENCH Simulation Inputs:
 Vin (min) = 15V Vin (max) = 25V
 Vout = 3.3V@30A
 Ta = 25 deg

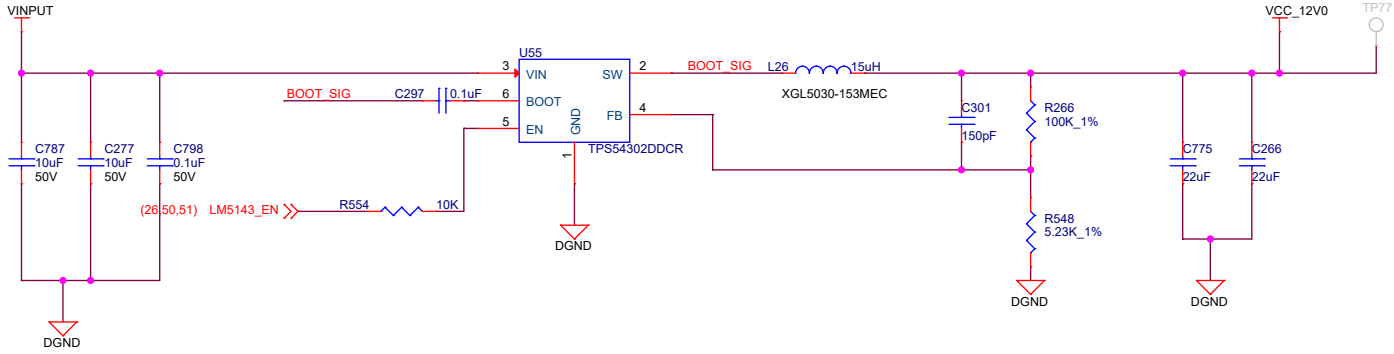


Project :		Title POWER SUPPLY #1	
AM69 Edge AI Kit		Size	Rev
		C	E3
		Date: Tuesday, March 21, 2023	Sheet 50 of 62

POWER SUPPLY #2

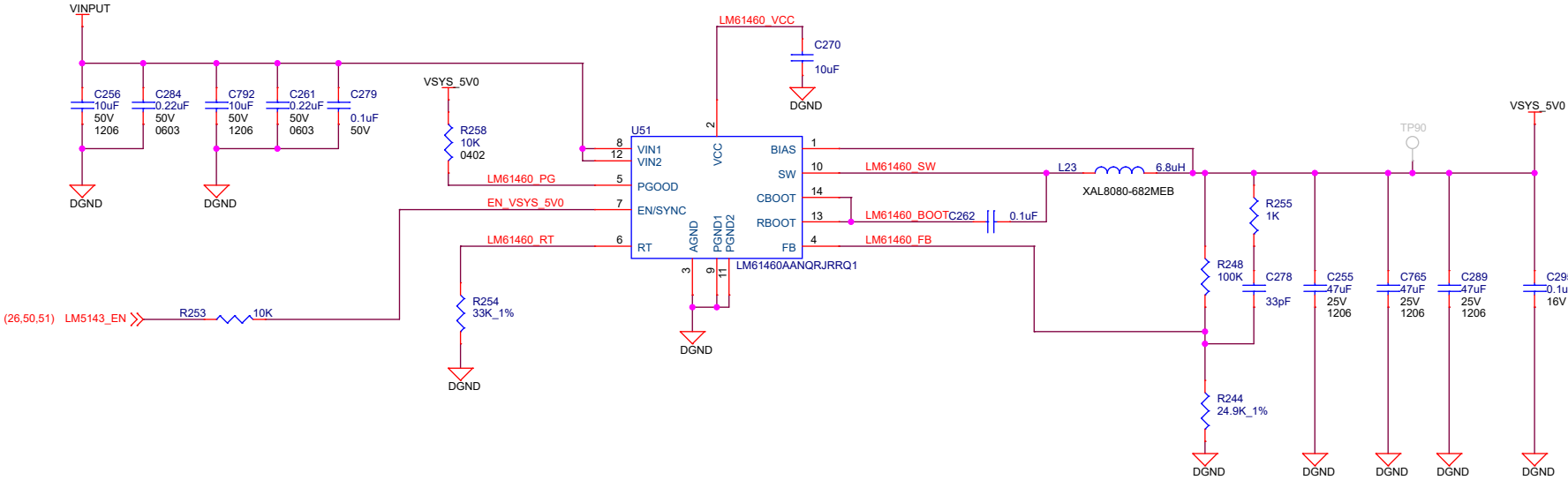
TI WEBENCH Simulation Inputs:
 Vin (min) = 15V Vin (max) = 25V
 Vout = 12V@3A
 Ta = 25 deg

12V GENERATION



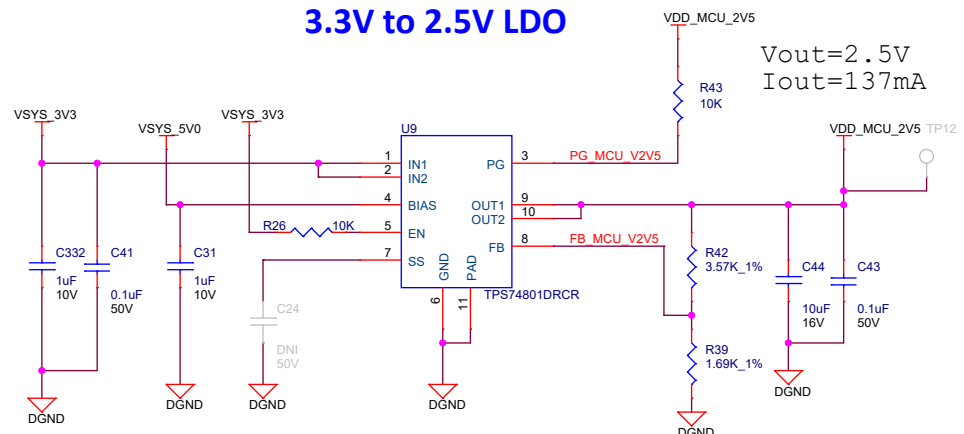
LM61460 5V BUCK REGULATOR
 VinMin = 12V
 VinMax = 25V
 Vout = 5.0V
 Iout = 6A

5V GENERATION

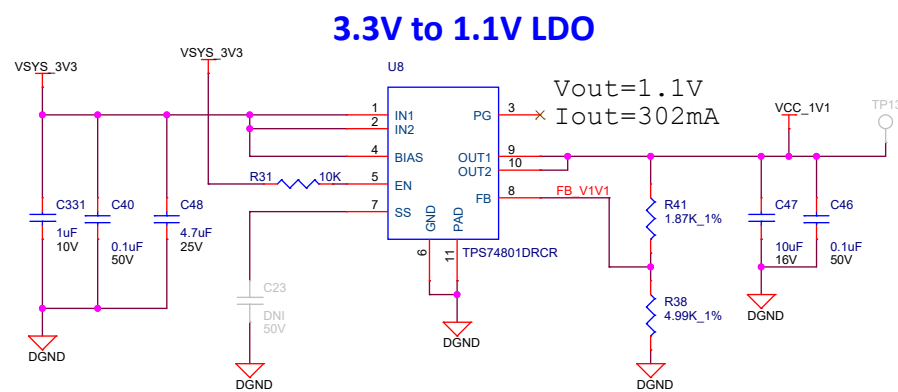


POWER SUPPLY #3

ETHERNET POWER- MCU RGMII

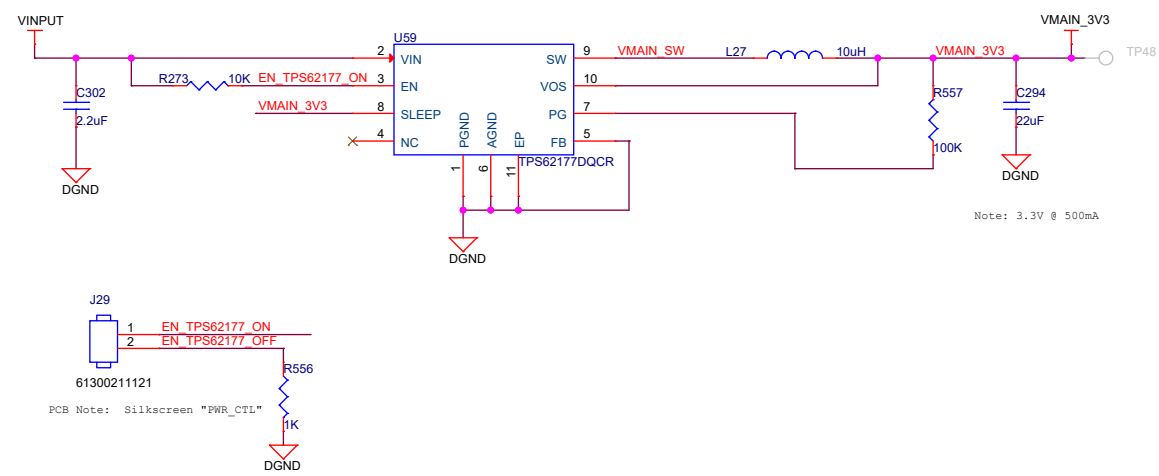


USB HUB POWER & ETHERNET POWER - RGMII1



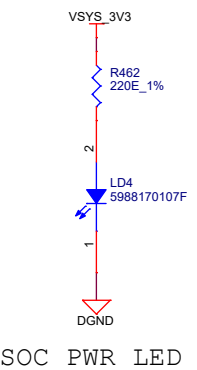
PCB NOTE: Keep 4.7uF capacitor close to BIAS pin

SYSTEM MANAGEMENT 3.3V REGULATOR



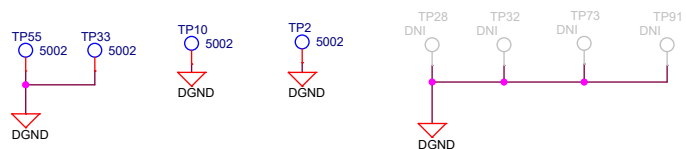
Note: 3.3V @ 500mA

POWER INDICATION LED'S



SOC PWR LED

GROUND TEST POINTS



PCB NOTE: Spread the SMD test points Top and Bottom Side of PCB

Project : AM69 Edge AI Kit		Title POWER SUPPLY #3	
		Size C	Rev E3
Date: Monday, March 20, 2023		Sheet 52 of 62	

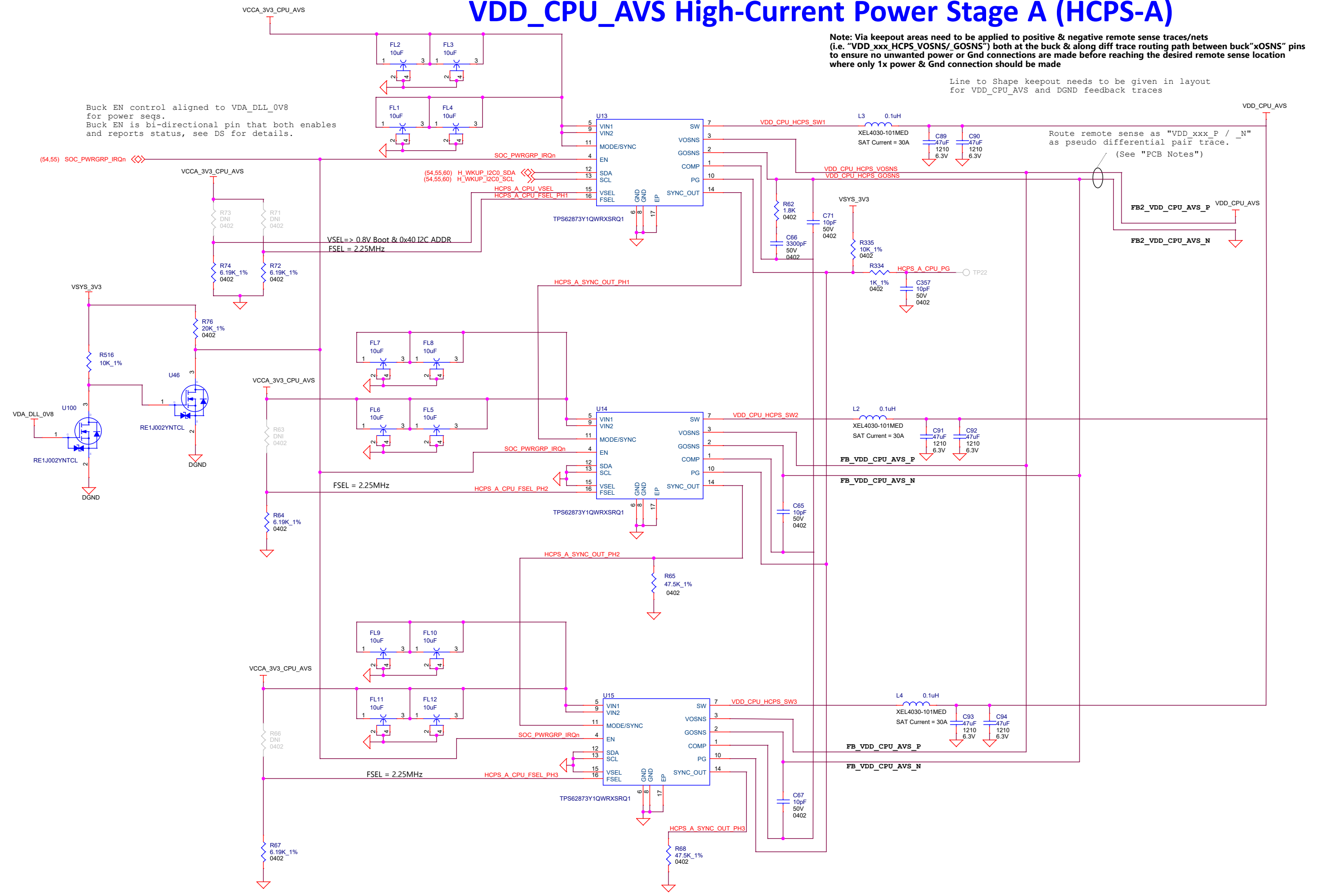
VDD_CPU_AVS High-Current Power Stage A (HCPS-A)

Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "VDD_XXX_HCPS_VOSNS/ GOSNS") both at the buck & along diff trace routing path between buck "xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

Line to Shape keepout needs to be given in layout for VDD_CPU_AVS and DGND feedback traces

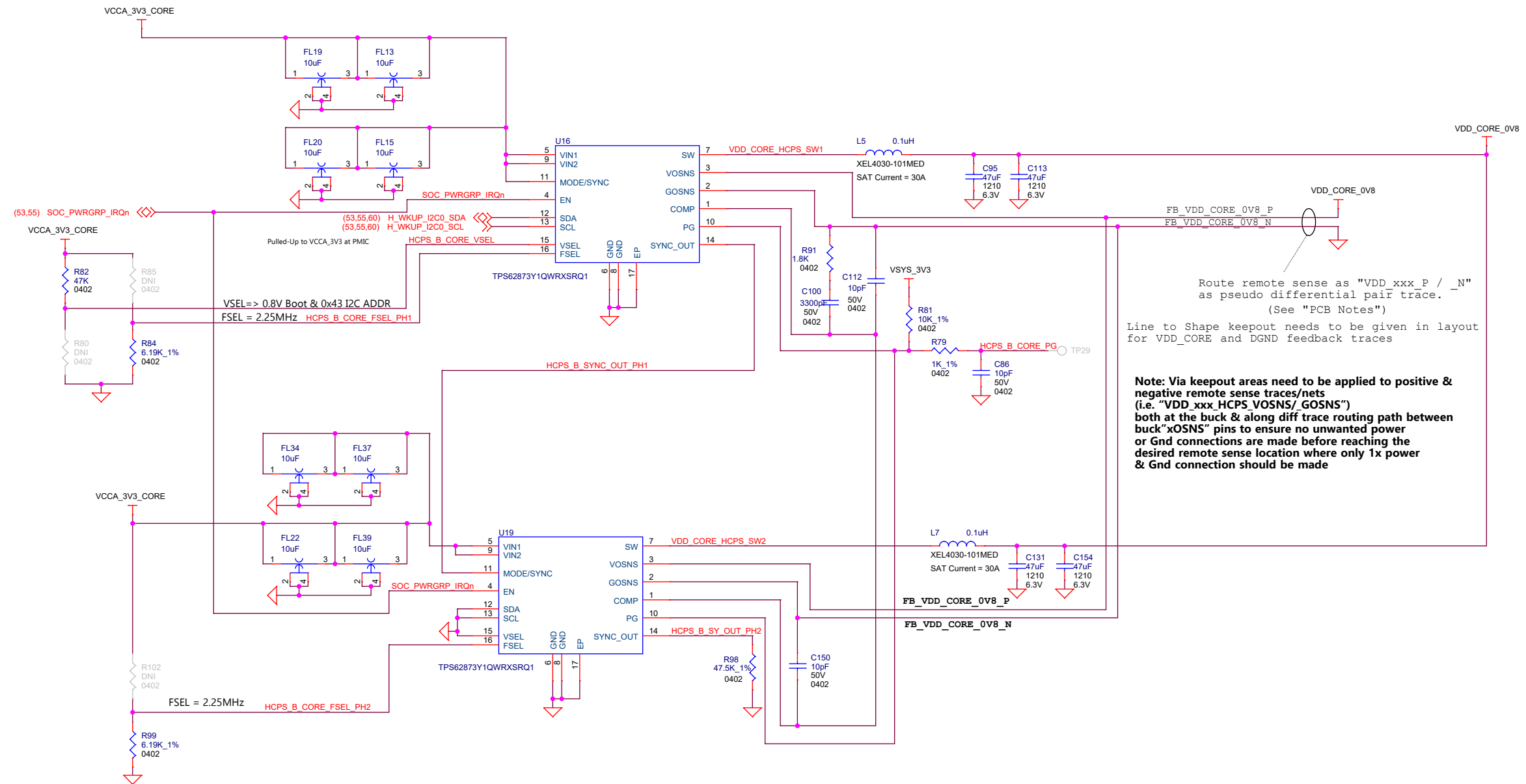
Buck EN control aligned to VDA_DLL_0V8 for power seqs.
Buck EN is bi-directional pin that both enables and reports status, see DS for details.

Route remote sense as "VDD_XXX_P / _N" as pseudo differential pair trace.
(See "PCB Notes")



Project : AM69 Edge AI Kit			Title: HCPS A - VDD CPU	
			Size: PROC154E3 001 SK AM69	Rev: E3
		Date: Monday, March 20, 2023	Sheet 53 of 62	

VDD_CORE_0V8 High-Current Power Stage A (HCPS-B)



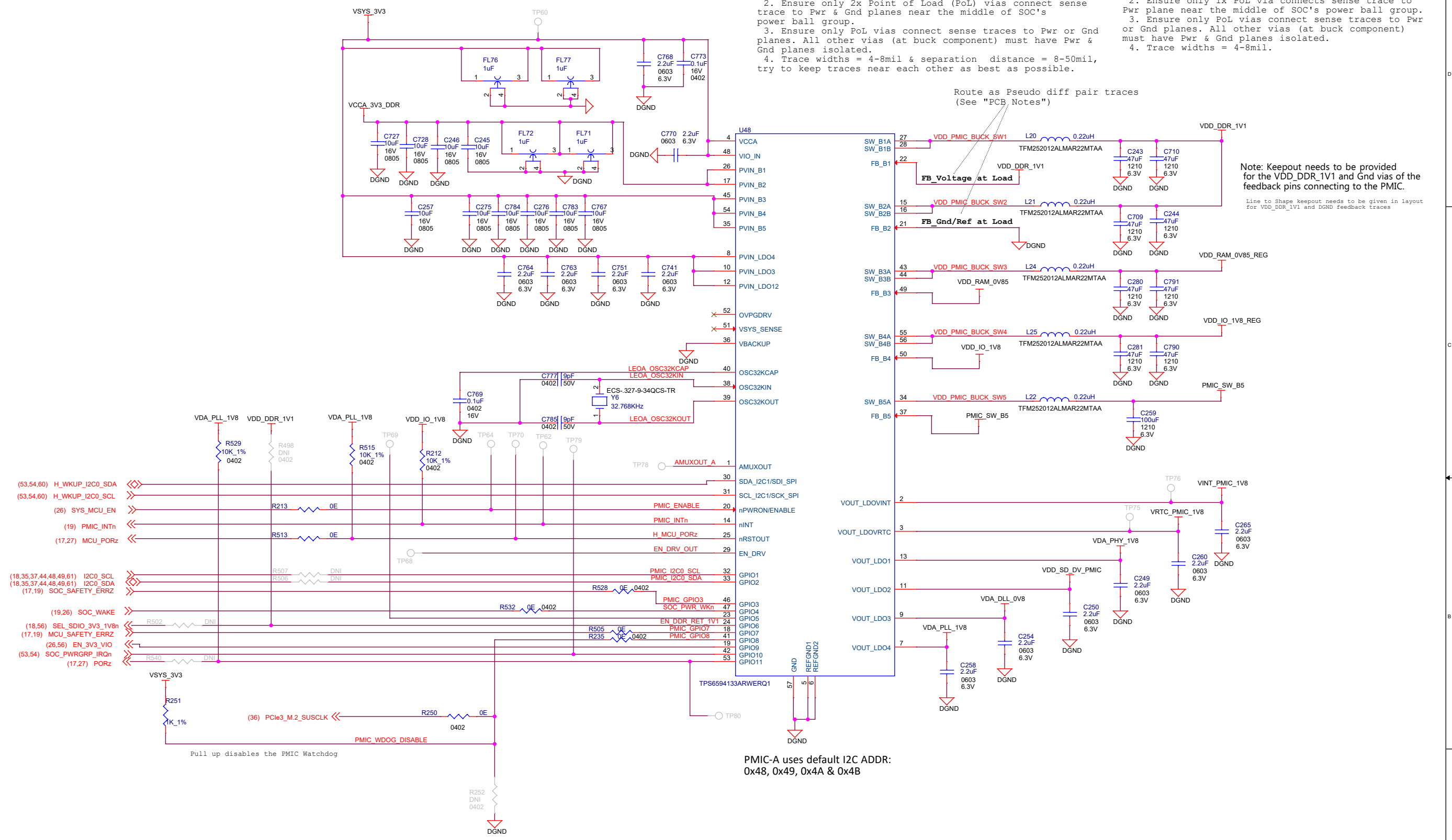
Route remote sense as "VDD xxx P / _N" as pseudo differential pair trace. (See "PCB Notes")
Line to Shape keepout needs to be given in layout for VDD_CORE and DGND feedback traces

Note: Via keepout areas need to be applied to positive & negative remote sense traces/nets (i.e. "VDD xxx HCPS_VOSNS/_GOSNS") both at the buck & along diff trace routing path between buck "xOSNS" pins to ensure no unwanted power or Gnd connections are made before reaching the desired remote sense location where only 1x power & Gnd connection should be made

PMIC

"PCB Notes":
 For multi-phase Buck converter configs, route remote sense feedback as follows:
 1. Use pseudo differential pair traces on same layer & next to primarily power plane segment. Avoid routing near to any noisy/switching signals.
 2. Ensure only 2x Point of Load (PoL) vias connect sense trace to Pwr & Gnd planes near the middle of SOC's power ball group.
 3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
 4. Trace widths = 4-8mil & separation distance = 8-50mil, try to keep traces near each other as best as possible.

For single-phase Buck converter configs, route remote sense feedback as follows:
 1. Use single-ended traces on same layer & next to primarily power plane segment as best as possible. Avoid routing near to any noisy/switching signals.
 2. Ensure only 1x PoL via connects sense trace to Pwr plane near the middle of SOC's power ball group.
 3. Ensure only PoL vias connect sense traces to Pwr or Gnd planes. All other vias (at buck component) must have Pwr & Gnd planes isolated.
 4. Trace widths = 4-8mil.



Note: Keptout needs to be provided for the VDD_DDR_1V1 and Gnd vias of the feedback pins connecting to the PMIC.

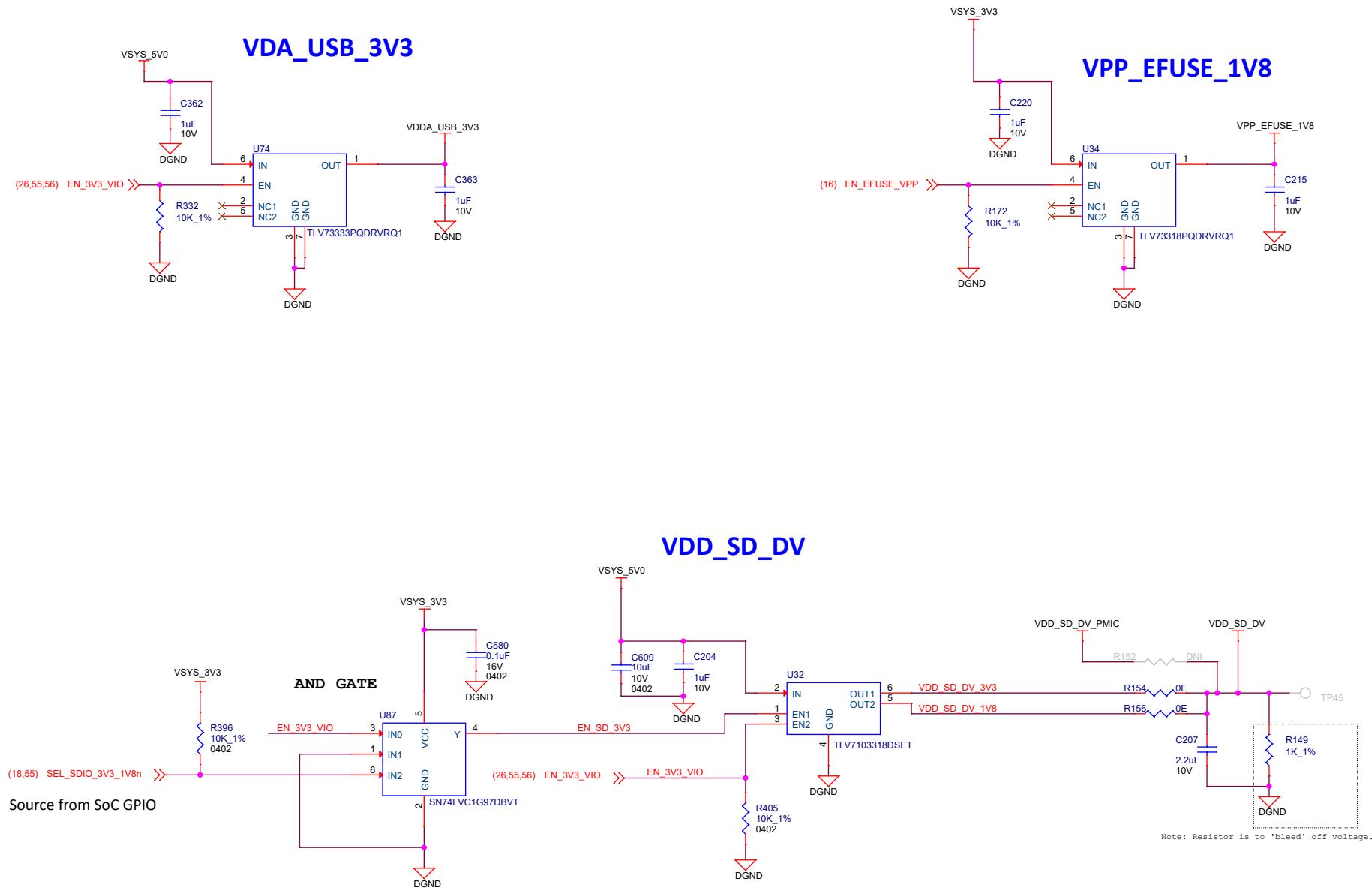
Line to Shape keeptout needs to be given in layout for VDD_DDR_1V1 and DGND feedback traces

PMIC-A uses default I2C ADDR: 0x48, 0x49, 0x4A & 0x4B

Pull up disables the PMIC Watchdog

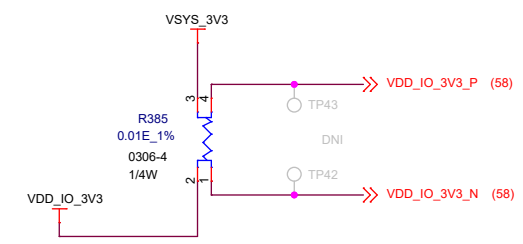
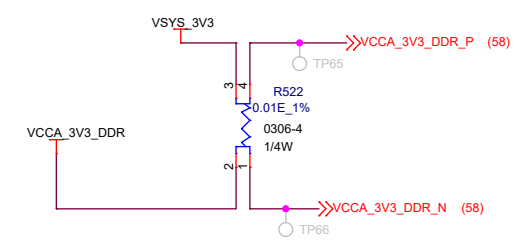
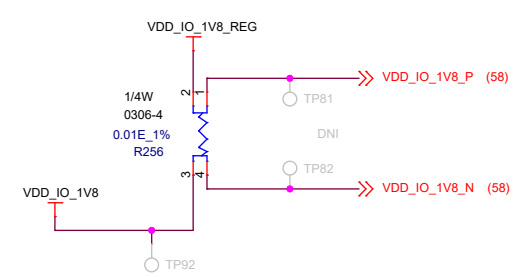
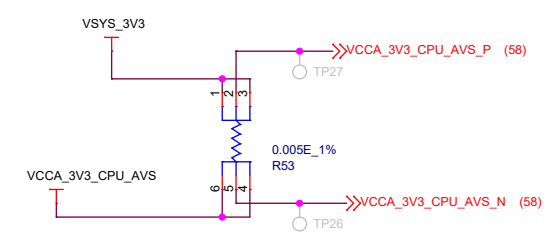
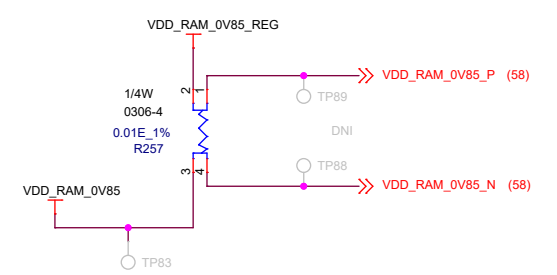
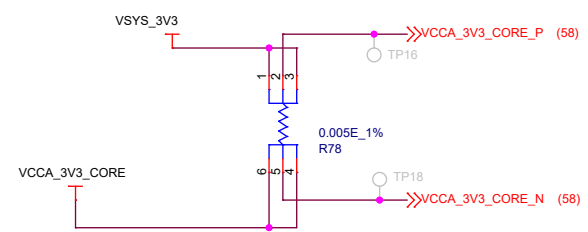
Project : AM69 Edge AI Kit		Title : PMIC	
		Size : C	Rev : E3
Date : Monday, March 20, 2023	Sheet : 55 of 62		

LDOs

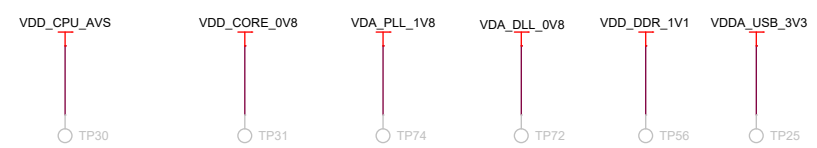


SOC Current Sense Resistors

CORE, AVS and DDR input supply sense resistors



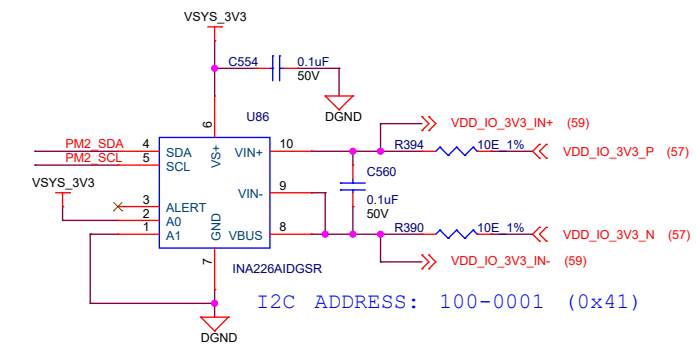
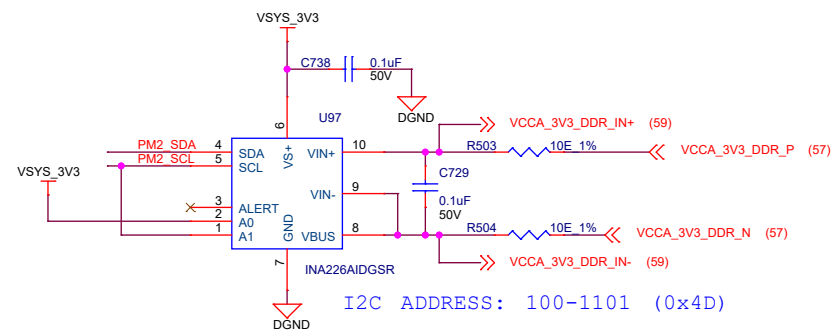
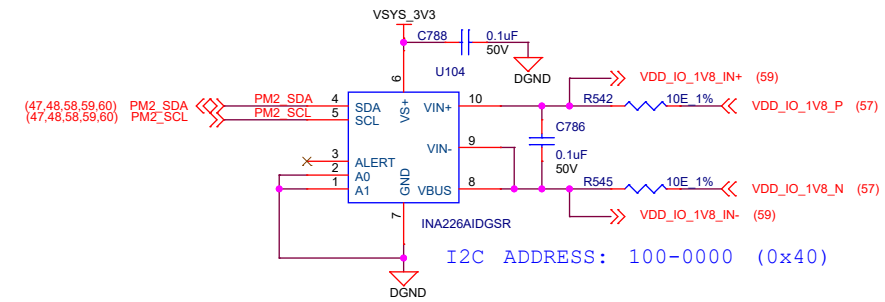
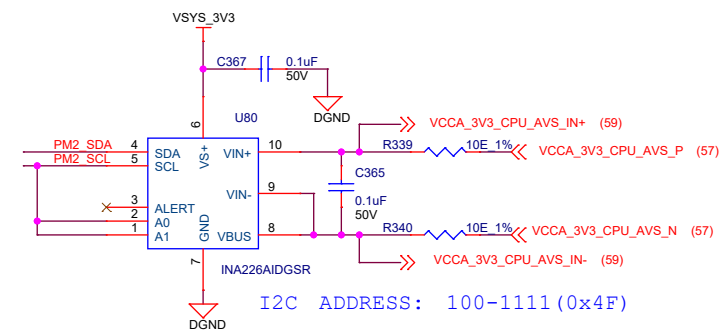
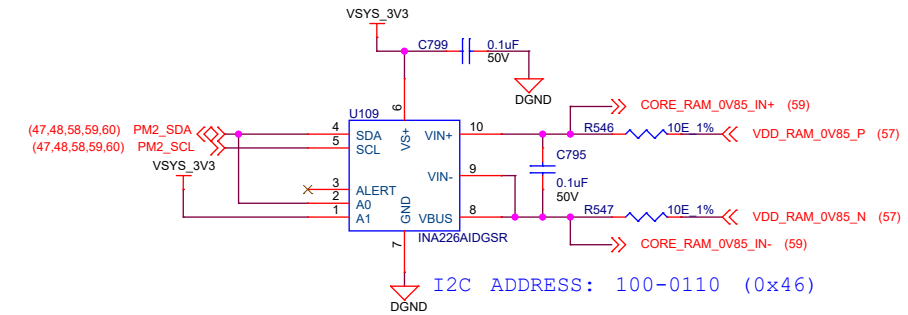
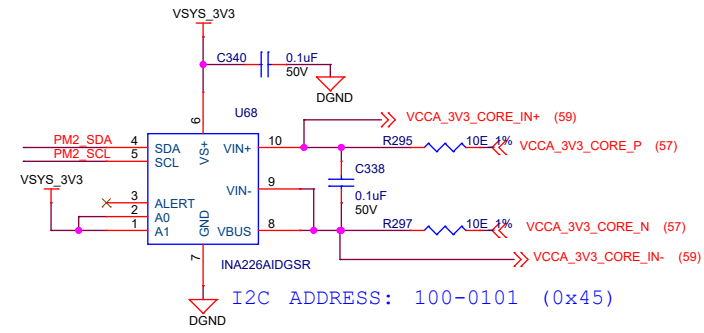
PCB Note: Place all SMT TPs on PCB top-side & on top of via at Bd-to-Bd connector



Project : AM69 Edge AI Kit		Title SOC - CURRENT SENSE RESISTORS	
		Size C	Rev E3
Date: Monday, March 20, 2023		Sheet 57 of 62	

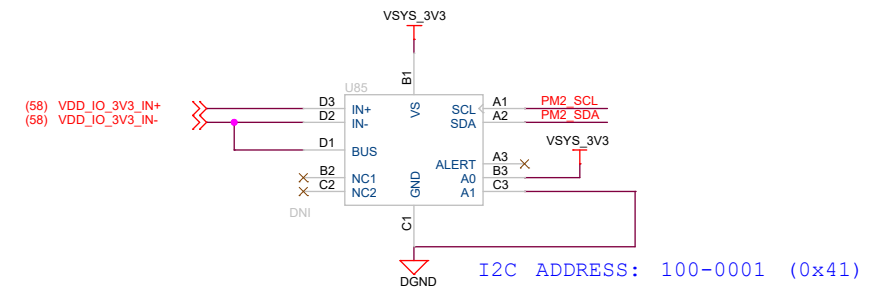
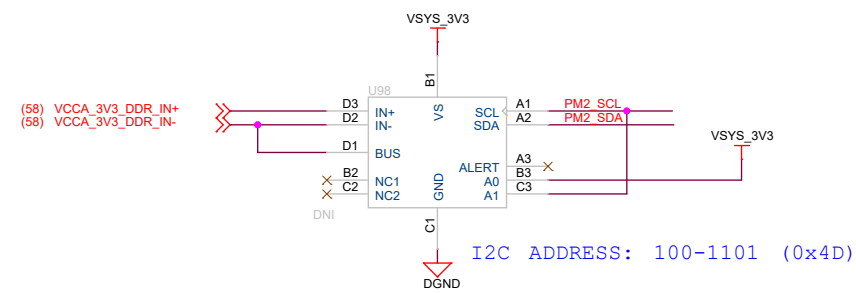
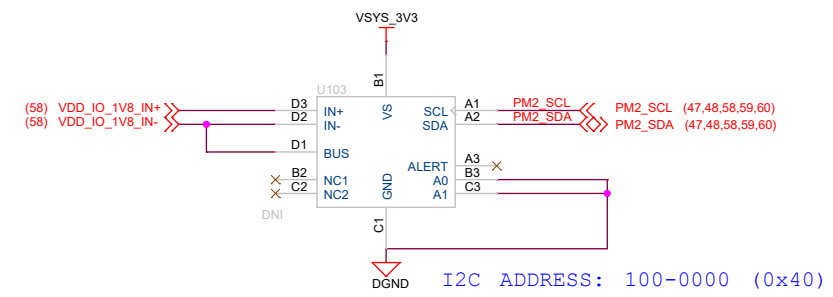
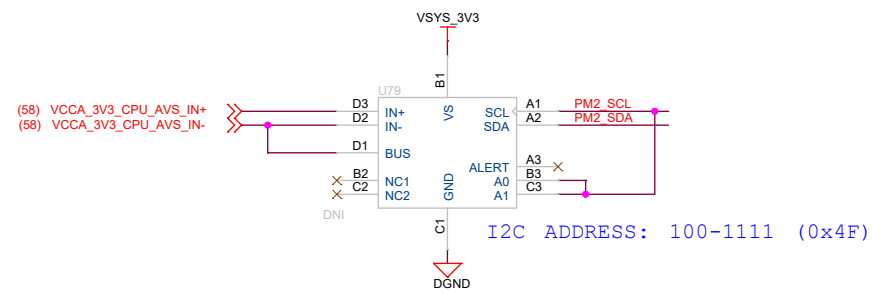
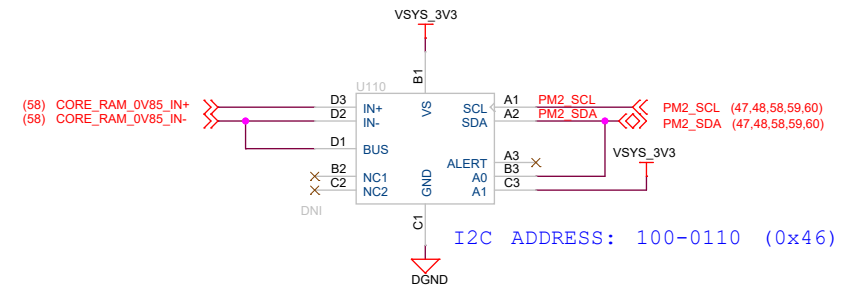
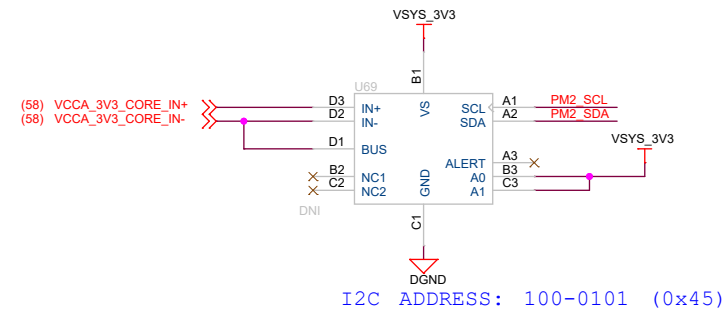
Note: The design supports current/voltage measurements using either INA226 or INA231. The SK will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

CURRENT MONITORS - INA226



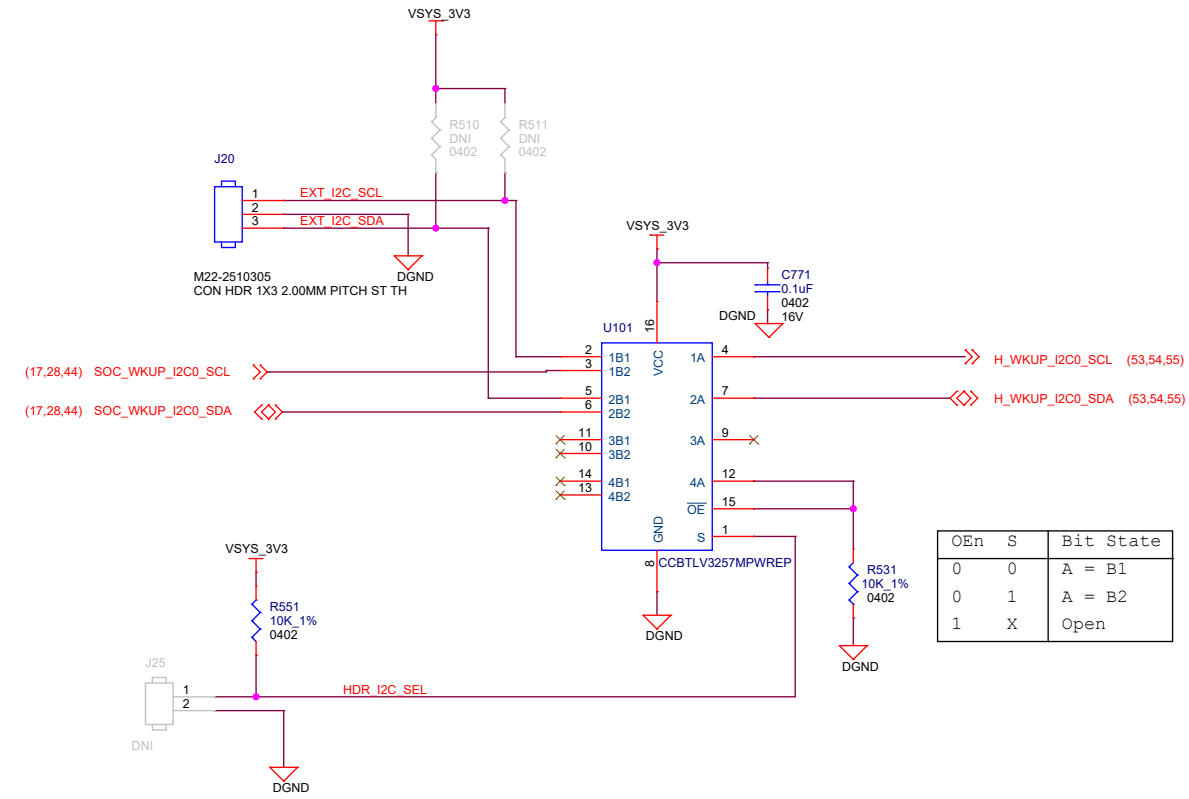
CURRENT MONITORS - INA231

Note: The design supports current/voltage measurements using either INA226 or INA231. The SK will be assembled with either INA226 or INA231, but not both (implemented via dual or stacked PCB footprint). These two INA devices are register compatible- so functionality and performance should not be impacted with either INA

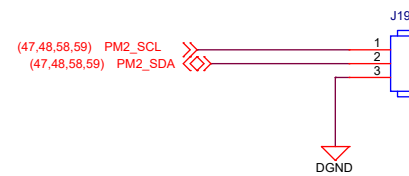


Project : AM69 Edge AI Kit		Title : CURRENT MONITORS - INA231	
Size : C		PROC154E3 001 SK AM69	
Date: Monday, March 20, 2023		Rev : E3	
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PMIC Support Circuit



EXT POWER MEASUREMENT



Project :
AM69 Edge AI Kit



Title: PMIC SUPPORT CIRCUIT

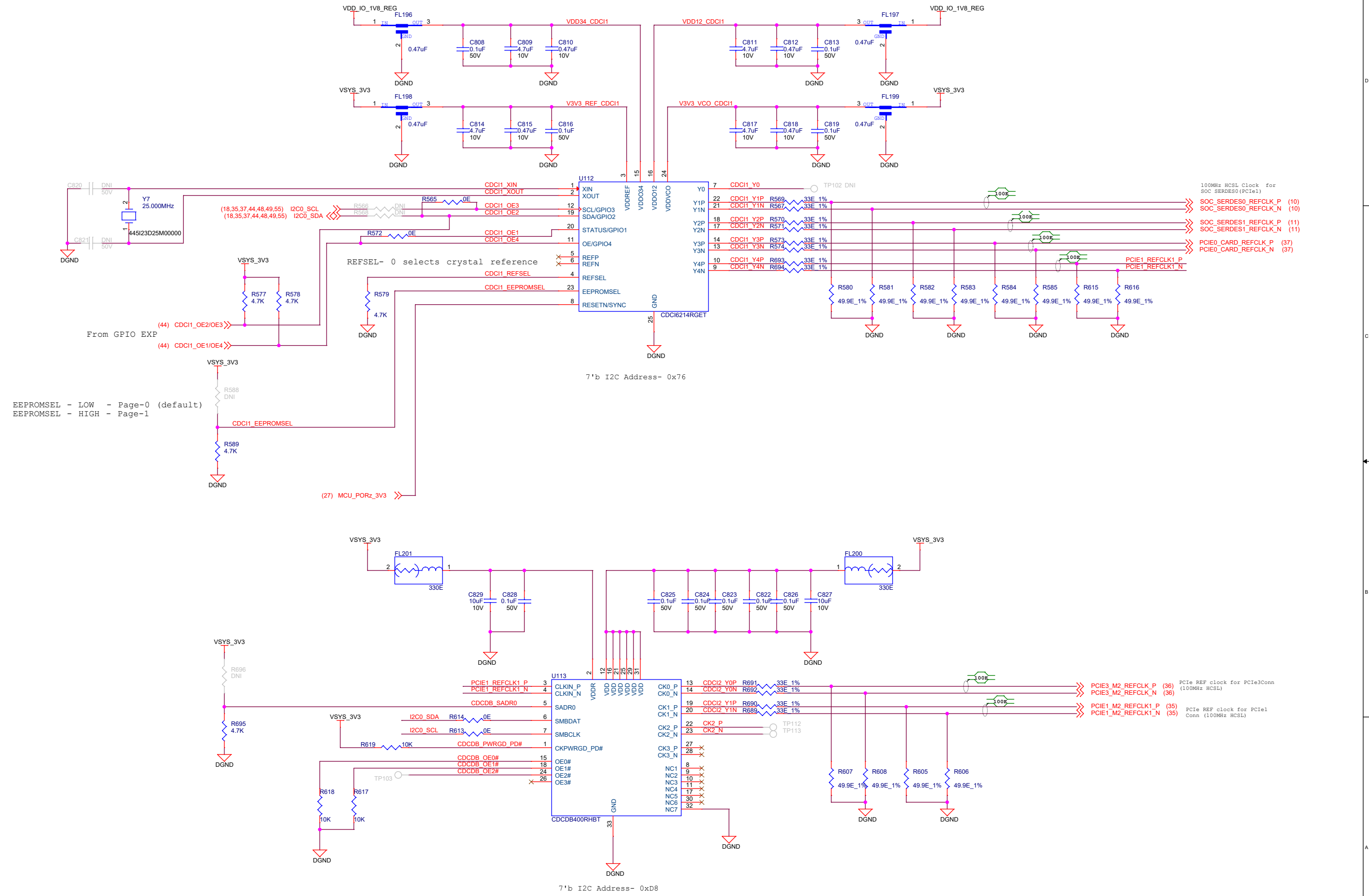
Size: PROC154E3 001 SK AM69

Date: Monday, March 20, 2023

Rev: E3

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SERDES CLOCK GENERATORS



EEPROMSEL - LOW - Page-0 (default)
EEPROMSEL - HIGH - Page-1

(44) CDC1_OE2/OE3
(44) CDC1_OE1/OE4

(27) MCU_PORz_3V3

NOTES, HW & LABELS

ASSEMBLY NOTES

1. All MSL components should be baked as per JEDEC standard.
2. PCB should be baked at 120 degree for 8 hours.
3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
4. These assemblies are ESD sensitive, ESD precautions shall be observed.
5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
6. Provide serial numbers to the assembled boards for identification.
7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

LABELS

Board Serial No.

LBL1
PCB LABEL

AM6-COMPROCEVM

Assembly Revision.

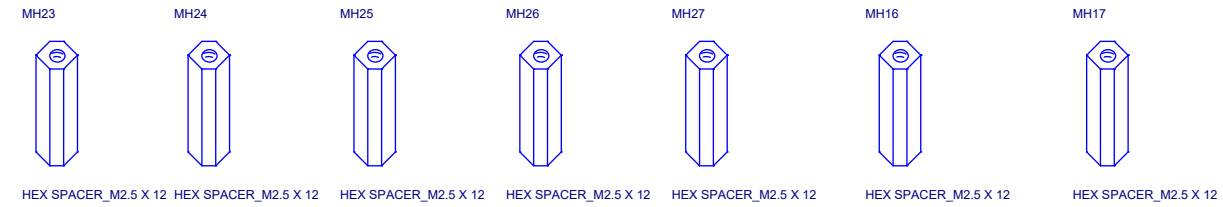
LBL2
PCB LABEL

AM6-COMPROCEVM

SCREWS



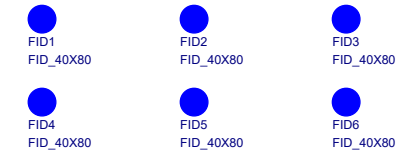
STANDOFFs



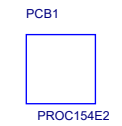
WASHER



FIDUCIALS



BARE PCB



SCREW & WASHER FOR PCIe M.2



LOGOs

PCB LOGO
Texas Instruments
Texas Instruments

PCB LOGO
For Evaluation only; not FCC approved for resale
For Evaluation only; not FCC approved for resale

PCB LOGO
WEEE Mark
WEEE Mark

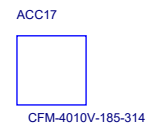
PCB LOGO
CE Mark
CE Mark

PCB LOGO
High Temperature
High Temperature

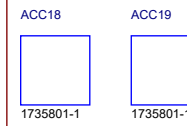
HEAT SINK



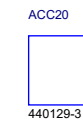
FAN



CRIMP PIN



CONN HOUSING



SCREW FOR FAN ASSEMBLY

