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PS8419

HDMI 2.1 Jitter Cleaning Repeater/Retimer

Version 0.9

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Notice

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KEY FEATURES

- Compliant with HDMI 2.1 specification FRL up to 12Gbps
- Compliant with HDMI 2.0 specification TMDS up to 6Gbps
- AC coupling capable for level shifting
- DC coupling capable for repeating
- SCDC interception technology for HDMI repeating
- Built-in DDC active buffering side-band signals
- Jitter Cleaning
- CrystalFree operation
- Automatic Link Training support – no system level support needed
- Superior Intra-pair and Inter-pair de-skewing
- Programmable receiver equalization to compensate for PCB, cable and/or connector losses
- Link training based automatic equalization adjustment for FRL mode
- Automatic power down management
- Low power consumption
- Pin control or optional local I2C control
- 3.3V and 1.1V power supply
- 4.5x6.5mm 46-pin QFN RoHS compliant and halogen-free package

APPLICATIONS

- Notebook/PC Motherboards
- Docking Stations
- TV/Monitor/Projectors
- Set-top Boxes

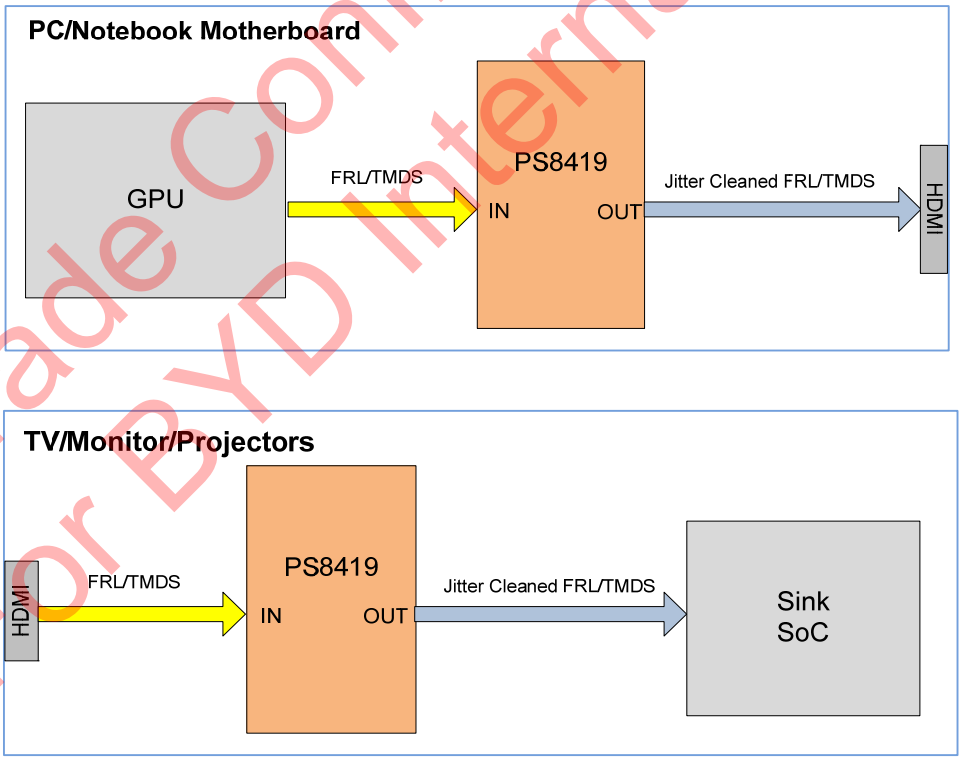


Figure 1. Typical Application

Overview

PS8419 is a single-port HDMI/DVI Level Shifter/Repeater with re-timing. It supports input FRL signals up to 12Gbps over 4 lanes with programmable equalization and jitter cleaning. It also supports both AC and DC coupled input TMDS signals up to 6Gbps operation with programmable equalization and jitter cleaning. The jitter cleaning PLLs remove input jitter and completely resets the system jitter budget; therefore better meets the HDMI jitter compliance requirement for higher data rates. Device operation and configuration can be realized through pin settings or I2C bus. Automatic power down and squelch provide flexible power management.

Fixed Rate Link

PS8419 is compliant with HDMI 2.1 spec; it can work in Fixed Rate Link (FRL) mode. When operating in 4-lane mode, the link rate is fixed to 6Gbps, 8Gbps, 10Gbps or 12Gbps. When operating in 3-lane mode, the link rate is fixed to 3Gbps or 6Gbps. The FRL mode of operation uses 16b18b coding, replacing TMDS coding and delivering improved performance and efficiency.

DDC Channel Interception

To support FRL link training over the HDMI output port, the PS8419 implements a DDC Channel interception scheme to manage the PHY setting at the output port. The DDC Channel interceptor in the PS8419 is a passive “listener” to intercept the FRL training information passing through the DDC Channel. This intercepted data is used to adjust the lane count, link rate and FFE level. The PS8419 is not directly involved with the Source-Sink handshaking interactions over the DDC Channel; it simply responds to the Source link training process to regenerate a high-quality signal directly at the output port.

Jitter Cleaning

PS8419 supports jitter cleaning mode and redriving mode for both FRL and TMDS operation. When operating in jitter cleaning mode, the internally jitter cleaning circuitry cleans out input jitter and regenerates output signals completely to achieve the great output jitter performance.

Programmable Receiving Equalization

PS8419 provides programmable equalization at the receiving side to compensate for signal loss caused by FR4 PCB traces, cables, connectors and other channel degradations, and to improve the signal quality before the output driver.

Feed Forward Equalizer

PS8419 supports the Feed Forward Equalizer (FFE) feature to compensate the Source channel and to improve the link performance. PS8419 implements FFE with up to 4 settings, TxFFE0 to TxFFE3. PS8419 also supports De-emphasis only, Pre-shoot only and No FFE modes.

Output Pre-emphasis

PS8419 supports TMDS output pre-emphasis. The pre-emphasis feature can be enabled to exaggerate/pre-condition the edges at the signal transmitter to optimize the output eye diagrams.

I2C-Over-AUX

PS8419 has a built-in bidirectional AUX to I²C bridge which converts mapped I²C transaction on AUX transaction (so called I²C-over-AUX) to native I²C signals, then passes them to DDC channel at sink side and vice versa.

Automatic Power Management

PS8419 features automatic power management capability that powers down the device when no sink device is connected. The hot plug detect pin HPD_SNK is used to achieve such function. When PS8419 detects this pin to be low which occurs when no sink device is connected, it goes into standby mode and tri-states its output for power saving. Upon an HPD assertion (Sink device connected), PS8419 will wake up automatically for normal operation.

Automatic Squelch and Input Fail Safe

PS8419 implements an automatic squelch feature for FRL/TMDS output to manage input signal detection and to control output signals on main link. With the automatic squelch, PS8419 will disable the output driver and put the device into power saving mode when the input signal is detected lower than the threshold, which is defined as loss of signal (LOS). This feature can help prevent signal repeating that is not needed and to manage the power state by monitoring the input swing. When LOS is asserted, the output will be tri-stated.

FUNCTIONAL BLOCK DIAGRAM

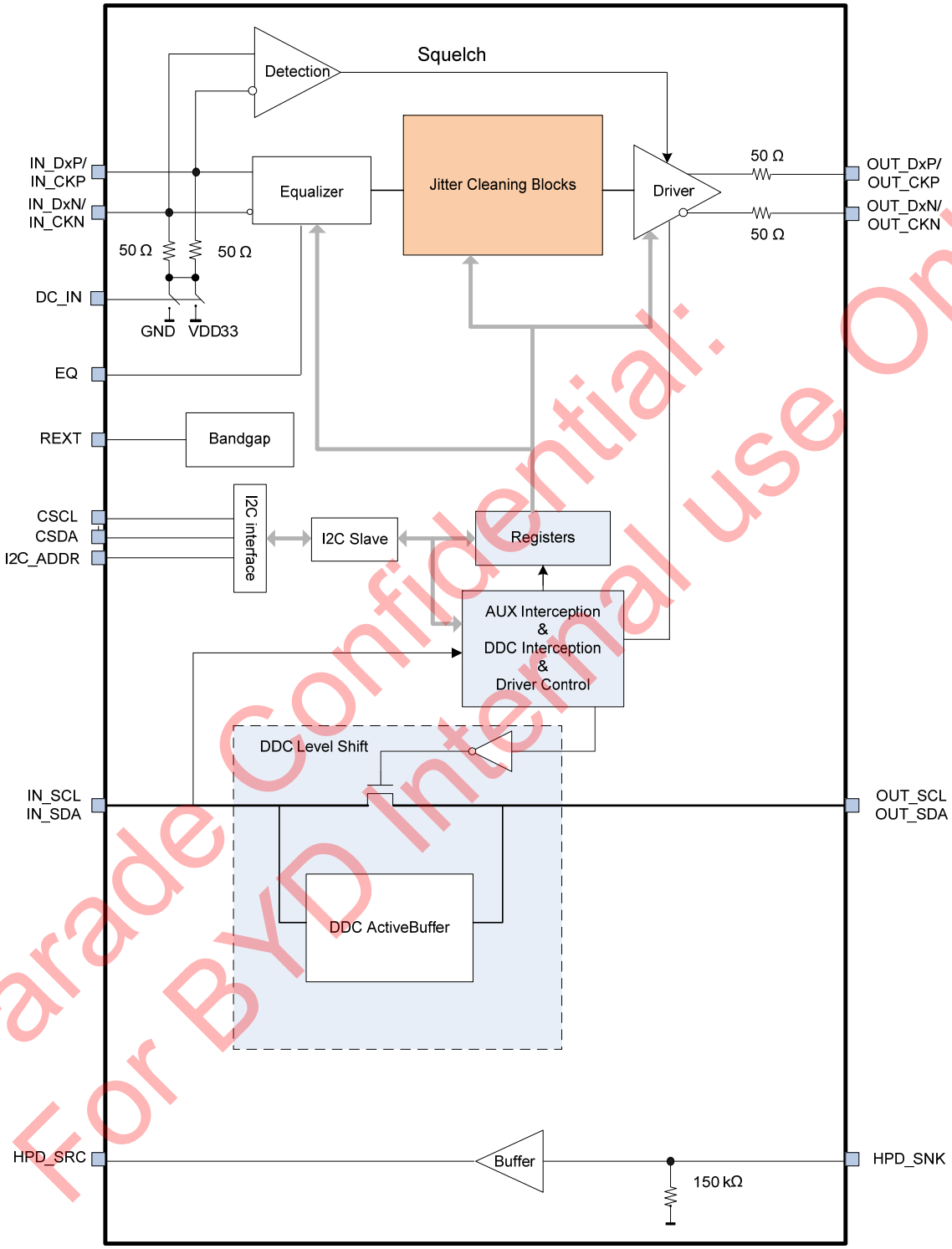


Figure 2. Functional Block Diagram

PIN ASSIGNMENT & DESCRIPTION: PS8419 – QFN46 (46-pin QFN)

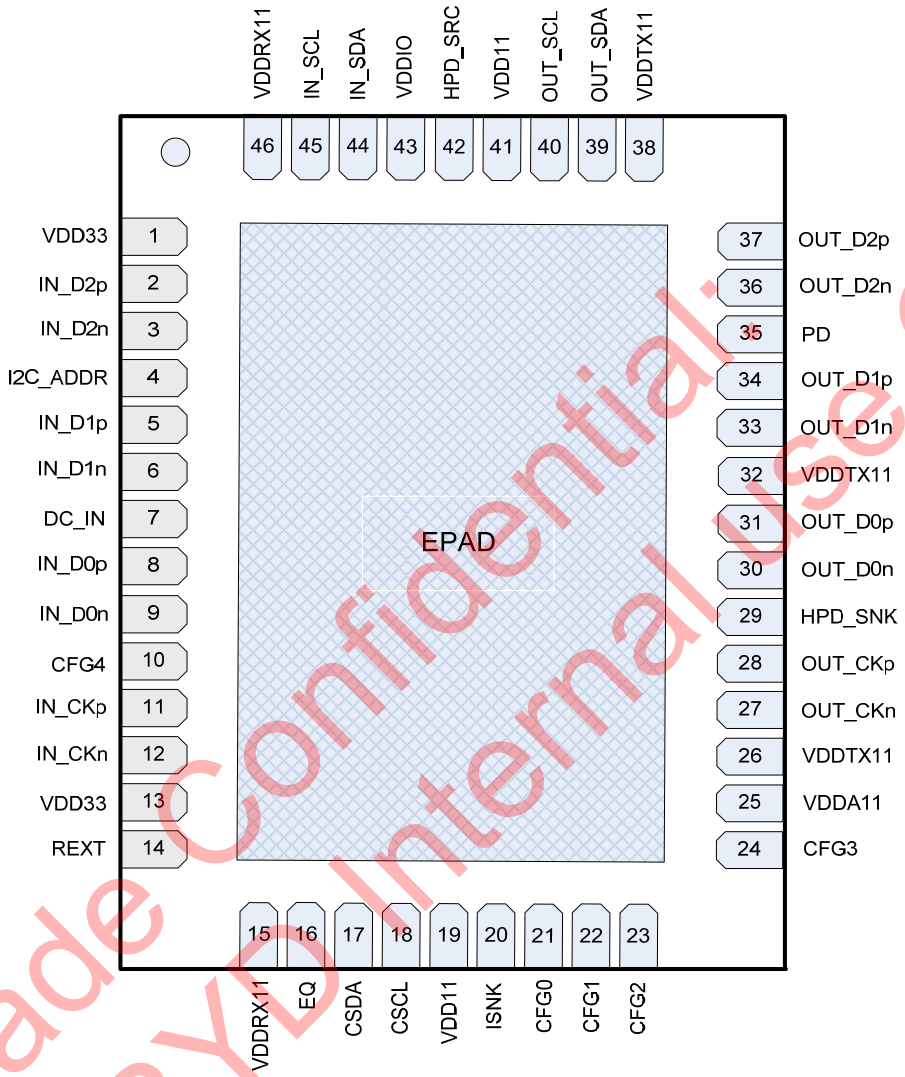


Figure 3. PS8419 QFN46 Pin Assignment (Top View)

Table 1. Pin Descriptions

Name	I/O	Description
IN_DxP/IN_DxN	I	HDMI data differential input: x=0,1,2
IN_CKP/IN_CKN	I	HDMI CK differential input
OUT_DxP/OUT_DxN	O	HDMI data differential output: x=0,1,2
OUT_CKP/OUT_CKN	O	HDMI CK differential output
HPD_SNK	I	SINK side HPD input, 5V tolerant, internal 150kΩ pull-down.
HPD_SRC	O	HPD output to Source, 3.3V CMOS output
IN_SCL/INSDA	I/O	DDC clock/data source side interface
OUT_SCL/SDA	I/O	DDC clock/data sink side interface. 5V tolerant
I2C_ADDR	I	I2C Address selection input pin, 3-level
CSCL/CSDA	I/O	Local I2C control bus for configuration
DC_IN	I	Internal 150kΩ pull-down L: RT50 at HDMI input tied to GND H: RT50 at HDMI input tied to VDD33
EQ	I	EQ setting with 5-level input
PD	I	Chip power-down. Active high. Internal 150kΩ pull-down. L: Normal operation H: chip power-down
ISNK	A	Open drain gate for HDMI output current sink
CFGx	I	Chip Configuration Pins: x=0,1,2,3,4
REXT	A	Connect a 4.99kΩ, 1% resistor to GND for analog current generation. This resistor is not adjustable.
VDDIO		DDC switch power supply. VDDIO should be connected to 1.8V or 3.3V power.
VDD11,VDDRX11,VDDTX11,VDDA11	P	1.1V supply for analog and digital circuit blocks
VDD33	P	3.3V supply
EPAD	P	Connects to GND plane through thermal Via

ABSOLUTE MAXIMUM RATINGS

Parameters	Comments	Min	Typ	Max	Unit
Supply Voltage Range:					
VDD33		-0.5		3.6	V
VDDRX11, VDDA11, VDD11, VDDTX11		-0.5		1.21	V
Normal I/O Voltage Range		-0.5		3.6	V
T_J	Junction temperature			125	°C
T_S	Storage temperature	-40		150	°C
ESD	Human Body Model				
	- Connector Pins		+/- 5000		V
	- Other Pins		+/- 5000		V
	Machine Model		+/- 200		V
	Charged Device Model		+/- 1000		V

ESD Standard:
Human Body Model: JS-001-2012
Machine Model: JESD22-A115-C
Charged Device Model: JESD22-C101-E
Latch-up Standard: JESD78D; I-Test: +/- 200mA; V-Test: 1.5X of Vcc

NORMAL OPERATION CONDITIONS

Parameter	Min	Typ	Max	Unit
Supply Voltage:				
VDD33	3.0	3.3	3.6	V
VDDIO (for 1.8V)	1.7	1.8	1.9	V
VDDIO (for 3.3V)	3.0	3.3	3.6	V
VDDRX11, VDDA11, VDD11, VDDTX11	1.05	1.1	1.15	V
Operation Temperature				
T_a – Ambient Temperature	0		70	°C
T_j – Junction Temperature	0		125	°C

POWER CONSUMPTION

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage, VDD33		3.0	3.3	3.6	V
Supply Voltage, VDDRX11, VDDA11, VDD11, VDDTX11		1.05	1.1	1.15	V
Data rates = 12Gbps, 4 lanes	Tested at				
1.1V Normal Supply Current, I_{DD}	VDD33 = 3.3V		720		mA
3.3V Normal Supply Current, I_{DD}	VDDRX11 = 1.1V		61		mA
Data rates = 10Gbps, 4 lanes	VDDA11 =1.1V				
1.1V Normal Supply Current, I_{DD}	VDD11=1.1V		708		mA
3.3V Normal Supply Current, I_{DD}	VDDTX11=1.1V		61		mA
Data rates = 8Gbps, 4 lanes	Input AC coupling,				
1.1V Normal Supply Current, I_{DD}	Jitter cleaning mode		655		mA
3.3V Normal Supply Current, I_{DD}			61		mA
Data rates = 6Gbps, 4 lanes					
1.1V Normal Supply Current, I_{DD}			612		mA
3.3V Normal Supply Current, I_{DD}			61		mA
Data rates = 6Gbps, 3 lanes					
1.1V Normal Supply Current, I_{DD}			496		mA
3.3V Normal Supply Current, I_{DD}			51		mA
Data rates = 3Gbps, 3 lanes					
1.1V Normal Supply Current, I_{DD}			400		mA
3.3V Normal Supply Current, I_{DD}			51		mA
Data rates = 5.94Gbps	Tested at				
1.1V Normal Supply Current, I_{DD}	Input DC coupling,		480		mA
3.3V Normal Supply Current, I_{DD}	Jitter cleaning mode		104		mA
Data rates = 2.97Gbps					
1.1V Normal Supply Current, I_{DD}			370		mA
3.3V Normal Supply Current, I_{DD}			104		mA
Auto Power Down, I_{APD}					
PD = Low, HPD_SNK = Low					
1.1V Normal Supply Current, I_{APD}			1		uA
3.3V Normal Supply Current, I_{APD}			10		uA
Power Down, I_{PD}					
PD = High, HPD_SNK = High					
1.1V Normal Supply Current, I_{PD}			1		uA
3.3V Normal Supply Current, I_{PD}			20		uA
Total Power Consumption@12Gbps, 4lanes			994		mW

Total Power Consumption@10Gbps, 4lanes			980		mW
Total Power Consumption@8Gbps, 4lanes			922		mW
Total Power Consumption@6Gbps, 4lanes			875		mW
Total Power Consumption@6Gbps, 3lanes			714		mW
Total Power Consumption@3Gbps, 3lanes			608		mW
Total Power Consumption@ 5.94Gbps			871		mW
Total Power Consumption@ 2.97Gbps			750		mW
Total Power Consumption @ Auto Power Down			34		uW
Total Power Consumption @Power Down Mode			67		uW

PACKAGE DISSIPATION RATING

46-pin QFN	Still air, 4-layer PCB
θ_{JA} – Junction to Ambient Thermal Resistance	28.5 °C/W
θ_{JC} – Junction to Case Thermal Resistance	12.1 °C/W
Maximum Power Dissipation Rating, Ta = 70 °C	1930mW

DC CHARACTERISTICS

Parameter		Test Conditions	Min	Typ[b]	Max	Unit
Five-level Input Pin: EQ						
Level 0		Pull Down with 1kΩ		19		dB
Level 1		Pull Down with 20kΩ		18		dB
Level 2		Floating		16		dB
Level 3		Pull up with 20kΩ		13		dB
Level 4		Pull up with 1kΩ		7		dB
Control Pins (Internal pull-up): DCIN, PD						
V_{IH}	LVTTL input High-level voltage		2		VDD33	V
V_{IL}	LVTTL input Low-level voltage		GND		0.8	V
$\|I_{IH}\|$	Input High-level current	V_{IH} = 2V to VDD33			10	µA
$\|I_{IL}\|$	Input Low-level current	V_{IL} = GND to 0.8V			40	µA
Control Pin (Internal pull-down): I2C_ADDR						
V_{IH}	LVTTL input High-level voltage		2		VDD33	V
V_{IL}	LVTTL input Low-level voltage		GND		0.8	V
$\|I_{IH}\|$	Input High-level current	V_{IH} = 2V to VDD33			40	µA
$\|I_{IL}\|$	Input Low-level current	V_{IL} = GND to 0.8V			10	µA
Control I^2C Pins: CSCL, CSDA						
V_{OH}	High-level output voltage	External 1.5 kΩ pull-up to			VDD33	V
V_{OL}	Low-level output voltage	VDD33, I_{OL} = 8 mA			0.4	V
SINK-side DDC Signal pins: OUT_SCL, OUT_SDA						
V_{IH}	LVTTL input High-level voltage	Active Buffer Enabled	2.3		5.3	V
V_{IL}	LVTTL input Low-level voltage	Externally pulled up to 5V	GND		0.8	V
V_{OL}	LVTTL output Low-level voltage	I_{OL}=8mA	GND		0.4	V
Source-side DDC Signal Pins: IN_SCL, IN_SDA (DDC mode)						
V_{IH}	LVTTL input High-level voltage	Active Buffer Enabled	VDDIO*0.7		VDDIO	V
V_{IL}	LVTTL input Low-level voltage	VDDIO = 3.3V.	GND		0.4	V
V_{OL}	LVTTL output Low-level voltage			0.65		V
V_{IH}	LVTTL input High-level voltage	Active Buffer Enabled	VDDIO*0.7		VDDIO	V
V_{IL}	LVTTL input Low-level voltage	VDDIO = 1.8V	GND		0.2	V
V_{OL}	LVTTL output Low-level voltage			0.4		V
HPD Input Pin: HPD_SNK						
V_{IH}	LVTTL input High-level voltage		2		5.3	V
V_{IL}	LVTTL input Low-level voltage		GND		0.8	V

[b] All typical values are measured at 25 °C and 3.3V / 1.1V power supply.

$\|I_{IH}\|$	Input High-level current	V_{IH} = 2 V to 5.3 V			80	uA
$\|I_{IL}\|$	Input Low-level current	V_{IL} = GND to 0.8 V			20	uA
HPD Output Pins: HPD_SRC						
V_{OH}	LVTTL High-level output voltage	I_{OH} = -8 mA	VDDIO*0.8			V
V_{OL}	LVTTL Low-level output voltage	I_{OL} = 8 mA			0.4	V
Resistors						
REXT	External reference resistor		4.94	4.99	5.04	kΩ
$R_{RX-TERM}$	Differential input termination resistor		80		120	Ω

AC CHARACTERISTICS

Parameter		Test Conditions	Min	Typ	Max	Unit
Supply Ramp-up Time						
$t_{3.3}$	3.3V supply ramp up time	10% to 90% of the 3.3V supply voltage			10	ms
$t_{1.1}$	1.1Vsupply ramp up time	10% to 90% of the 1.1V supply voltage			10	ms
Status Pins: HPD_SRC, HPD_SNK						
t_{HPD}	Propagation delay of HPD_SNK assertion at power saving mode to HPD_SRC assertion	C_L = 10 pF		35		ms
PD						
t_{Turn_On}	Delay from power down to normal operation			20		ms
t_{Power_Down}	Delay from normal operation to power down			200		ms

HDMI CHARACTERISTICS

Symbol and Parameter	Test Conditions	Min	Typ	Max	Unit
FRL Output					
V_{OD} Peak-to-Peak differential output swing	Test at TP1	400		1000	mV
DC Common Mode Voltage		AVcc-800		AVcc+30	mV
AC coupling capacitor	Only for AC coupled Source	100		250	nF
t_r Differential output rise time	20% to 80%	22.5			ps
t_f Differential output fall time	20% to 80%	22.5			ps
t_{sk_intra} Intra-pair differential skew			0.15		T_{bit}
t_{sk_inter} Inter-pair differential skew			4		T_{bit}
Through Connection Impedance		90		110	Ω
Source Termination Impedance		90		110	Ω

FRL TP2_EQ Source Jitter Requirement	**Data Bit Rate (R_{bit})**					**Unit**
	3G	**6G**	**8G**	**10G**	**12G**	
RJ: Peak-to-Peak random jitter for BER 10^{-10}	0.2					T_{bit}
DJ: Deterministic Jitter(=TJ-RJ)	0.3	0.4	0.415	0.43	0.45	T_{bit}
TJ: Total Jitter for BER 10^{-10}	0.5	0.6	0.615	0.63	0.65	T_{bit}

FRL Input					
V_{ID} Input Differential Swing voltage	3 Gbps@TP2	150		1200	mV
V_{ID} Input Differential Swing voltage	6 Gbps@TP2	150		1200	mV
V_{ID} Input Differential Swing voltage	8 Gbps@TP2	135		1200	mV
V_{ID} Input Differential Swing voltage	10 Gbps@TP2	120		1200	mV
V_{ID} Input Differential Swing voltage	12 Gbps@TP2	100		1200	mV
V_{ICM} Input Common Mode Voltage		Avcc-800		Avcc+30	mV

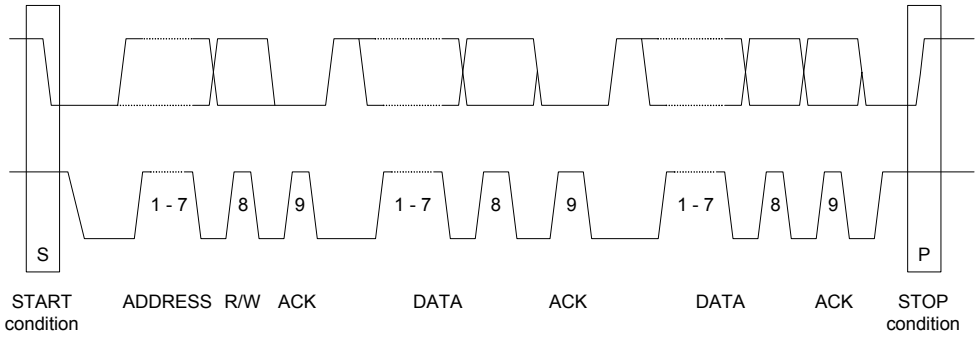
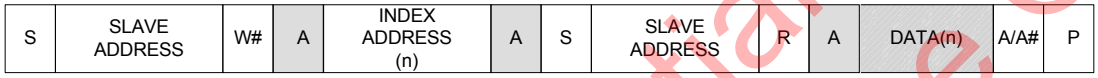
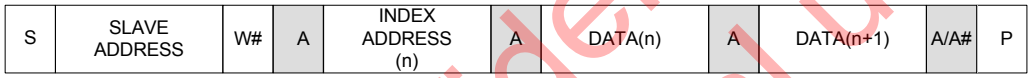


Figure 4. I2C Complete Data Transfer



I2C Read Command



I2C Write Command

From Master to Slave

From Slave to Master

S: START condition
P: STOP condition
A: Acknowlegde (SDA Low)
A#: not acknowledge (SDA High)
W#: Write command (SDA Low)
R: Read command (SDA High)
Slave Address: 7 bits
Index Address: 8 bits, index n
Data: 8 bits, reference to index n

Figure 5. I2C Read and Write Command

PIN MAPPING

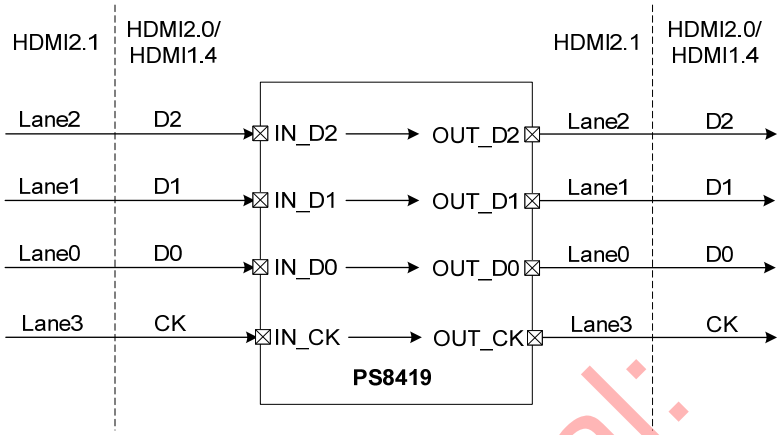


Figure 6. Pin Mapping for FRL and TMDS

TYPICAL APPLICATION

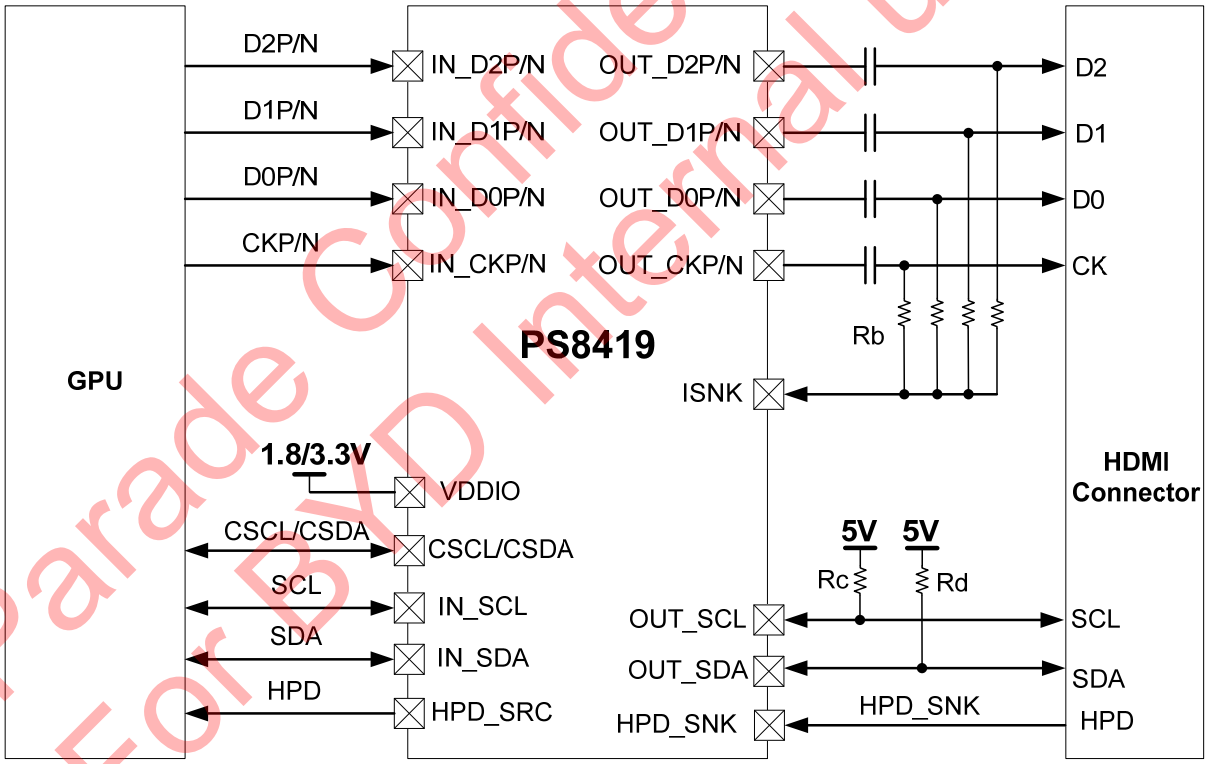


Figure 7. HDMI Repeater Source Application Diagram

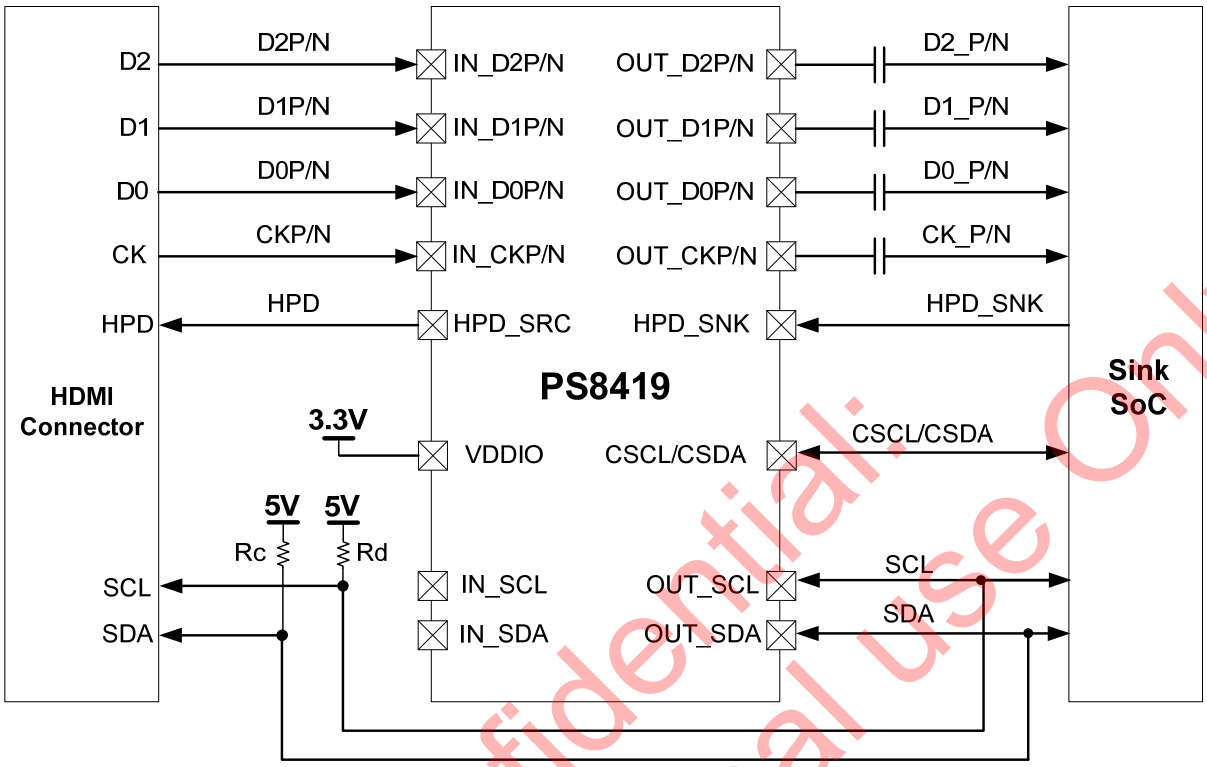


Figure 8. HDMI Repeater Sink Application Diagram

PCB LAYOUT PATTERN GUIDELINES – QFN46

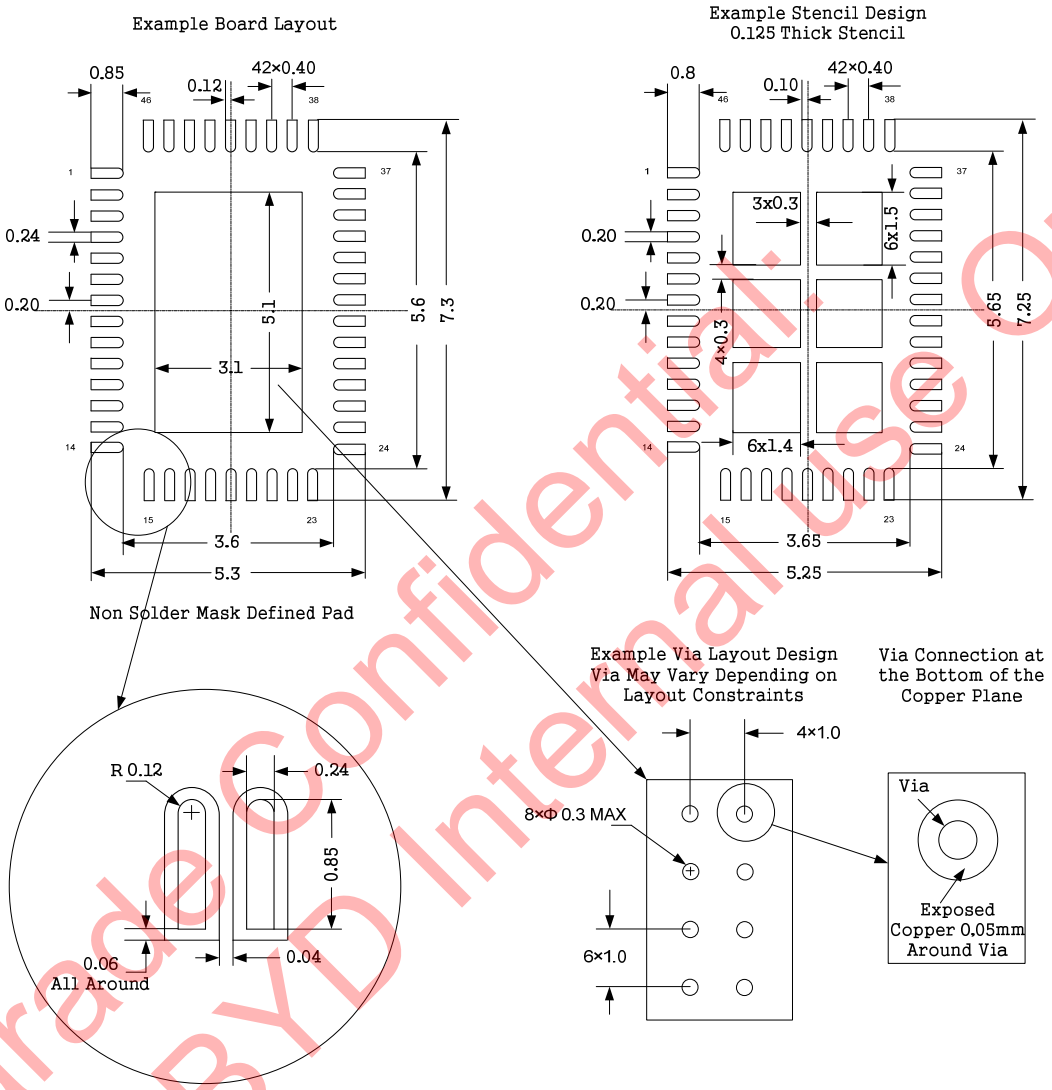


Figure 9. Exposed Thermal Pad Layout Guidelines – QFN46

NOTES:

1. All dimensions are in millimeters.
2. The drawing is subject to change without notice.
3. Customers should contact their board fabrication manufacturers for recommended solder mask tolerances and via tenting recommendations for via's placed in the thermal pad.

ORDER&PACKAGIN INFORMATION

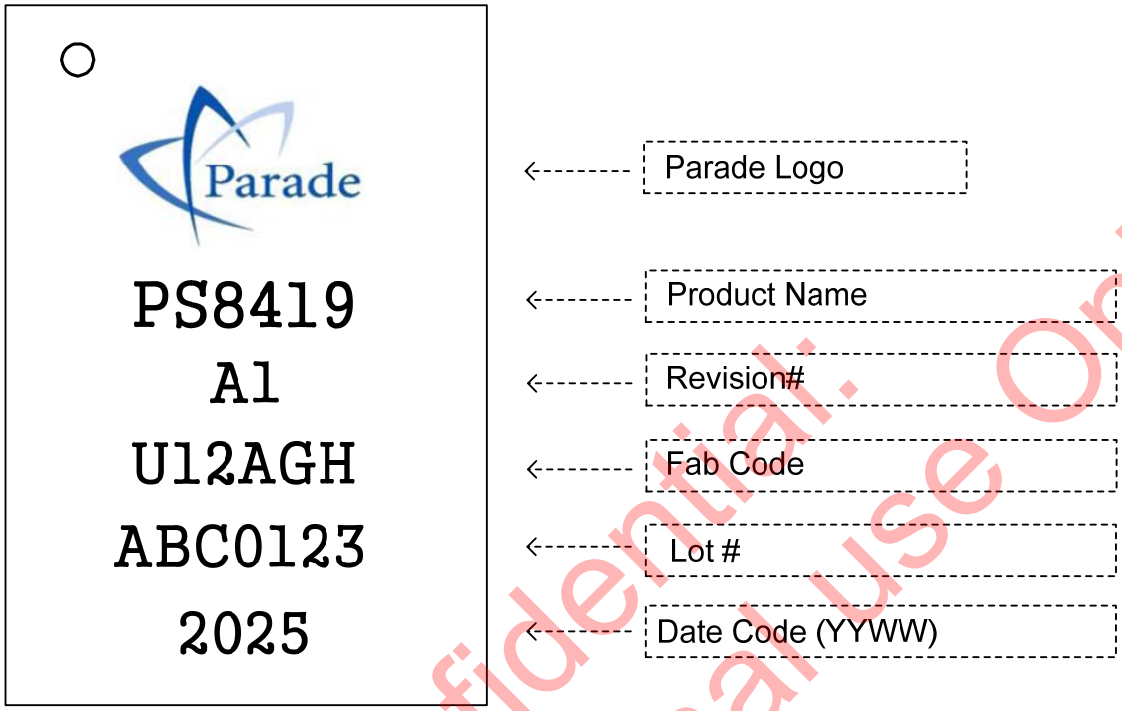
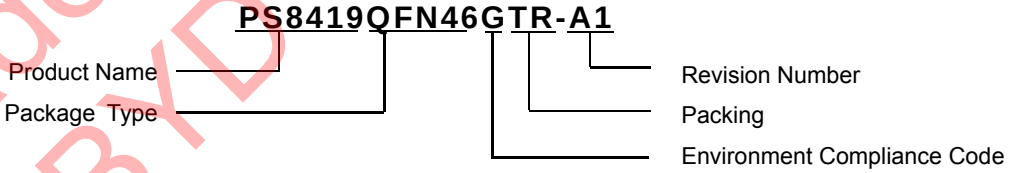


Figure 10. Top Side Marking

Ordering Information:

Part number:

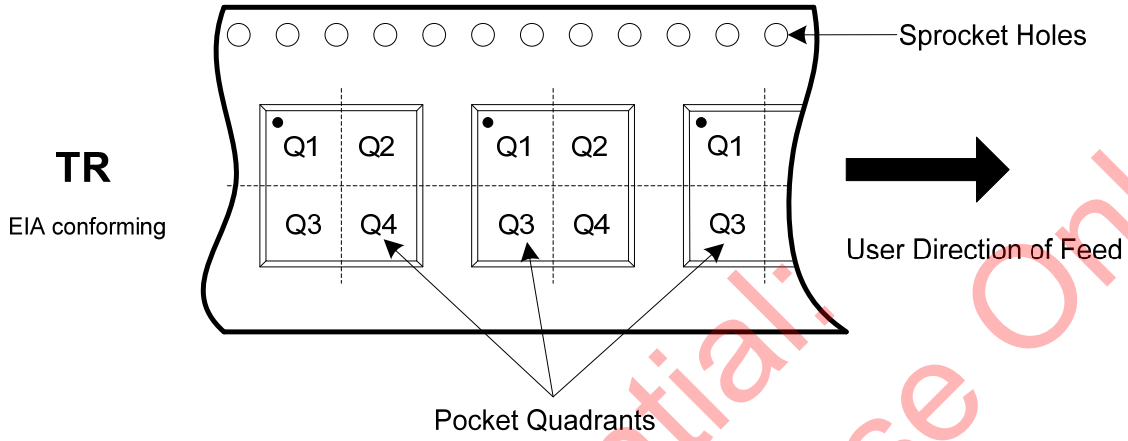


Part Number	Packing
PS8419QFN46GTR-A1	Tape and Reel

Lead Finish: 100% Sn

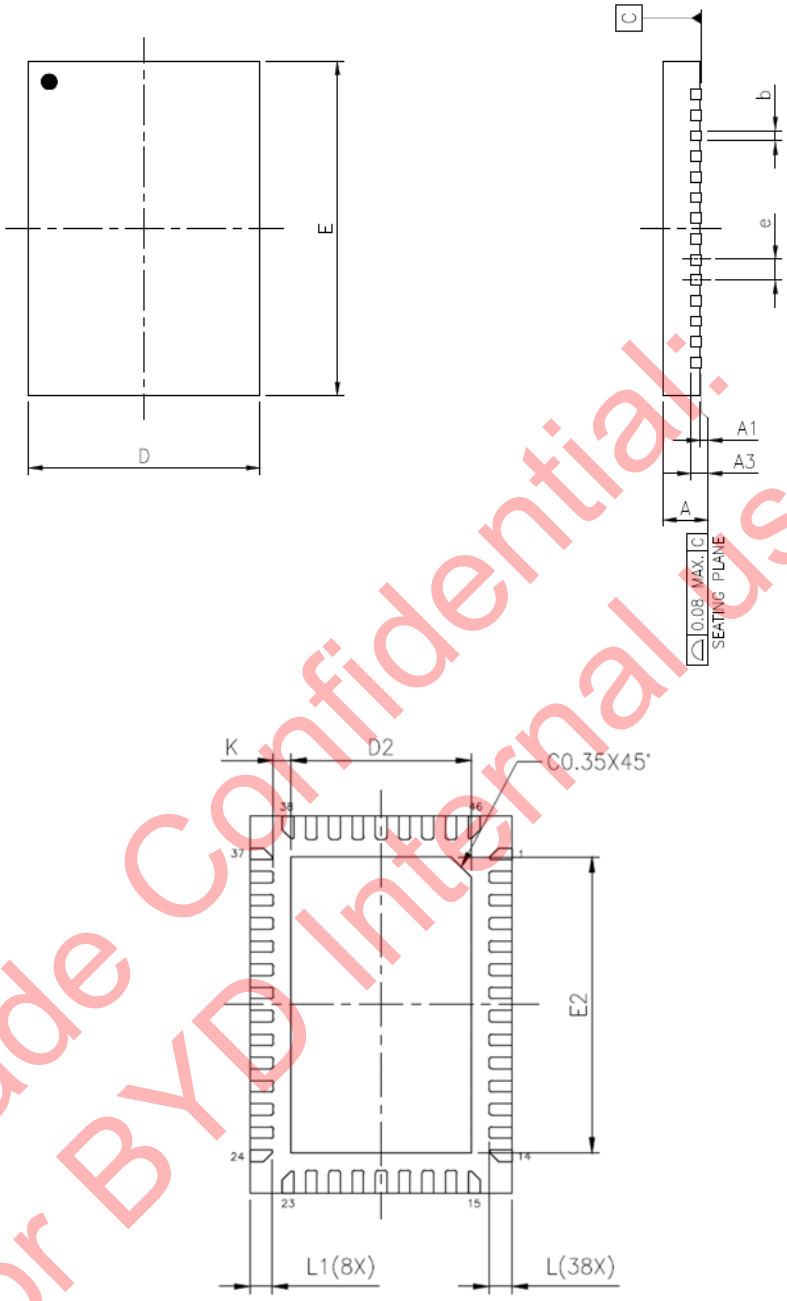
TAPE AND REEL PACKING PIN1 ORIENTATION

QUADRANT ASSIGNMENT FOR PIN1 ORIENTATION IN TAPE



PHYSICAL DIMENSIONS – QFN46

46-pin TQFN 4.5x6.5 mm²



Notes:

0. All linear dimensions are in millimeters.

Parameter	MIN	NOM	MAX	Unit
A	0.70	0.75	0.80	mm
A1	0.00	0.02	0.05	mm
A3		0.203 REF		mm
b	0.15	0.20	0.25	mm
D	4.40	4.50	4.60	mm
E	6.40	6.50	6.60	mm
e		0.40 BSC		mm
K	0.2			mm
D2	3.05	3.10	3.15	mm
E2	5.05	5.10	5.15	mm
L	0.35	0.40	0.45	mm
L1	0.33	0.38	0.43	mm

REVISION HISTORY

Version	Date	Items
Version 0.6	8/26/2019	Initial release
Version 0.8	1/22/2020	Update the power consumption table, Update the Chip Revision, Update Figure 7
Version 0.9	4/12/2020	Update the ESD and EQ parameter