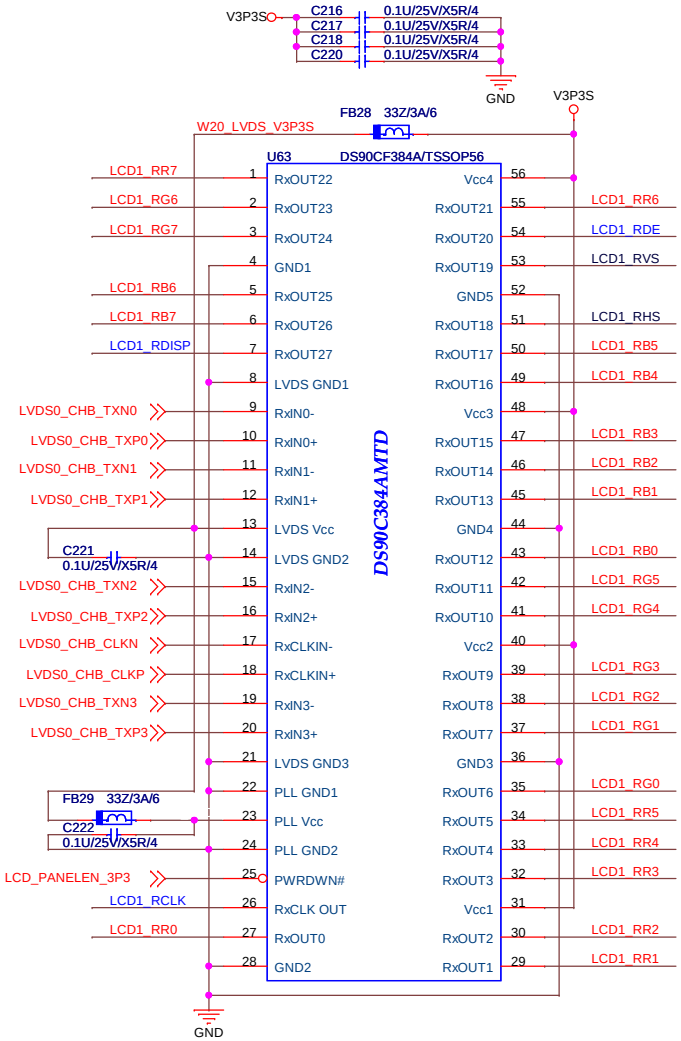
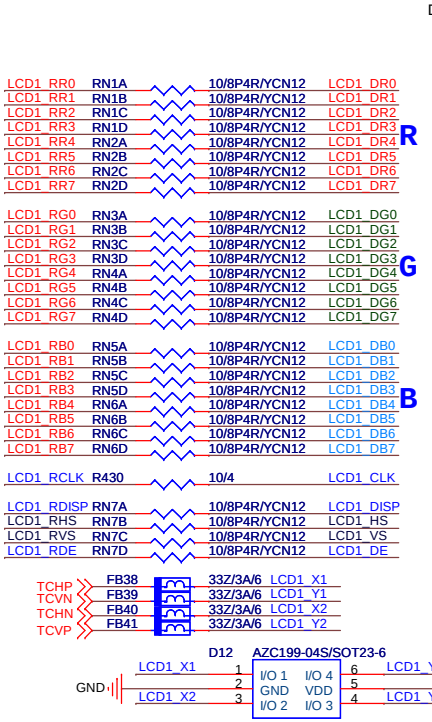
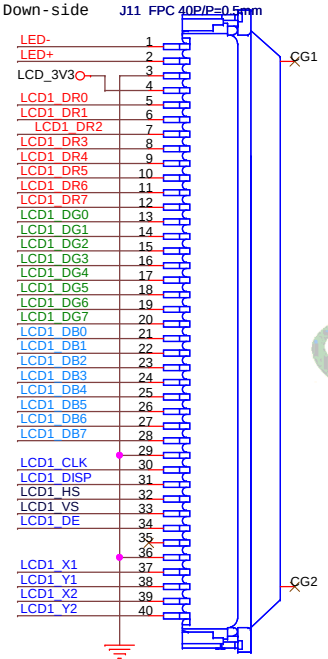
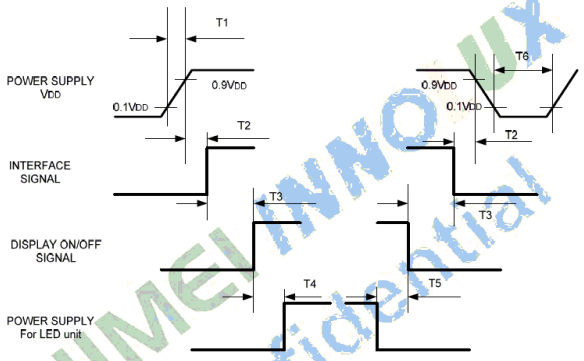




4.3" Panel



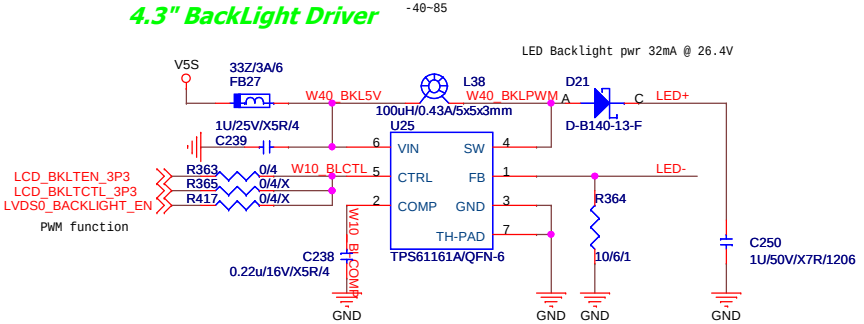


Symbol	Specification	Symbol	Specification
T1	0≦T1≦10 msec	T4	160 msec ≦T4
T2	0≦T2≦100 msec	T5	160 msec ≦T5
T3	0≦T3≦200 msec	T6	1 msec ≦T6

4.3" Sequence:
1. VDD/3.3V (Tr < 10ms)
2. Signal (Delay < 100ms)
3. DISP (Delay < 200ms)
4. VLED (Delay > 160ms)

4.3" BackLight Driver

-40~85



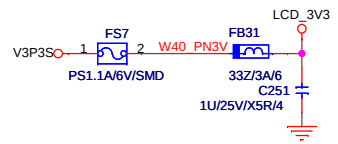


Table 8. LVDS single bus, 24 bpp, VESA data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

Ganlot Inc.		
Page 4.3" Panel		
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