

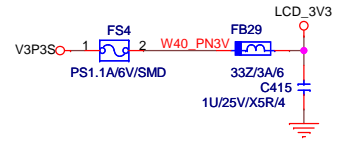
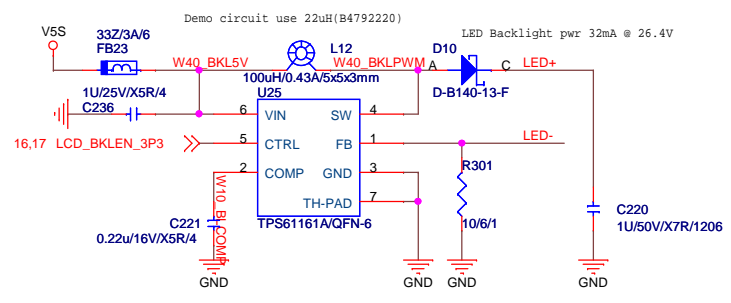
Symbol	Specification	Symbol	Specification
T1	$0 \leq T1 \leq 10$ msec	T4	160 msec $\leq T4$
T2	$0 \leq T2 \leq 100$ msec	T5	160 msec $\leq T5$
T3	$0 \leq T3 \leq 200$ msec	T6	1 msec $\leq T6$

- 4.3" Sequence:
1. VDD/3.3V ($T_r < 10$ ms)
 2. Signal (Delay < 100 ms)
 3. DISP (Delay < 200 ms)
 4. VLED (Delay > 160 ms)

Table 8. LVDS single bus, 24 bpp, VESA data packing

Channel	Bit position						
	6	5	4	3	2	1	0
LVDS odd differential channel A	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
LVDS odd differential channel B	bit 1	bit 0	bit 5	bit 4	bit 3	bit 2	bit 1
LVDS odd differential channel C	DE	VSYNC	HSYNC	bit 5	bit 4	bit 3	bit 2
LVDS odd differential channel D	don't care	bit 7	bit 6	bit 7	bit 6	bit 7	bit 6

4.3" BackLight Driver



Ganlot Inc.		
Page	4.3" Panel	
Size B	Project	Rev
	PTB-4110	Z000
Date:	Wednesday, August 09, 2017	Sheet 18 of 39