Phase Alignment in Synchronous Ethernet Mode for DP83640

1、background：

TI file **AN-1729** : 3.2 Phase Alignment talk about the clock output Phase Alignment, and there is an example about Phase alignment of a 10 MHz clock output:

3.2 Phase Alignment

Aligning the phase of the clock output requires the following steps:

1. Ensure the clock output pin is enabled.
2. Prior to enabling the PTP synchronization protocol, enable the clock output and the PTP clock.
3. Enable an event monitor for a single event to catch the rising edge of the clock output pin.
4. Determine clock output offset from aligned expected time: clock output period – (event timestamp mod clock output period).
5. Do a step adjustment to align the clock output.
6. During synchronization, all step adjustments should be in units of the clock output period.

Example: Phase alignment of a 10 MHz clock output:

1. Ensure the clock output pin is enabled. This can be done by strapping the GPIO1 pin high prior to power-up, or by clearing the CLK_OUT_DISABLE bit (bit 2) in the PHYCR2 register (register 0x1C).
2. Enable the clock output at 10 MHz: write 0x8019 to the PTP_COC register. Note that 0x19 is 25 decimal, to divide the 250 MHz clock by 25. Enable the PTP clock: write 0x0004 to the PTP_CTL register.
3. Take 100 samples of the CLK_OUT phase error.

TI file **AN-1730** : 4.2 Key Configuration Requirements talk about Phase Alignment in Synchronous Ethernet Mode:

For a network node to function as a PTP slave device, the node must be attached to a partner (node, switch, or repeater) which provides access to a Master PTP clock, and the PTP protocol must be enabled and active.

In addition, the partner must have its local reference clock frequency locked to the PTP master clock. If PTP clock phase alignment between the master and slave is also desired, the PTP master clock must be phase-aligned with the master PTP counter. For information on phase aligning the output clock in the DP83640, see *AN-1729 DP83640 IEEE 1588 PTP Synchronized Clock Output* (SNLA099).

It is also important to note that Synchronous Ethernet mode should only be enabled in a device which is utilized as a slave PTP clock node. Enabling Synchronous Ethernet mode in a master node will produce undesired results.

So I suppose DP83640 support Phase Alignment in Synchronous Ethernet Mode for Clock output.

2、for reference

a、TI file **AN-1729** 3.2 Example: Phase alignment of a 10 MHz clock output

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b、TI EPL-lib: EPL\protocol\PTP\ptpControl.c line 272 to 312 in function PTPInitHardware.

3、test condition

STM32 + FPFA + DP83640

master： Synchronous Ethernet Mode disabled

slave：Synchronous Ethernet Mode enabled

ptpd stack: not running

master and slave connected with cable.

Watch the two clock output by oscilloscope.

3、result

I do the Phase alignment in slave board, cause I don't think should adjust the master.

1、two clock output locked（cause Synchronous Ethernet Mode）

2、Phase is random when power up, and Phase alignment not working.

I debug the code find that the step adjustment is not working. Before this step, everything goes right.

7. Do a step adjustment to the 1588 clock time:
   - Write the correction value to PTP_TDR.
   - Write PTP_STEP_CLK (0x8) to PTP_CTL.

4、questions

a、To do the in Synchronous Ethernet Mode, Shoud I must run the ptpd stack?

I don't think so. This part of code is in function PTPInitHardware, and at this time the ptpd stack is not running, just set up the PHY. In addition, the two 83640 is Synchronous and Locked by set Synchronous Ethernet Mode bit.

In this condition, is it still need the ptpd stack running?

b、whether the phase of 2 clock outputs(GPIO 12) can be alignment through a step adjustment (reg PTP_TDR) to the 1588 clock time.

For example, in Synchronous Ethernet Mode AN-1730

4.1 Key Terms

Master Node: A master node is a Precision Time Protocol (PTP) enabled network node which contains or propagates a Master PTP clock signal and Master PTP counter data.

Slave Node: A slave node is a PTP-enabled network node which contains a Slave PTP clock and counter. A slave node is usually connected to a master node via a network connection. PTP is used to synchronize the slave PTP clock and counter to a master PTP clock and counter.

PTP Clock: A PTP clock is the source of an output clock signal which is locked to a PTP counter. In the DP83640, the local PTP clock operates at 250 MHz, and can be configured to control the CLK_OUT signal. This PTP CLK_OUT signal is programmable to frequencies which are integral divisions of the 250 MHz PTP clock in the range of 2 and 255 (125 MHz to 0.98 MHz).

PTP Counter: A PTP counter contains time information, and is locked to the PTP clock. In a master node, the PTP counter is the source of data used in the Precision Time Protocol for the purpose of synchronizing counters in PTP slave nodes. The PTP counter is incremented every 8 ns.

Local Reference Clock: A local reference clock is used for generating network traffic. The local reference clock is embedded into the transmit network packet traffic and is recovered from the network packet traffic at the receiver node. All Ethernet Physical Layer devices use local reference clock sources. Internally, the local reference clock in the DP83640 operates at 125 MHz.

In Synchronous Ethernet Mode the PTP logic (PTP clock and PTP counter) between master and slave are locked. But there is random phase error when power up. I don't think do a step adjustment (reg PTP_TDR) can align this kind phase error. The PTP clock is the source of clock output, and Divide-by N. I don't find any explain about **phase config** between PTP clock and clock output or PTP clock and PTP counter in TI file. You can't do phase adjust(PTP clock) by change the PTP counter.

So what am I missing? What is a correct way to phase align a CLK_OUT on master and between

master and slaves?

I have seen some similar questions on E2E

https://e2e.ti.com/support/interface/ethernet/f/903/t/261812?tisearch=e2e-sitesearch&keymatch=Phase%20alignment

https://e2e.ti.com/support/interface/ethernet/f/903/t/413987?tisearch=e2e-sitesearch&keymatch=Phase%20alignment

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