Schematic Review Form

Rafal

Pin #	Name	Info	Violations	*Description*
4	GRSTz	Tied to AND gate. Deasserted after 3.3V and 1.1V rails are high.		Global power reset. This reset brings all of the TUSB9261 internal registers to their default states. When GRSTz is asserted , the device is completely nonfuncitonal.
52	XI	Tied to external clock.		Crystal input. This terminal is the crystal input for the internal oscillator. The input may alternately be driven by the output of an external oscillator. When using a crystal, a 1-Mohm feedback resistor is required between XI and XO.
54	XO	Unconnected.		Crystal output. This terminal is the crystal output for the internal oscillator. If XI is driven by an external oscillator, this pin may be left unconnected. When using a crystal, a 1-Mohm feedback resistor is required between XI and XO.
31, 30	FREQSEL[1:0]	Configured by jumper settings.		Frequency select. These terminals indicate the oscillator input frequency and are used to configure the correct PLL multiplier. The field encoding is as follows: FREQSEL[1]=1, FREQSEL[0]=1, Input clock frequency=40Mhz.
57	SATA_TXP	10F caps to connector. Swapped with TX- by default.		Serial ATE transmitter differential pair (positive)
56	SATA_TXM	10F caps to connector. Swapped with TX- by default.		Serial ATE transmitter differential pair (negative)

60	SATA_RXP	10nF caps to connector. Straight to connector.		Serial ATE receiver differential pair (positive)
59	SATA_RXM	10nF caps to connector. Straight to connector.		Serial ATE receiver differential pair (negative)
43	USB_SSTXP	10nF caps. Schematic does not show connection.	Cannot review.	SuperSpeed USB transmitter differential pair (positive)
42	USB_SSTXM	10nF caps. Schematic does not show connection.	Cannot review.	SuperSpeed USB transmitter differential pair (negative)
46	USB_SSRXP	Schematic does not show connection.	Cannot review.	SuperSpeed USB transmitter differential pair (positive)
45	USB_SSRXM	Schematic does not show connection.	Cannot review.	SuperSpeed USB receiver differential pair (negative)
36	USB_DP	Schematic does not show connection.	Cannot review.	USB high-speed differential transceiver (positive)
35	USB_DM	Schematic does not show connection.	Cannot review.	USB high-speed differential transceiver (negative)
50	USB_VBUS	Uses resistor divider that is not recommended in datasheet, but should offer similar voltage.		USB bus power
38	USB_R1	Connected to USB_R1RTN by 10Kohm.		Precision resistor reference. A 10-kohm +1% resistor should be connected between R1 and R1RTN.
39	USB_R1RTN	Connected to USB_R1 by 10Kohm.		Precision resistor reference return.
17	SPI_SCLK	Connected to SN74HCT244 MUX to select external or on-board SPI.		SPI clock

18	SPI_DATA_OUT	Connected to SN74HCT244 MUX to select external or on-board SPI.		SPI master data out
20	SPI_DATA_IN	Connected to SN74HCT244 MUX to select external or on-board SPI.		SPI master data in
21	SPI_CS0	Connected to SN74HCT244 MUX to select external or on-board SPI.		Primary SPI chip select for flash RAM
23	SPI_CS2/GPIO11	Configured as SATA_FAULT. Pulled high by default.		SPI chip select for additional peripherals. When not used for SPI chip select, this pin may be used as a general-purpose I/O.
22	SPI_CS1/GPIO10	Configured as SATA_EN.		SPI chip select for additional peripherals. When not used for SPI chip select, this pin may be used as a general-purpose I/O.
25	JTAG_TCK	Floating		JTAG test clock
26	JTAG_TDI	Floating		JTAG test data in
27	JTAG_TDO	Floating		JTAG test data out
28	JTAG_TMS	Floating		JTAG test mode select
29	JTAG_TRSTz	Floating		JTAG test reset
6	GPIO9/UART_TX	Configured as UART Tx.		GPIO/UART transmitter. This terminal can be configured as a GPIO or as the transmitter for a UART channel. This pin defaults to a general-purpose output.
5	GPIO8/UART_RX	Configured as UART Rx.		GPIO/UART receiver. This terminal can be configured as a GPIO or as the receiver for a UART channel. This pin defaults to a general-purpose output.

16	GPIO7	Configured as SATA_SS_Connect.		Configurable as a general-purpose inputs/outputs.
15	GPIO6	Configured as SATA_HS_FS_Connect.		Configurable as a general-purpose inputs/outputs.
14	GPIO5	Configured as SATA_PWR_STATE_1.		Configurable as a general-purpose inputs/outputs.
13	GPIO4	Configured as SATA_SELF_PWR.		Configurable as a general-purpose inputs/outputs.
11	GPIO3	Configured as SATA_PBUTTON.		Configurable as a general-purpose inputs/outputs.
10	GPIO2	Configured as SATA_HS_FS_SUSPEND.		Configurable as a general-purpose inputs/outputs.
9	GPIO1	Configured as SATA_PWR_STATE_0.		Configurable as a general-purpose inputs/outputs.
8	GPIO0	Configured as SATA_SW_HB.		Configurable as a general-purpose inputs/outputs.
2	PWM0	Configured as SATA_HDD_ACT.		Pulse-width modulation (PWM). Can be used to drive status LEDs.
3	PWM1	SATA_MISC_LED.		Pulse-width modulation (PWM). Can be used to drive status LEDs.
1, 12, 19, 32, 33, 42, 47, 49, 55, 61, 63	VDD	Connected to 1.1V power with bypass caps. No ferrite bead.		1.1-V power rail
7, 24, 51	VDD33	Connected to 1.1V power with bypass caps. No ferrite bead.		3.3-V power rail
34, 40, 48, 62	VDDA33	Connected to 1.1V power with bypass caps. No ferrite bead.		3.3-V analog power rail

53	VSSOSC	Connected to PCB ground.		Oscillator ground. If using a crystal, this should not be connected to a PCB ground plane. If using an oscillator, this should be connected to PCB ground. See Clock Source Requirements for more details.
44, 58	VSS	Connected to GND.		Ground
65	VSS	Connected to GND.		Ground - Thermal pad
37, 64	NC	Floating.		No connect, leave floating

Comments

```
Not final review.  Investigation is still ongoing.
```