Register Set Value

Device Address	Register Address	Value		Comment
		Not Optimized	Optimized	
0x07	0x0000	0x2000		Disable Auto Negotiation
0x01	0x0096	0x0000		Disable Link Training start-up protocol
0x1E	0x0004	0xD500	0x5540	See Table below

* All registers except above is set default.

Table 8-7. HS_SERDES_CONTROL_3

Device Address: 0x1E	Register Address:0x0004	Default:0x1500	
Bit(s)	**Name**	**Description**	**Access**
15	HS_ENTRACK (RXG)	HSRX ADC Track mode. 0 = Normal operation (Default 1'b0) 1 = Forces ADC into track mode	RW
14:12	HS_EQPRE[2:0] (RXG)	Serdes Rx precursor equalizer selection 000 = 1/9 cursor amplitude 001 = 3/9 cursor amplitude (Default 3'b001) 010 = 5/9 cursor amplitude 011 = 7/9 cursor amplitude 100 = 9/9 cursor amplitude 101 =11/9 cursor amplitude 110 = 13/9 cursor amplitude 111 = Disable	RW
11:10	HS_CDRFMULT[1:0] (RXG)	Clock data recovery algorithm frequency multiplication selection (Default 2'b01) 00 = First order. Frequency offset tracking disabled 01 = Second order. 1x mode 10 = Second order. 2x mode 11 = Reserved	RW
9:8	HS_CDRTHR[1:0] (RXG)	Clock data recovery algorithm threshold selection (Default 2'b01) 00 = Four vote threshold 01 = Eight vote threshold 10 = Sixteen vote threshold 11 = Thirty two vote threshold	RW
7	RESERVED	For TI use only (Default 1'b0)	RW
6	HS_PEAK_DISABLE (RXG)	HS Serdes PEAK_DISABLE control 0 = Normal operation (Default 1'b0) 1 = Disables high frequency peaking. Suitable for <6 Gbps operation	RW
5	HS_H1CDRMODE (RXG)	HS_Serdes H1CDRMODE control 0 = Normal operation (Default 1'b0) 1 = Enables CDR mode suitable for short channel operation.	RW
4:0	HS_TWCRF[4:0] (RXG)	Cursor Reduction Factor (Default 5'b00000). Refer to Table 8-8.	RW

Not optimized : ADC into track mode
Optimized : Normal operation

Not optimized : Enable
Optimized : Disable