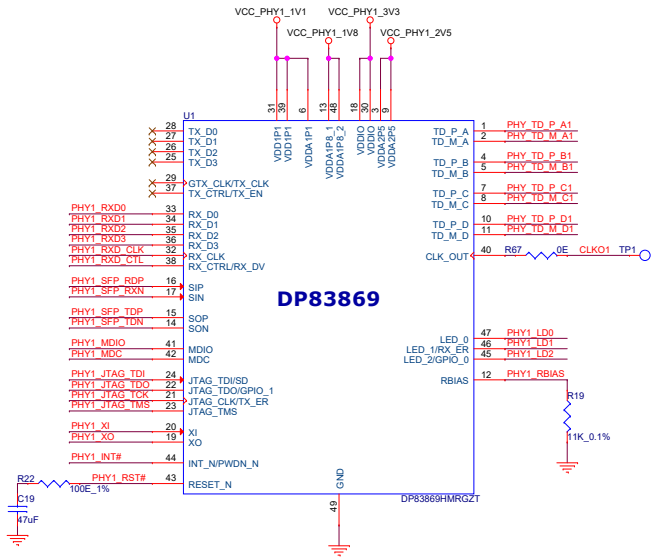
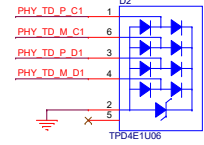
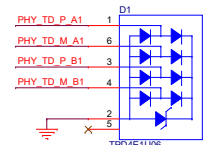


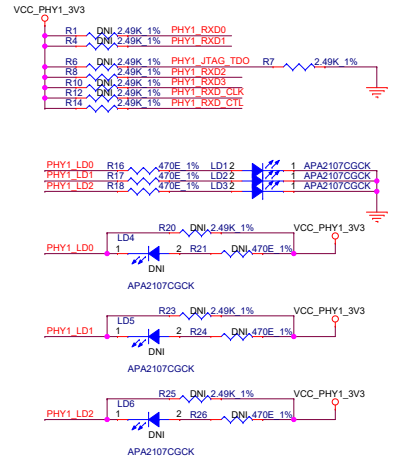
GIGABIT ETHERNET PHY 1



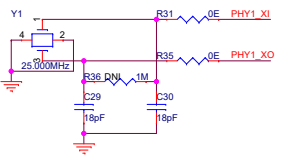
Protection Diodes



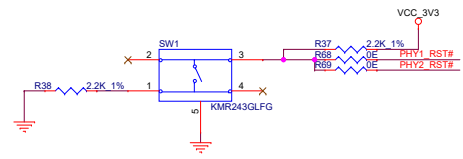
Hardware Strap Configuration



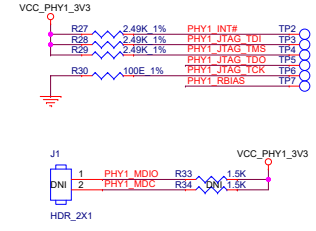
Crystal



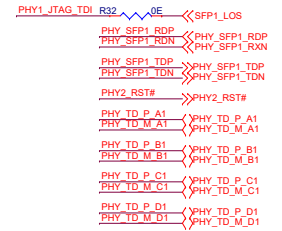
Reset Switch



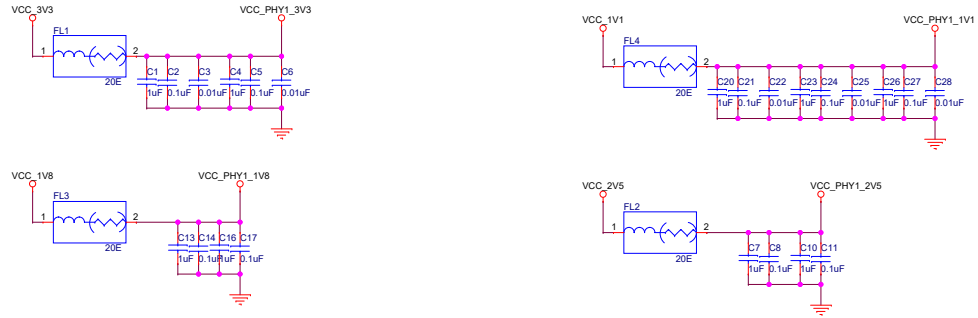
Debug & Test Points



Off-Page Connections



Power Supply Input & Decaps



Cad Note: Place the Decaps close to each power pins

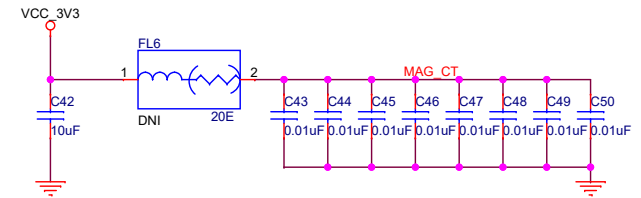
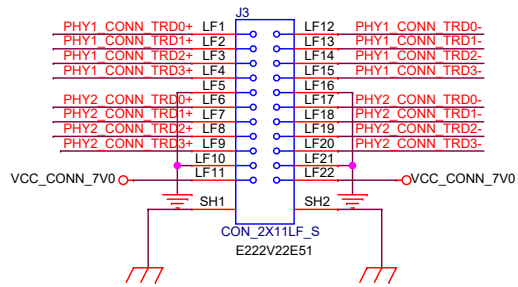
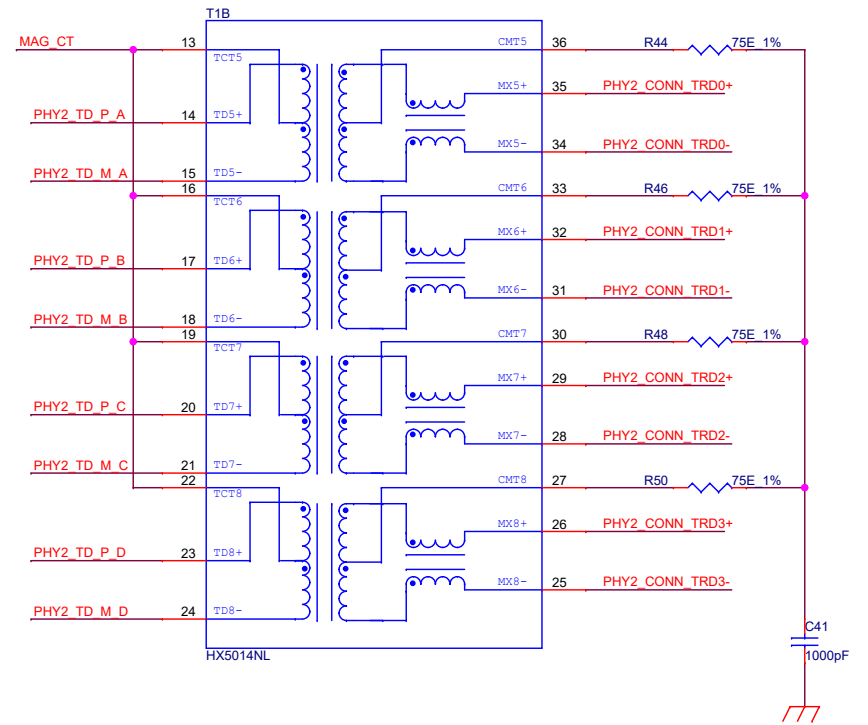
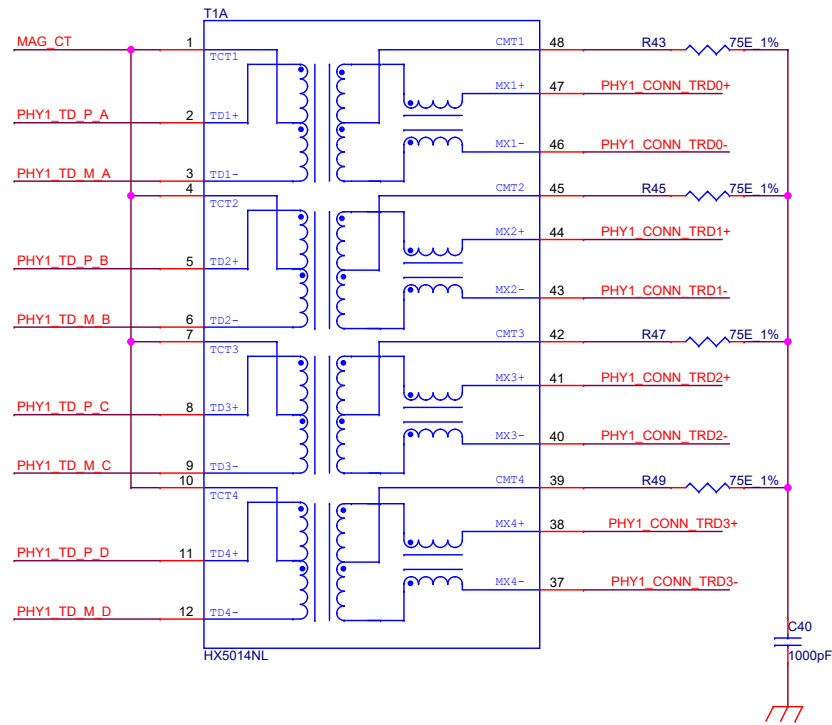
Hardware Strap Configuration

Net Name	Configuration	Summary
PHYx_RXD0	Open	PHY_ADD[1:0] : 00
PHYx_RXD1	Open	PHY_ADD[3:2] : 00
PHYx_JTAG_TDO	PD (0)	OPMODE_0 : 0
PHYx_RXD2	PU (1)	OPMODE_2 : 1
PHYx_RXD3	PD (0)	OPMODE_1 : 0
PHYx_RXD_CLK	PD (0)	Link Loss Pass Thru Enabled
PHYx_RXD_CTL	PU (1)	Copper: Mirror Enable
PHY1_LD0	PD (0)	Fiber Auto Negotiation
PHY1_LD1	PD (0)	ANEGSEL_0 : 0
PHY1_LD2	PD (0)	ANEGSEL_1 : 0

OPMODE_[2:0] : 100
1000Base-T to 1000Base-X

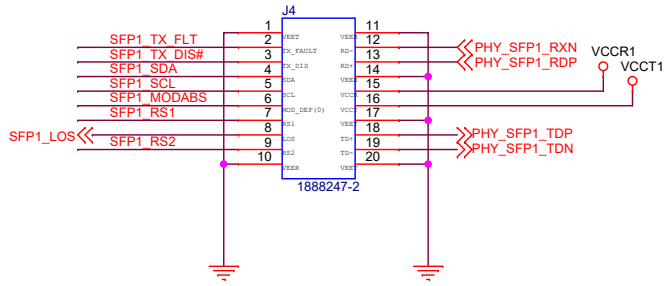
ANEGSEL[1:0] : 00
Copper:Auto-negotiation (1000/100 Advertised), Auto MDIX

MAGNETICS & I/O CONNECTOR

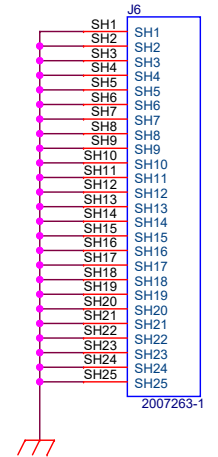
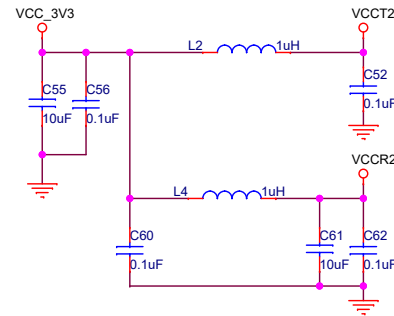
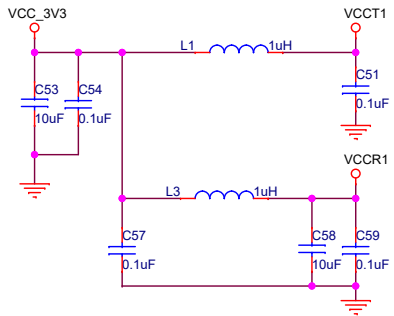
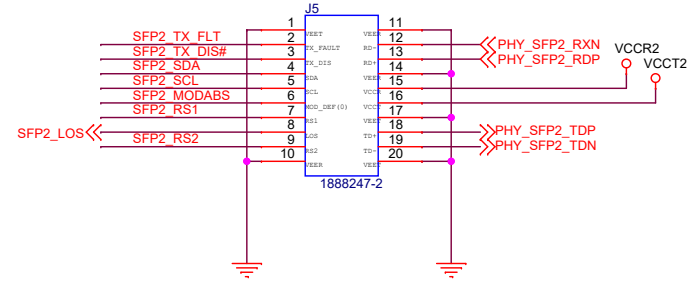


SFP CAGE & CONNECTOR

SFP 1 CONNECTOR & CAGE



SFP 2 CONNECTOR & CAGE



Cad Note: Place the Decaps close to each power pins

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