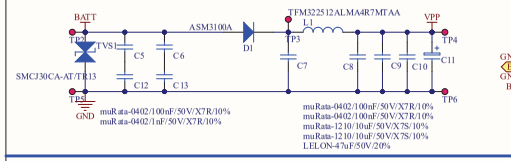
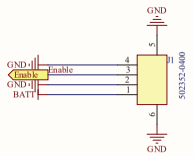
文件编号：MSYF-MPR-007-36
文件版本：A02

电源输入端滤波电路

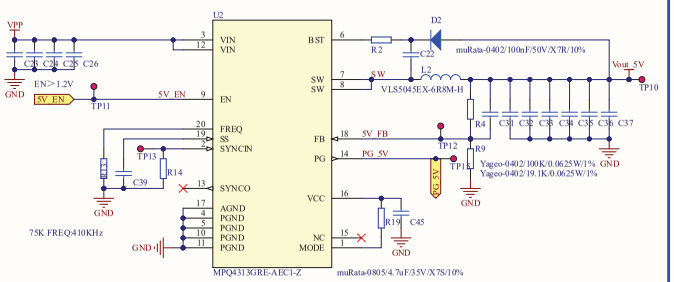


输入接插件

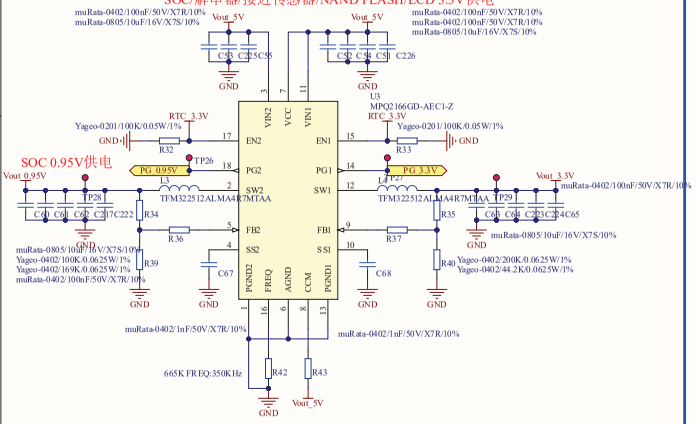


一级 5V供电电路

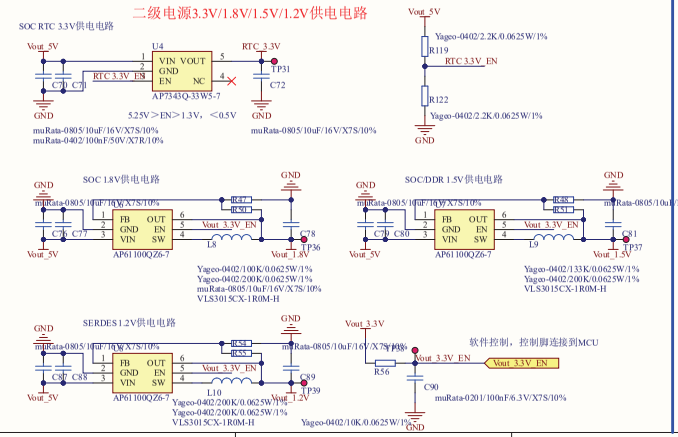
muRata-12 10/10uF/50V/X7S/10%
muRata-12 10/10uF/50V/X7S/10%
muRata-0402/100nF/50V/X7R/10%
muRata-0402/100nF/50V/X7R/10%



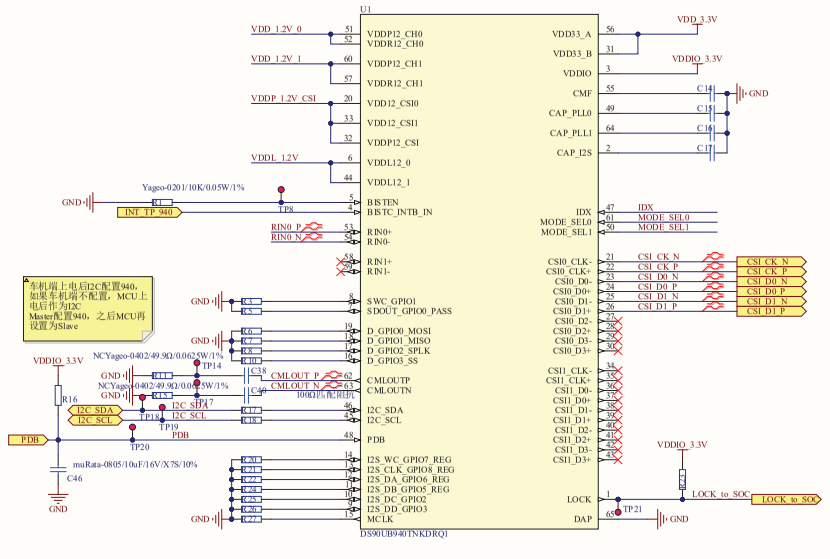
SOC/解串器/接近传感器/NAND FLASH/LCD 3.3V供电

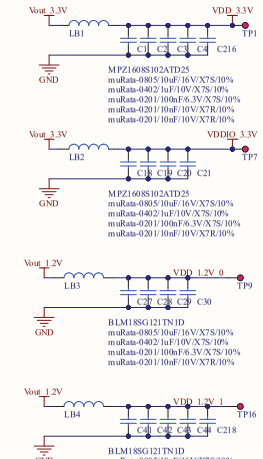


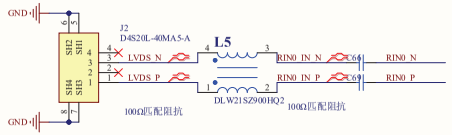
二级电源3.3V/1.8V/1.5V/1.2V供电电路

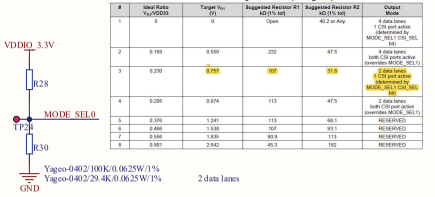


解串器电路









#	Ideal Ratio V_{IN}/VDD33	Target V_{IN} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	Output Mode
1	0	0	Open	40.2 or Any	4 data lanes 1 CSI port active (determined by MODE_SEL0 and MODE_SEL1)
2	0.169	0.559	232	47.5	4 data lanes both CSI ports active (overrides MODE_SEL1)
3	0.230	0.757	107	31.6	2 data lanes 1 CSI port active (determined by MODE_SEL0 and MODE_SEL1)
4	0.295	0.974	113	47.5	2 data lanes both CSI port active (overrides MODE_SEL1)
5	0.370	1.241	113	68.1	RESERVED
6	0.466	1.539	107	93.1	RESERVED
7	0.556	1.835	90.9	113	RESERVED
8	0.801	2.642	45.3	182	RESERVED

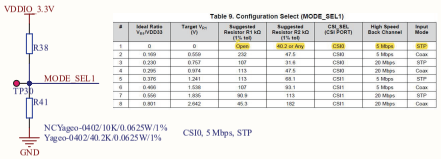
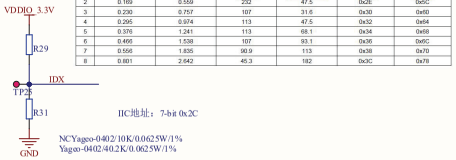


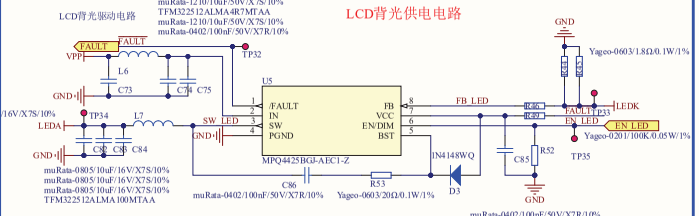
Table 9. Configuration Select (MODE_SEL1)

#	Ideal Ratio V_{IN}/VDD33	Target V_{IN} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	CSI_SEL (CSI PORT)	High Speed Back Channel	Input Mode
1	0	0	Open	40.2 or Any	CSI0	5 Mbps	STP
2	0.169	0.559	232	47.5	CSI0	5 Mbps	Coax
3	0.230	0.757	107	31.6	CSI0	20 Mbps	STP
4	0.295	0.974	113	47.5	CSI0	20 Mbps	Coax
5	0.370	1.241	113	68.1	CSI1	5 Mbps	STP
6	0.466	1.539	107	93.1	CSI1	5 Mbps	Coax
7	0.556	1.835	90.9	113	CSI1	20 Mbps	STP
8	0.801	2.642	45.3	182	CSI1	20 Mbps	Coax



#	Ideal Ratio V_{IN} / VDD33	Ideal V_{IN} (V)	Suggested Resistor R1 kΩ (1% tol)	Suggested Resistor R2 kΩ (1% tol)	7-bit Address	8-bit Address
1	0	0	Open	40.2 or 10	0x2C	0x58
2	0.169	0.559	232	47.5	0x2E	0x5C
3	0.230	0.757	107	31.6	0x30	0x60
4	0.295	0.974	113	47.5	0x32	0x64
5	0.370	1.241	113	68.1	0x34	0x68
6	0.466	1.538	107	93.1	0x36	0x6C
7	0.556	1.835	90.9	113	0x38	0x70
8	0.801	2.642	45.3	182	0x3C	0x78

LCD背光供电电路



项目 ITEM	签名 SIGN	日期 DATE	
设计 DE	Author	2024/4/25	研发中心 R&D Center
审核 AUDIT	Checked by	2024/4/25	工程名称 PRJ Name
批准 APP	Approved by	2024/4/25	HS11_B_Pilar_Board-SCH_20240129_V00.0.PrjPcb
页码 SHEET NO.	1 / 4		图纸名称 SCH Name
			HS11_B_Pilar_Board-SCH1_20240129_V00.0.SchDoc