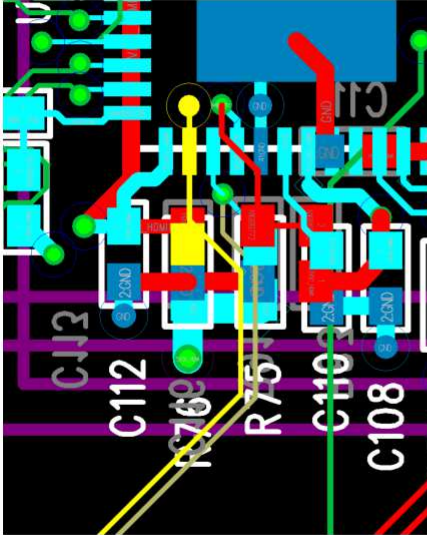
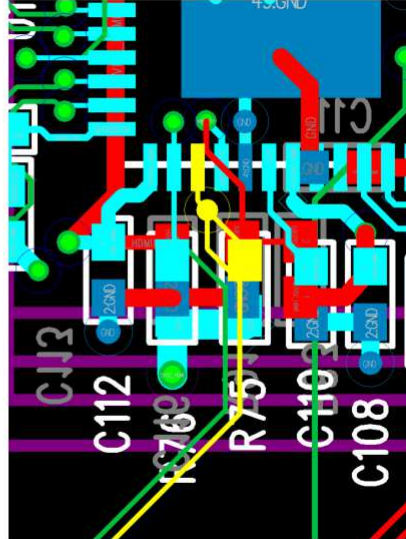


## SINK SCL AND SDA:

SCL highlighted in yellow:

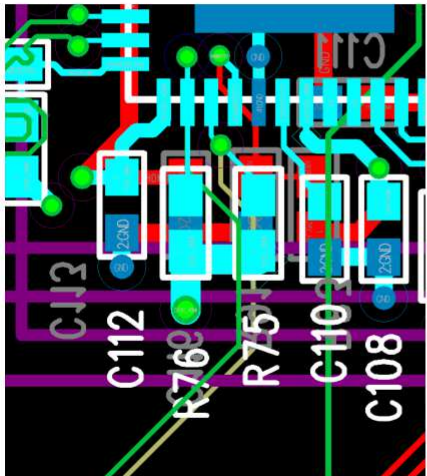


SDA highlighted in yellow:



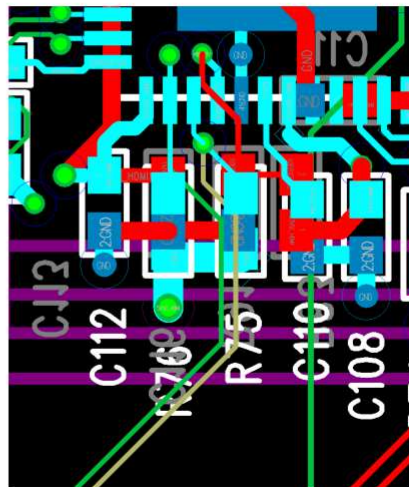
SCL

from top layer, down to layer 3.  
layer 3 is adjacent to a gnd plane.

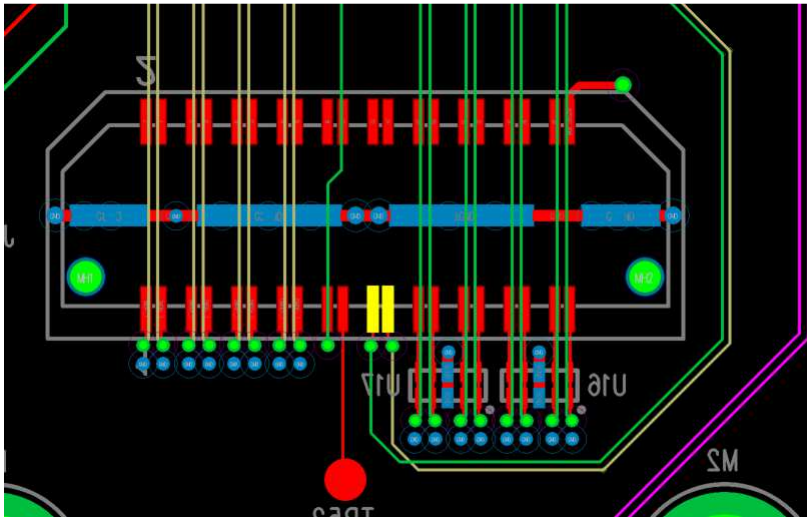


SDA

from top layer, down to layer 8.  
layer 8 is adjacent to a gnd plane.



Both route to a pins on a high speed differential connector --- transfers to pins on bottom layer:



The difference in length is 101.5 mils:

Property	Value
Net	HDMI_TO_FPGA_CONN_SCL
Connection	R76.2-U18.38
Layout Data	
Unrouted Length	0
Routed Length	4820.26
Via Count	2
Capacitance (pf)	16.66
Impedance (ohm)	50 - 78
Delay (ns)	0.840
Rules Data	
Class	Net
Rule Hierarchy	Net
Trc/Trc Clearance	7.89
Width	4
Trace Width	4

Property	Value
Net	HDMI_TO_FPGA_CONN_SDA
Connection	J8.23-U18.39
Layout Data	
Unrouted Length	0
Routed Length	4718.72
Via Count	2
Capacitance (pf)	18.06
Impedance (ohm)	45 - 78
Delay (ns)	0.817
Rules Data	
Class	Net
Rule Hierarchy	Net
Trc/Trc Clearance	7.89
Width	4
Trace Width	4

SOURCE SCL AND SDA (pads on IC highlighted in yellow):

