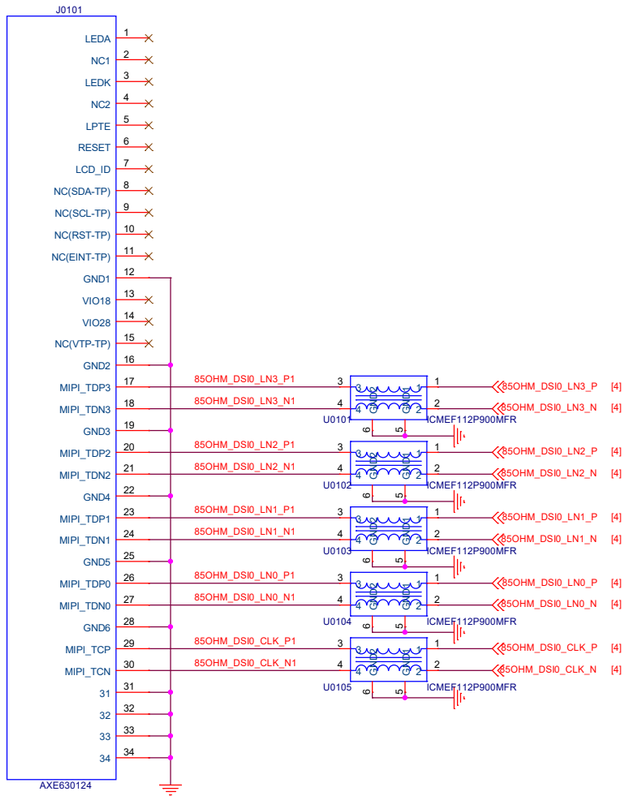
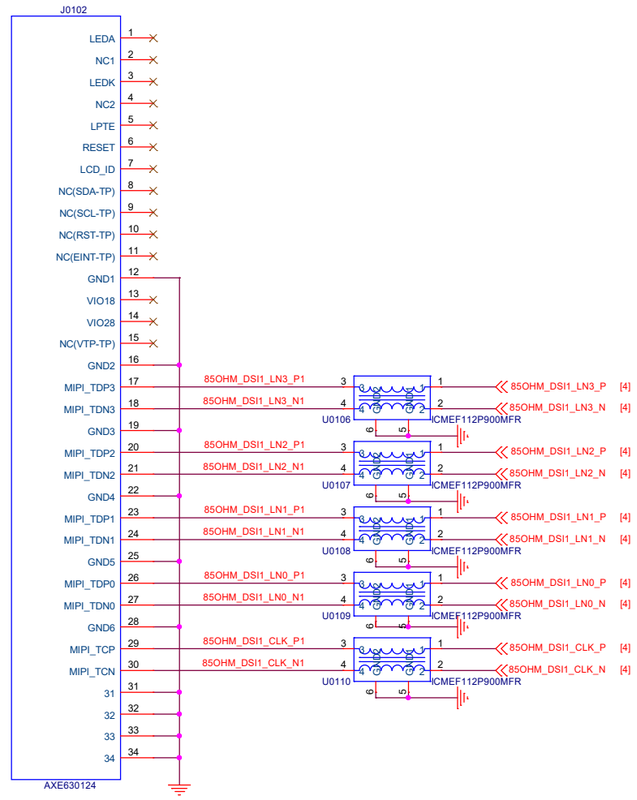
LCM1



LCM2



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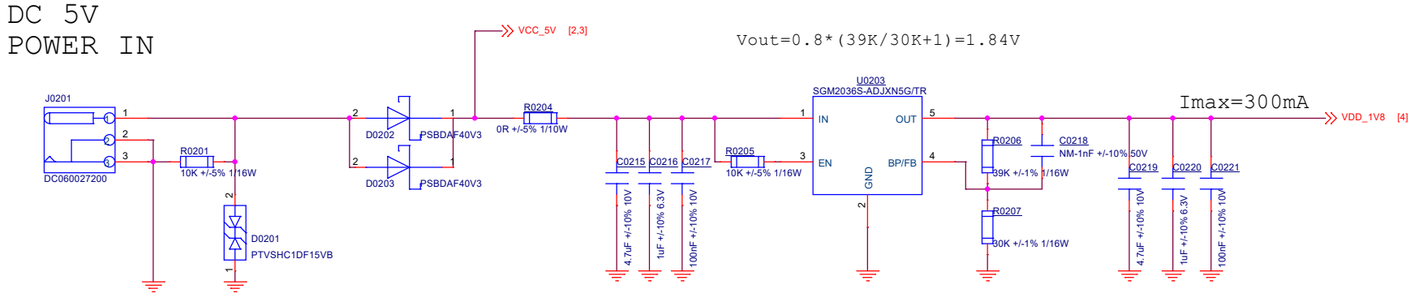
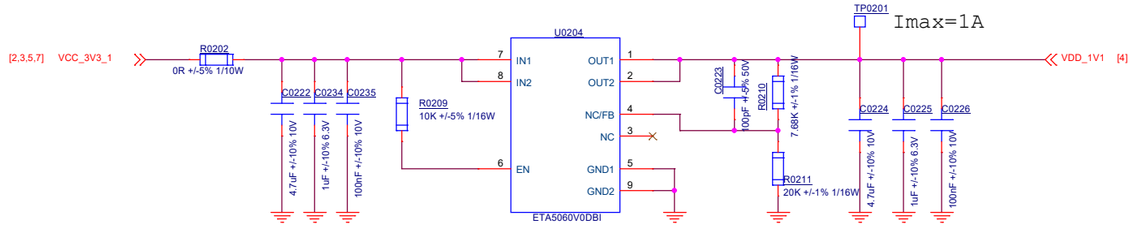
UB941 POWER

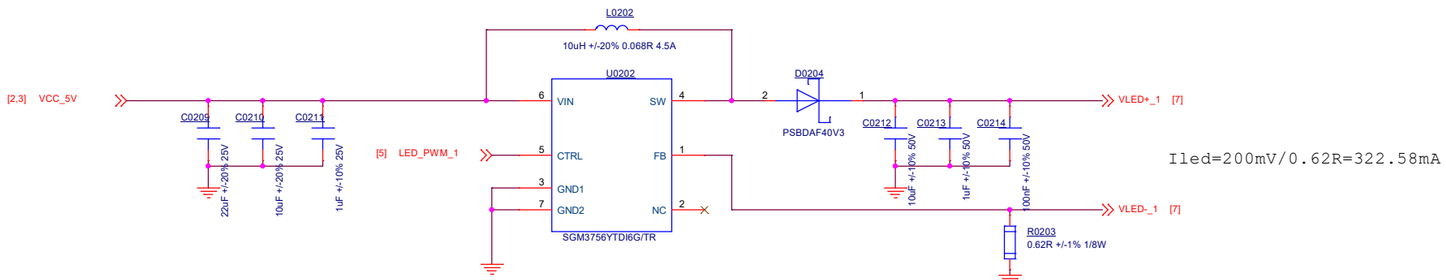
DC 5V
POWER IN

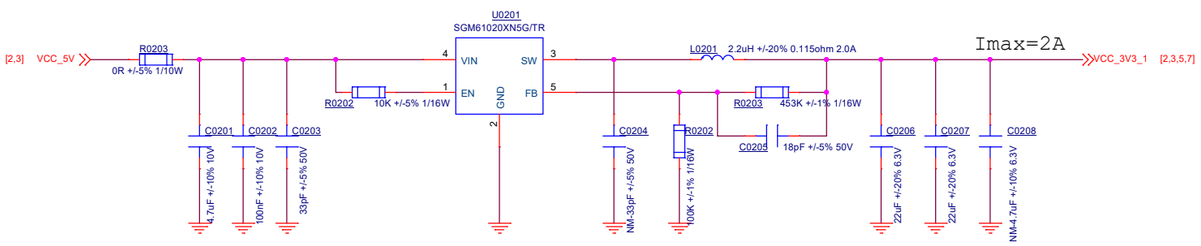


Vout=0.8*(1+7.68k/20k)=1.107V

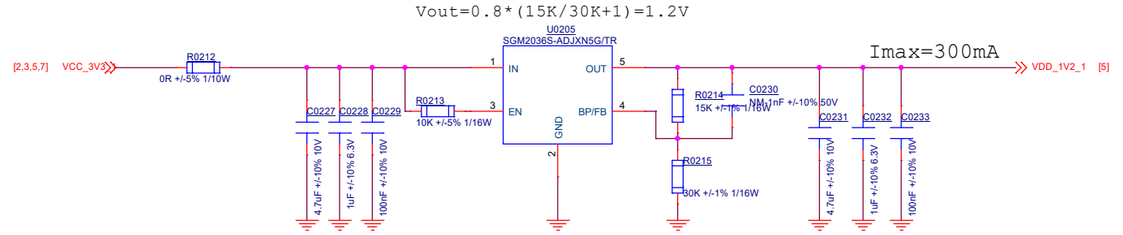


UB948-1 POWER





Vout=0.8*(15K/30K+1)=1.2V



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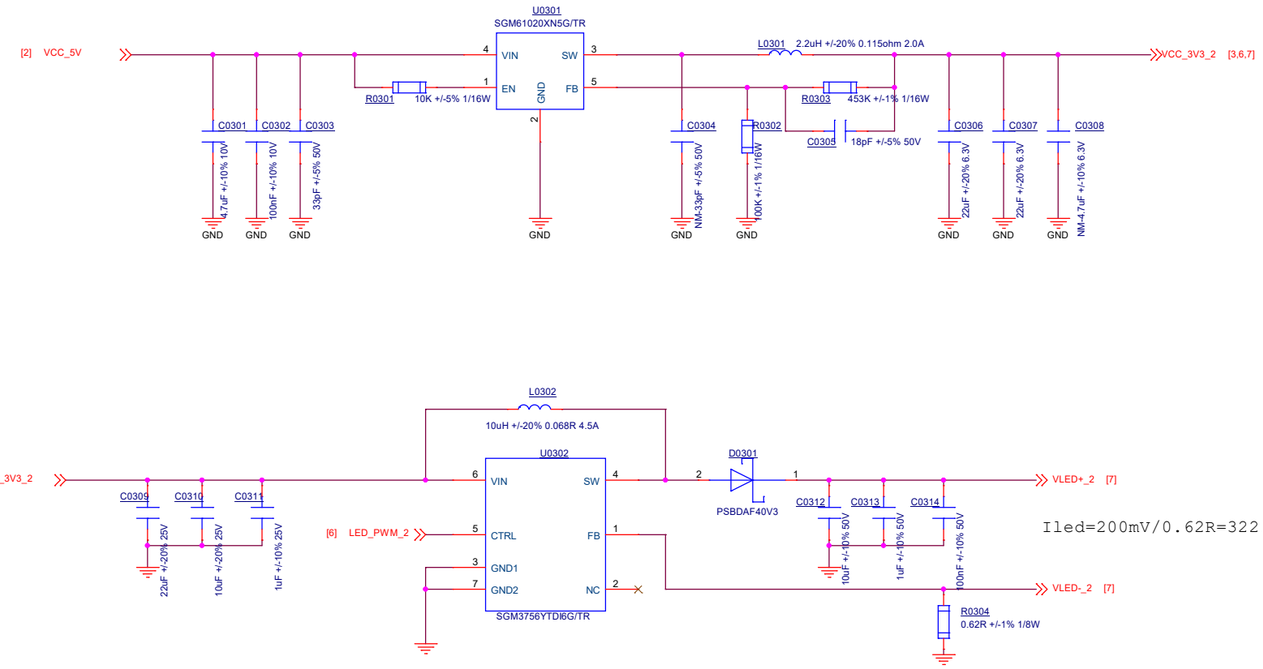
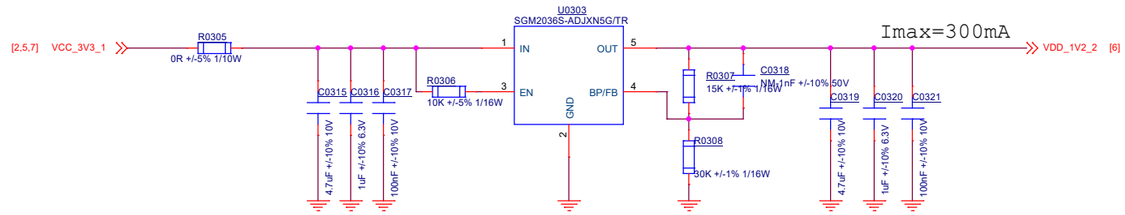
UB948-2 POWER



Vout=0.8*(15K/30K+1)=1.2V



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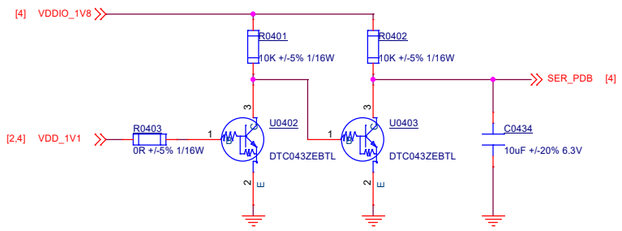
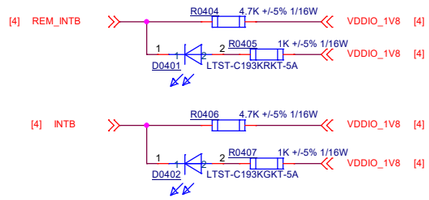
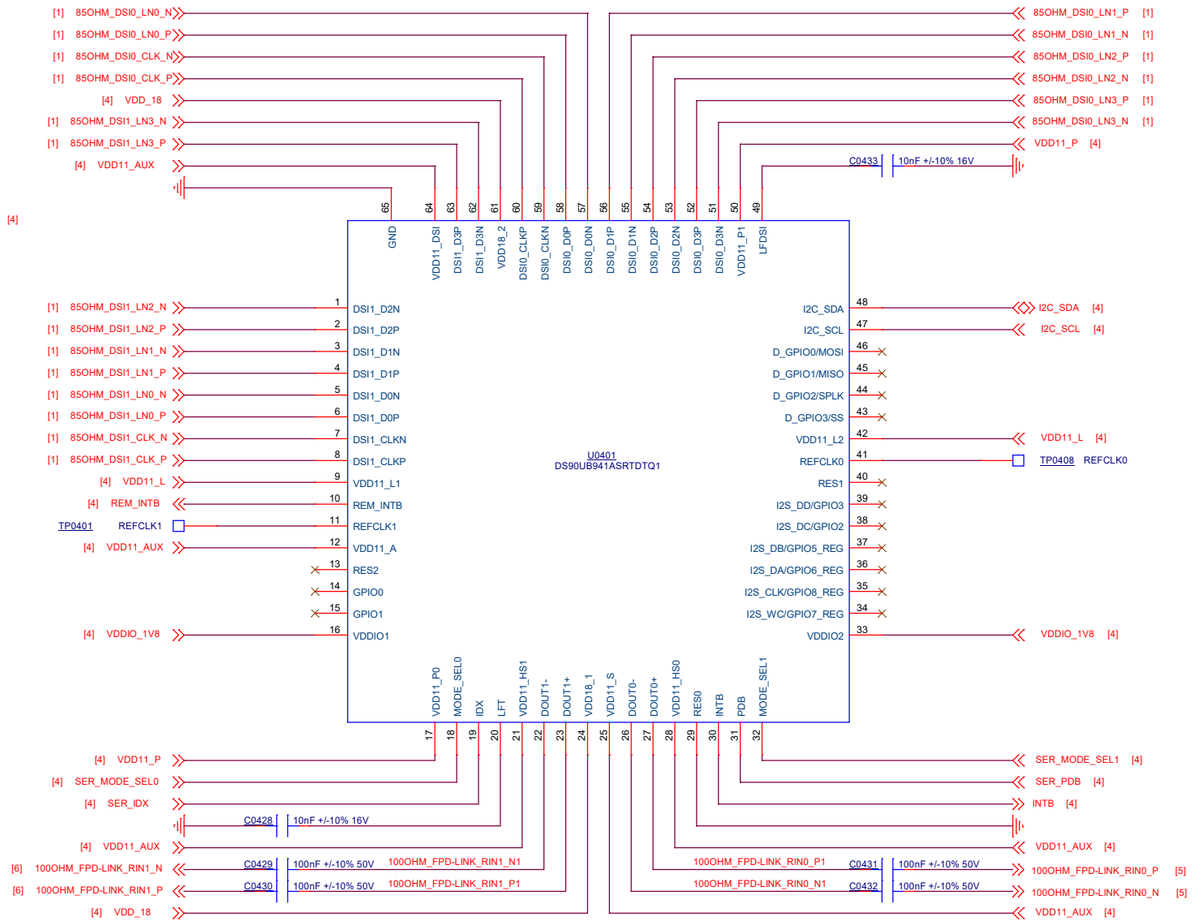
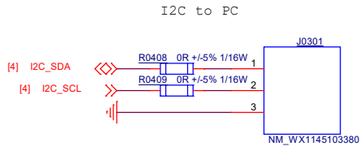
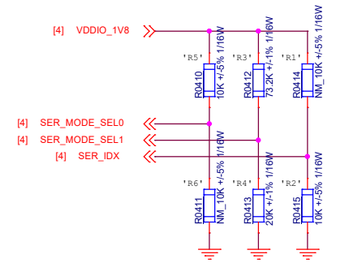




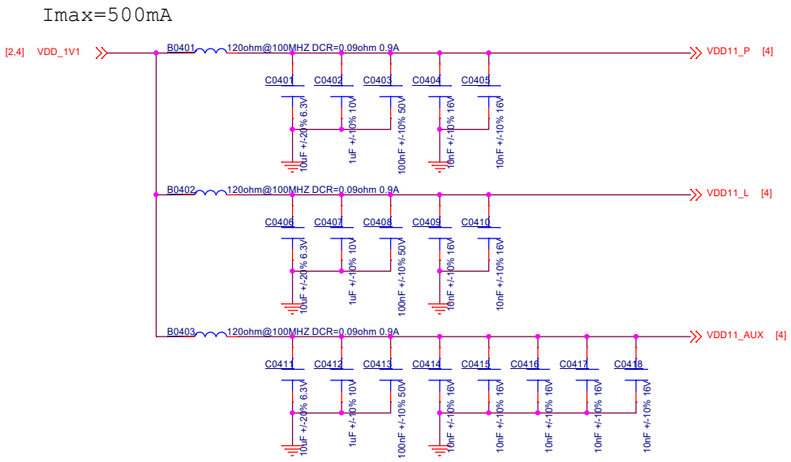


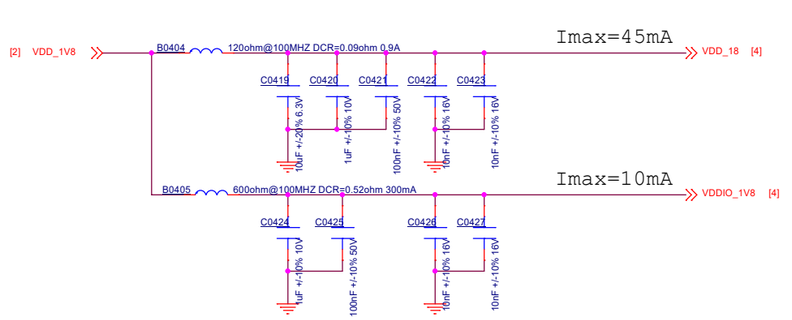




VIDX TARGET VOLTAGE Y (VDD18)	SUGGESTED STRAP RESISTORS (1% TOL) R1 (kΩ)	R2 (kΩ)	ASSIGNED I2C ADDRESS 7-BIT	8-BIT
0	OPEN	10	0x0C	0x18
0.384	73.2	20	0x0E	0x1C
0.589	60.4	30.1	0x10	0x20
0.793	51.1	40.2	0x12	0x24
0.999	40.2	51.1	0x14	0x28
1.208	30.1	61.9	0x16	0x2C
1.417	18.7	71.5	0x18	0x30
1.8	10	OPEN	0x1A	0x34

MODE	SETTING	FUNCTION
DSI LANES	00	1 Lane
	01	2 Lanes
	10	3 Lanes
	11	4 Lanes
SPLITTER Mode	0	DSI inputs enabled.
	1	DSI inputs disabled. This is a recommended strap option as any configuration of DSI inputs needs to be done while the inputs are disabled.
COAX Mode	0	Enable FPD-Link III for twisted pair cabling.
	1	Enable FPD-Link III for coaxial cabling.
CLOCK Mode	0	FPD-Link III is generated from DSI clock. The DSI clock has to be continuous.
	1	FPD-Link III is generated from external oscillator provided to REFCLK pin(s). The DSI clock may be continuous or discontinuous





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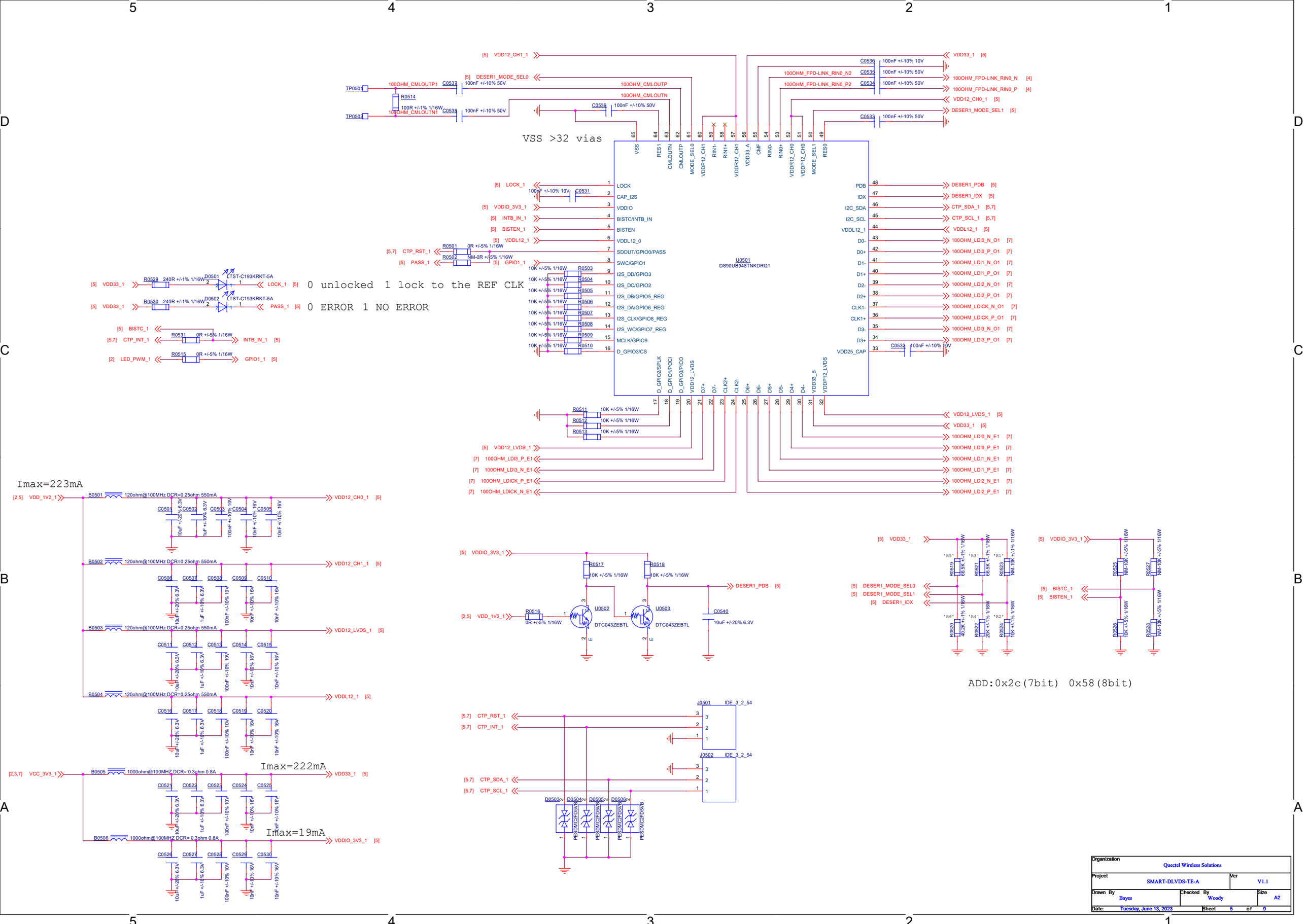
VSS >32 vias
U0501
DS90UB948TNKDRQ1
0 unlocked 1 lock to the REF CLK
0 ERROR 1 NO ERROR
Imax=223mA
Imax=222mA
Imax=19mA
ADD:0x2c(7bit) 0x58(8bit)
Organization
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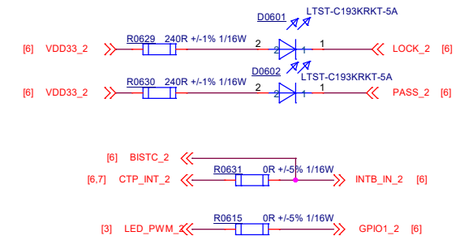
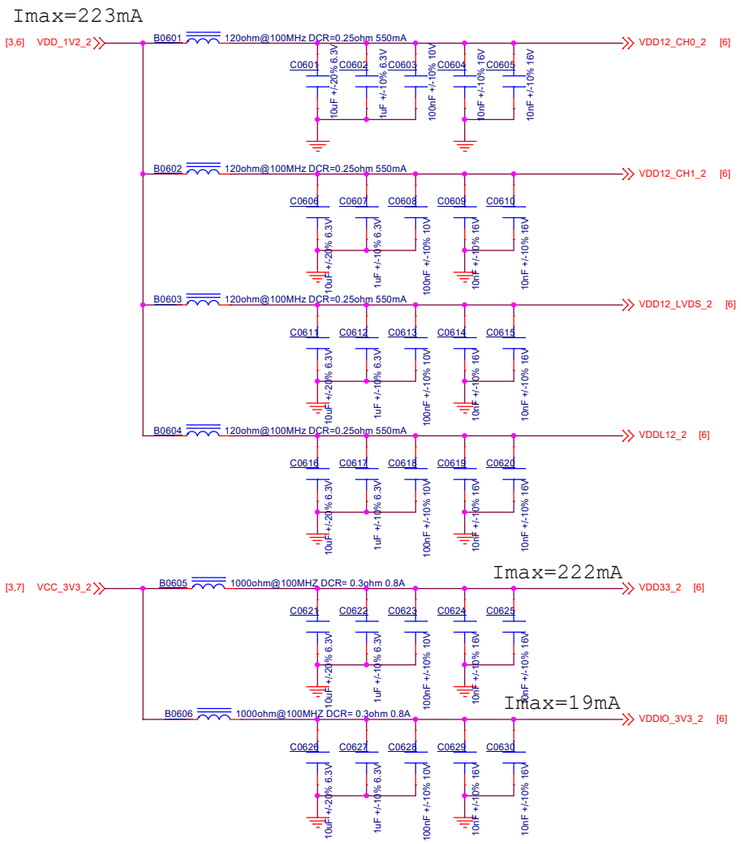
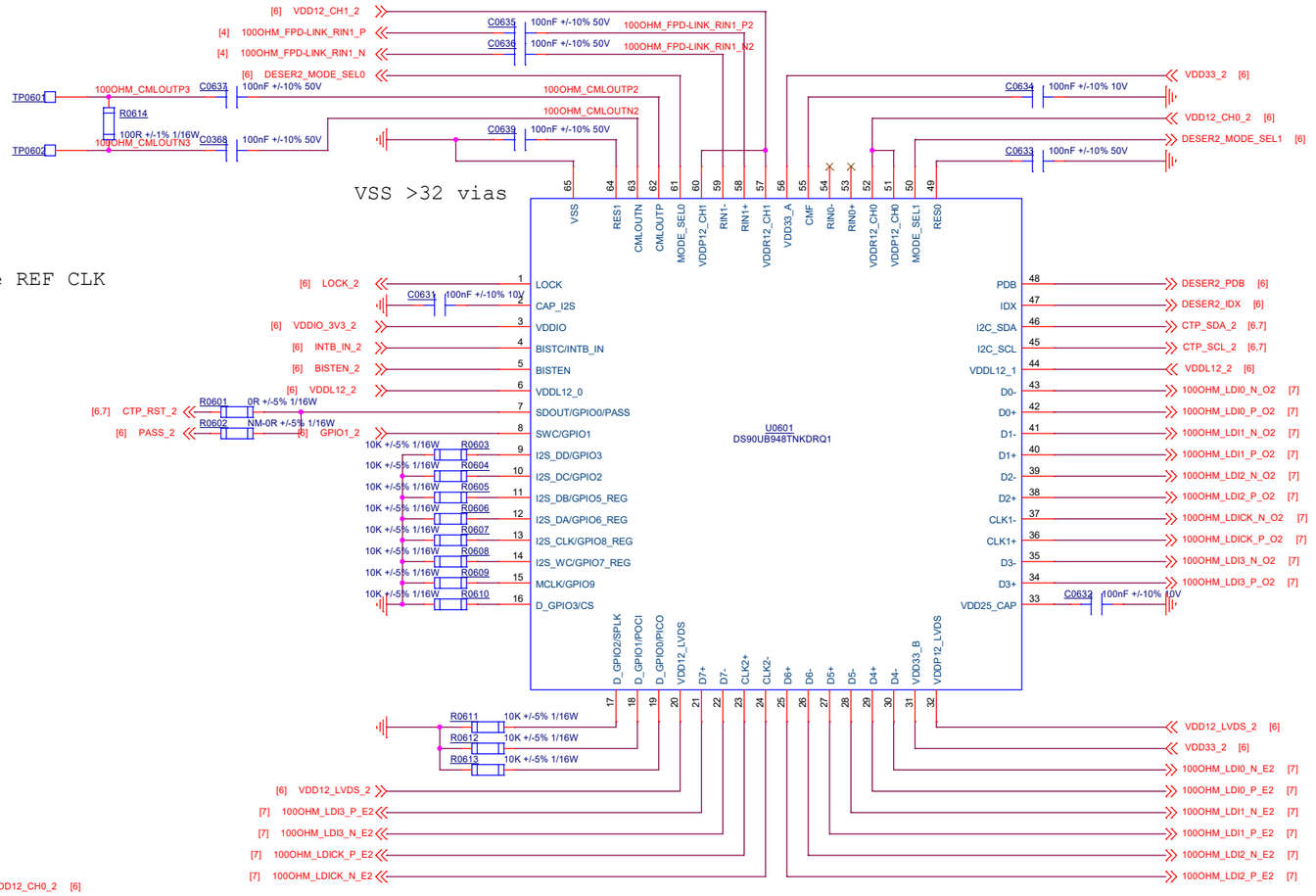


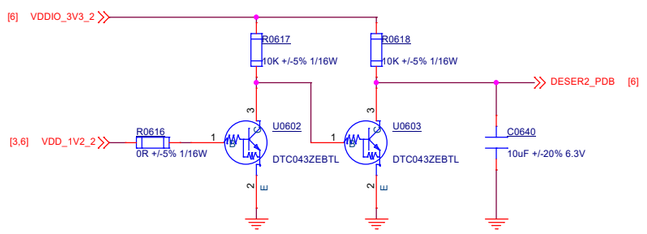
1 lock to the REF CLK
0 unlocked

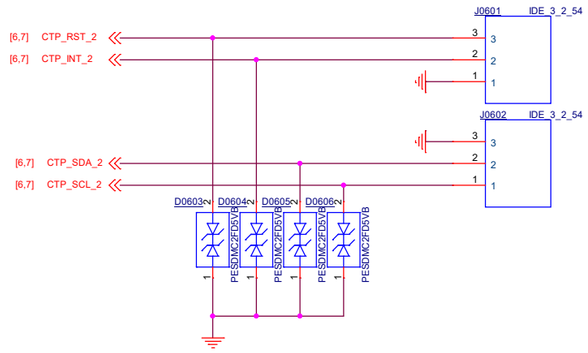
1 NO ERROR
0 ERROR

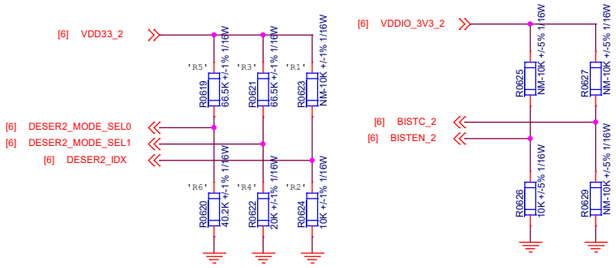
Imax=223mA











ADD:0x2c(7bit) 0x58(8bit)

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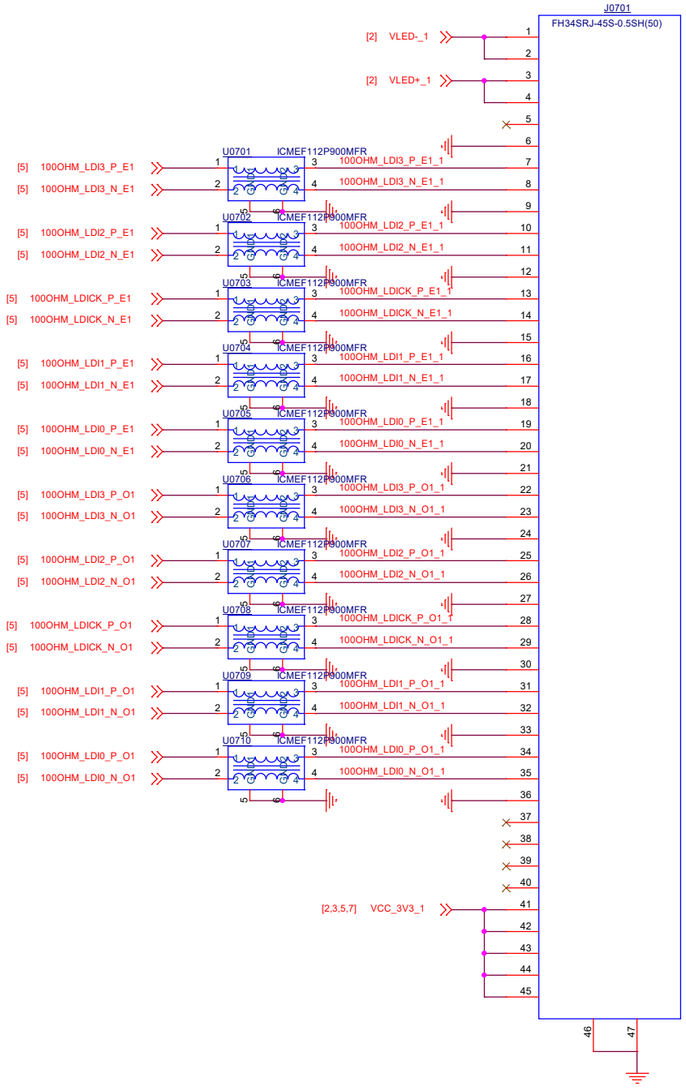
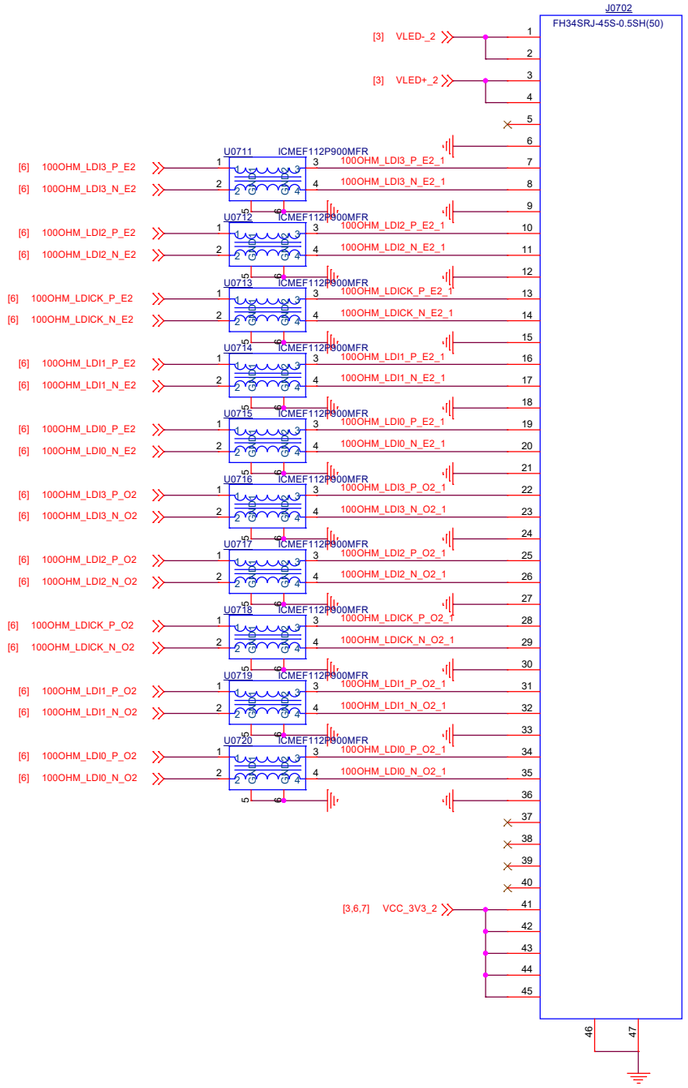
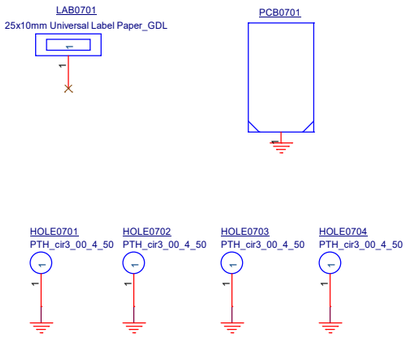
LVDS

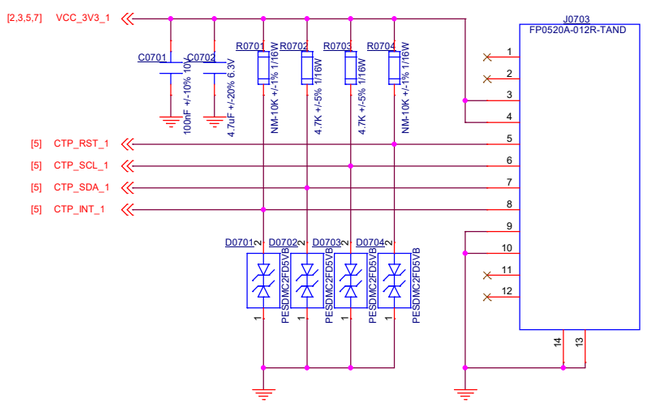




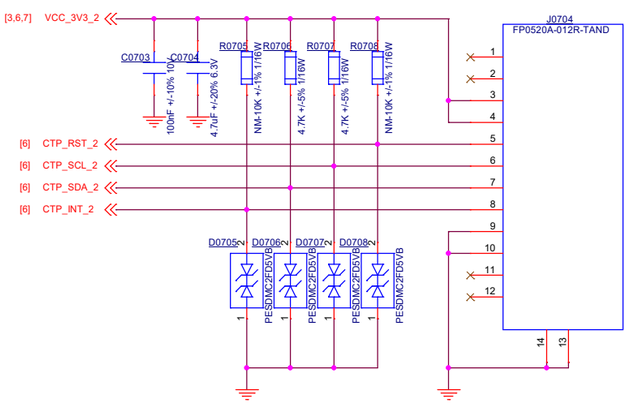


TP

Imax=300mA TP ADD:0x20



Imax=300mA TP ADD:0x20



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