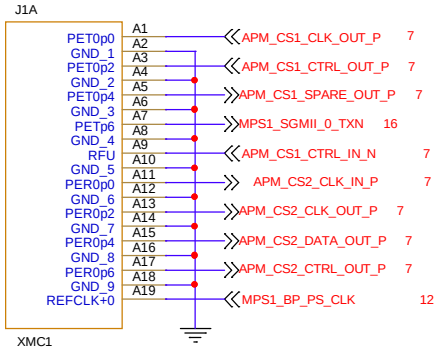
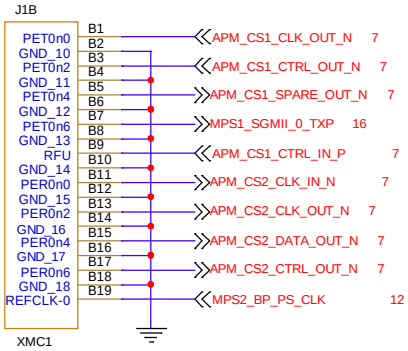
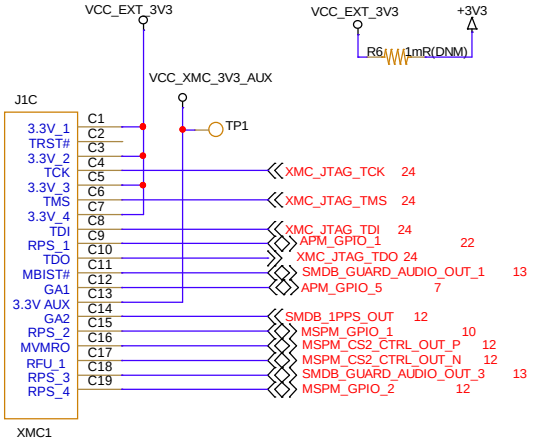
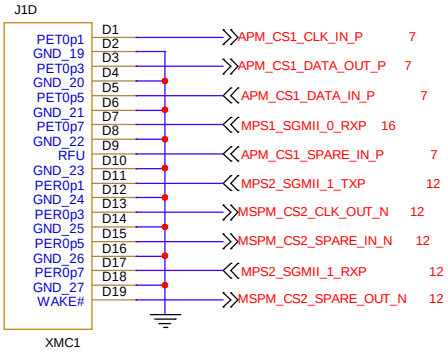
note: part# need to update for XMC1

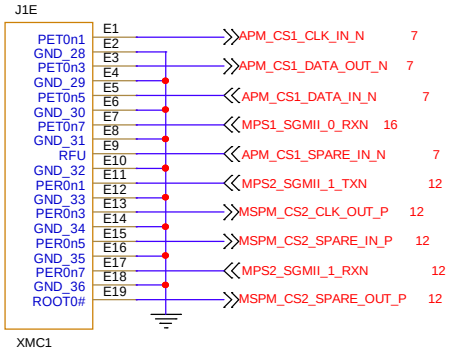
XMC_INTERFACE_CONN_1

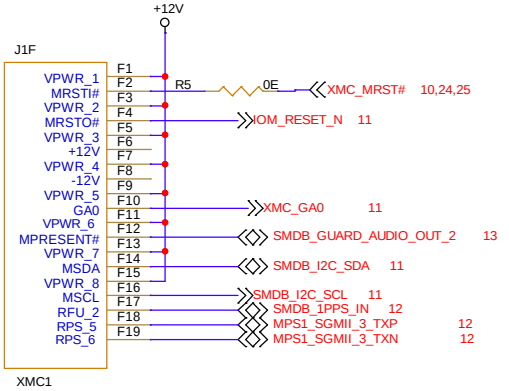












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Size: B	Document Number: <Doc>	Rev: 1.0
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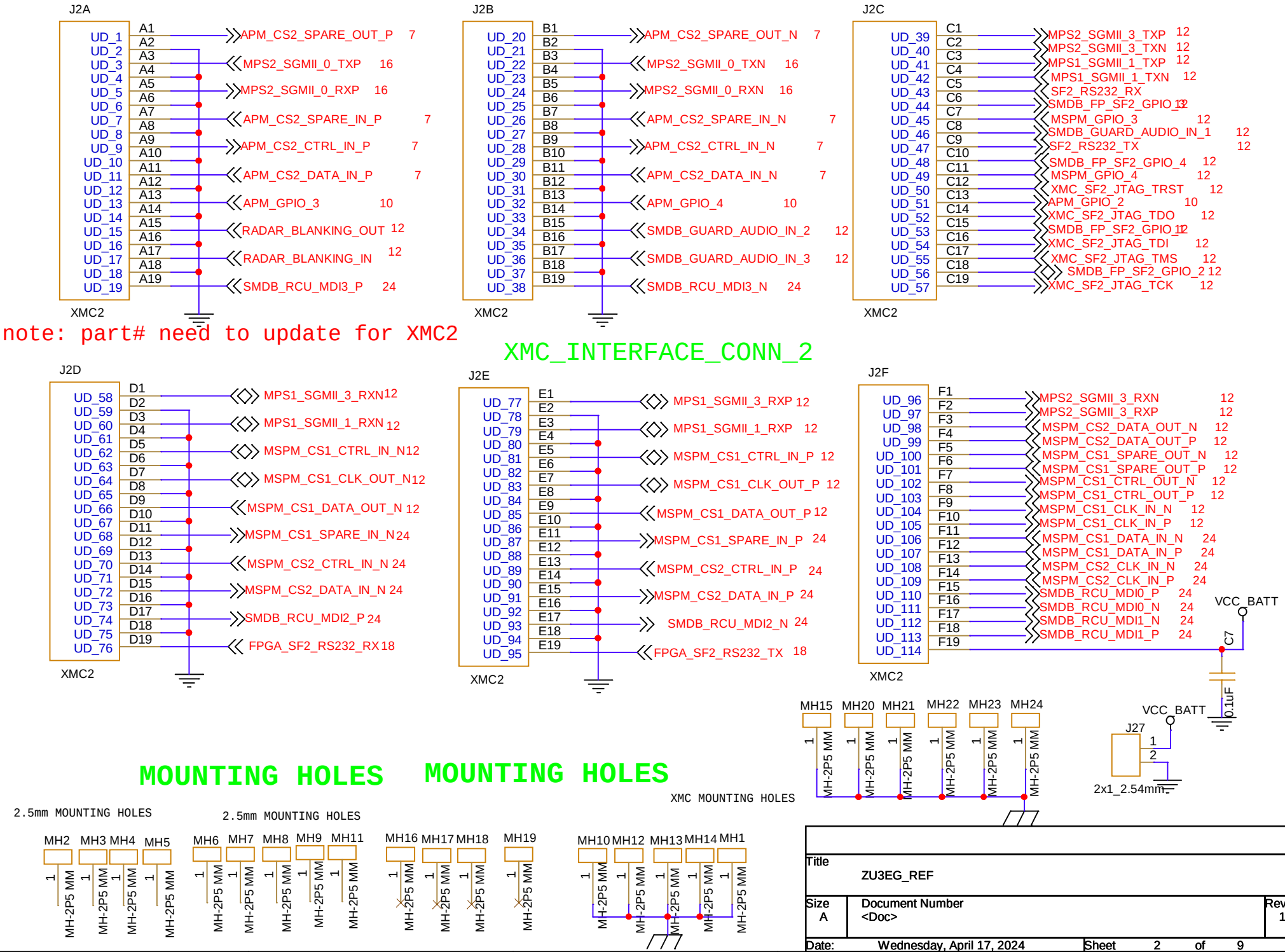
J2A
XMC2
J2B
XMC2
J2C
XMC2
note: part# need to update for XMC2
XMC_INTERFACE_CONN_2
J2D
XMC2
J2E
XMC2
J2F
XMC2
VCC_BATT
C7
0.1uF
VCC_BATT
J27
2x1_2.54mm
MOUNTING HOLES
MOUNTING HOLES
2.5mm MOUNTING HOLES
2.5mm MOUNTING HOLES
XMC MOUNTING HOLES
MH15 MH20 MH21 MH22 MH23 MH24
MH2 MH3 MH4 MH5
MH6 MH7 MH8 MH9 MH11
MH16 MH17 MH18 MH19
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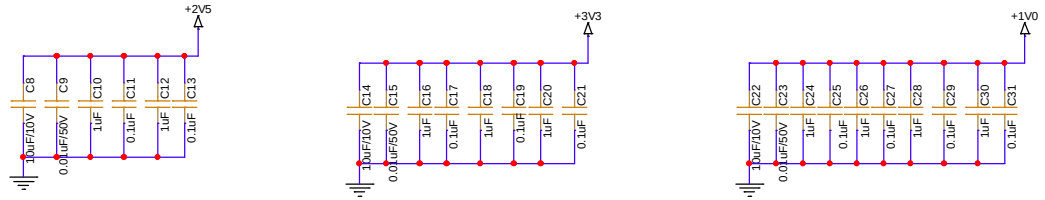
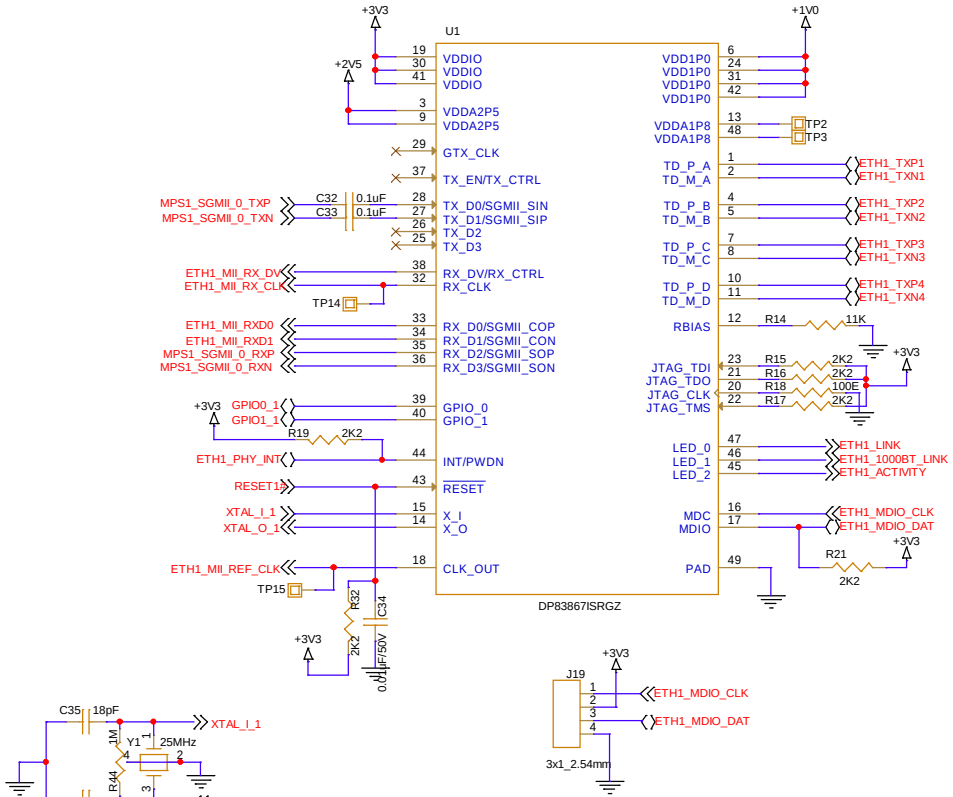
of
9

ETHERNET PHY



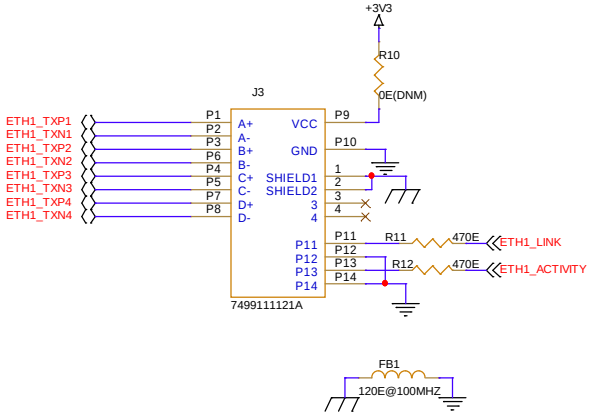
NOTE: place 1uf and 0.1uf near to every Power pins



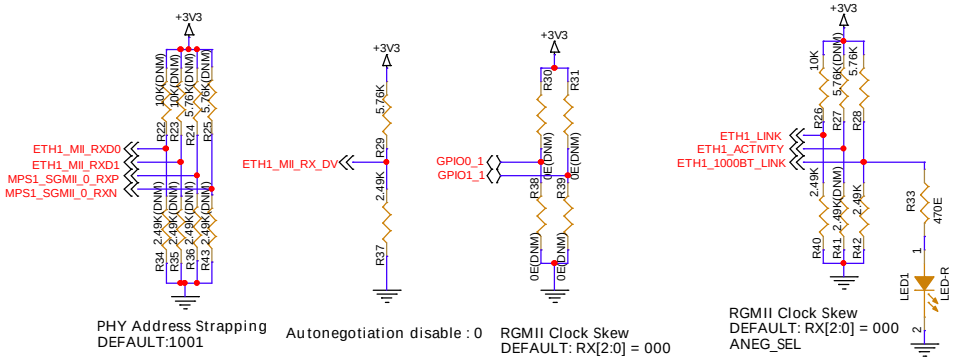
STRAP CONFIGURATION RESISTOR VALUES FOR DIFFERENT MODES

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
1	0	0	0.098 × VDDIO	OPEN	OPEN
2	0.140 × VDDIO	0.165 × VDDIO	0.191 × VDDIO	10	2.49
3	0.225 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

ETHERNET CONNECTOR



STRAP CONFIGURATION



PHY Address Strapping
DEFAULT:1001

Autonegotiation disable : 0

RGMII Clock Skew
DEFAULT: RX[2:0] = 000

RGMII Clock Skew
DEFAULT: RX[2:0] = 000
ANEG_SEL

PLACE CONFIURTION RESISTOR CLOSE TO IC PIN

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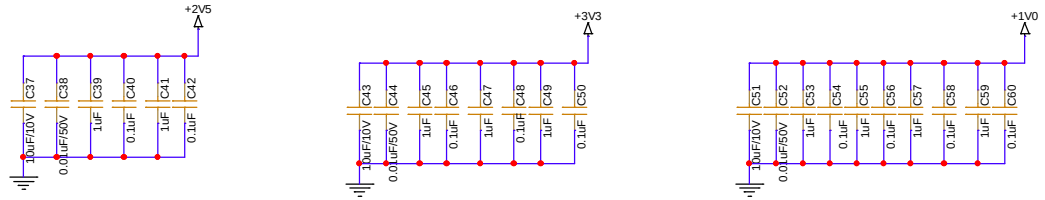
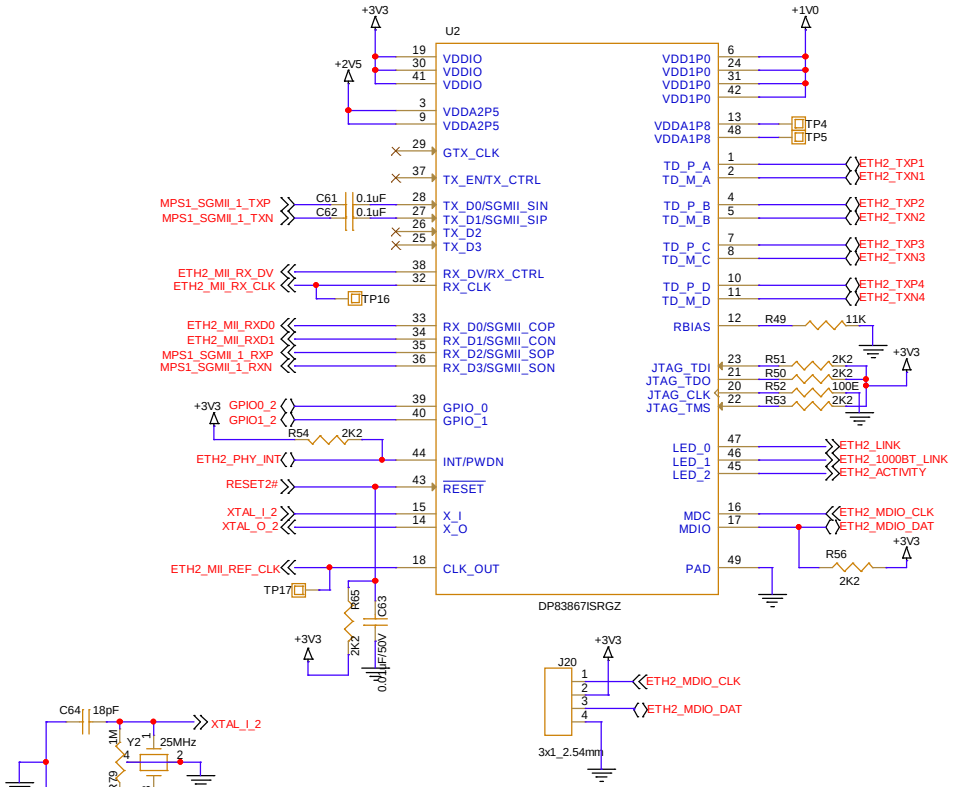
ETHERNET PHY



NOTE: place 1uf and 0.1uf near to every Power pins



STRAP CONFIGURATION RESISTOR VALUES FOR DIFFERENT MODES

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
1	0	0	0.098 × VDDIO	OPEN	OPEN
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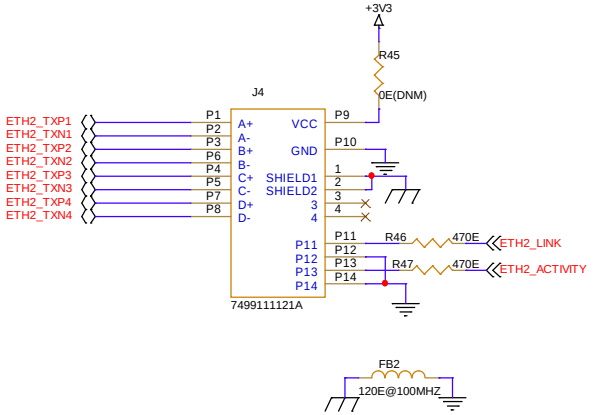
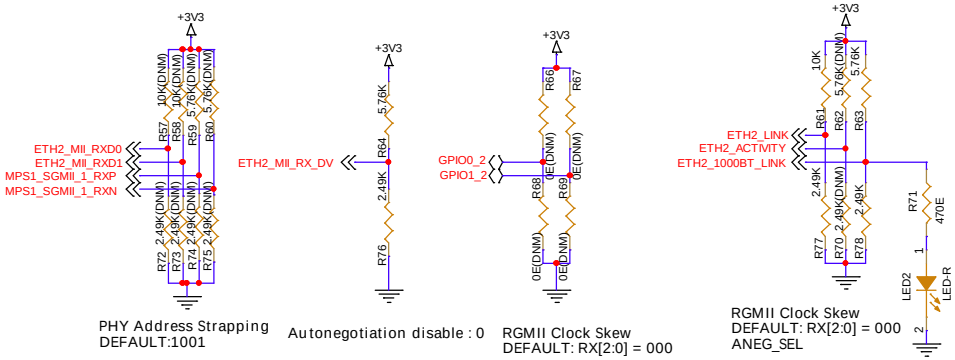
3	0.225 × VDDIO	0.255 × VDDIO	0.284 × VDDIO	5.76	2.49
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

ETHERNET CONNECTOR



STRAP CONFIGURATION



PHY Address Strapping
DEFAULT:1001

Autonegotiation disable : 0

RGMII Clock Skew
DEFAULT: RX[2:0] = 000

RGMII Clock Skew
DEFAULT: RX[2:0] = 000
ANEG_SEL

PLACE CONFIURTION RESISTOR CLOSE TO IC PIN

Title	<Title>		
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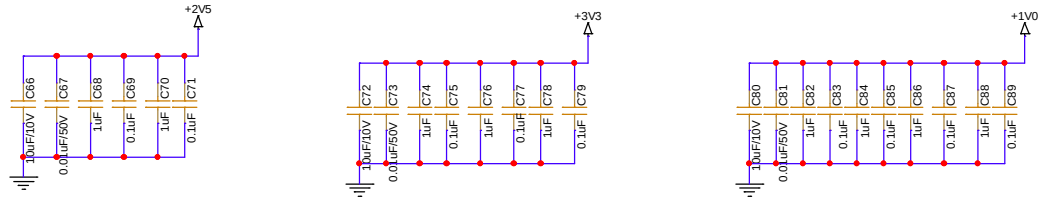
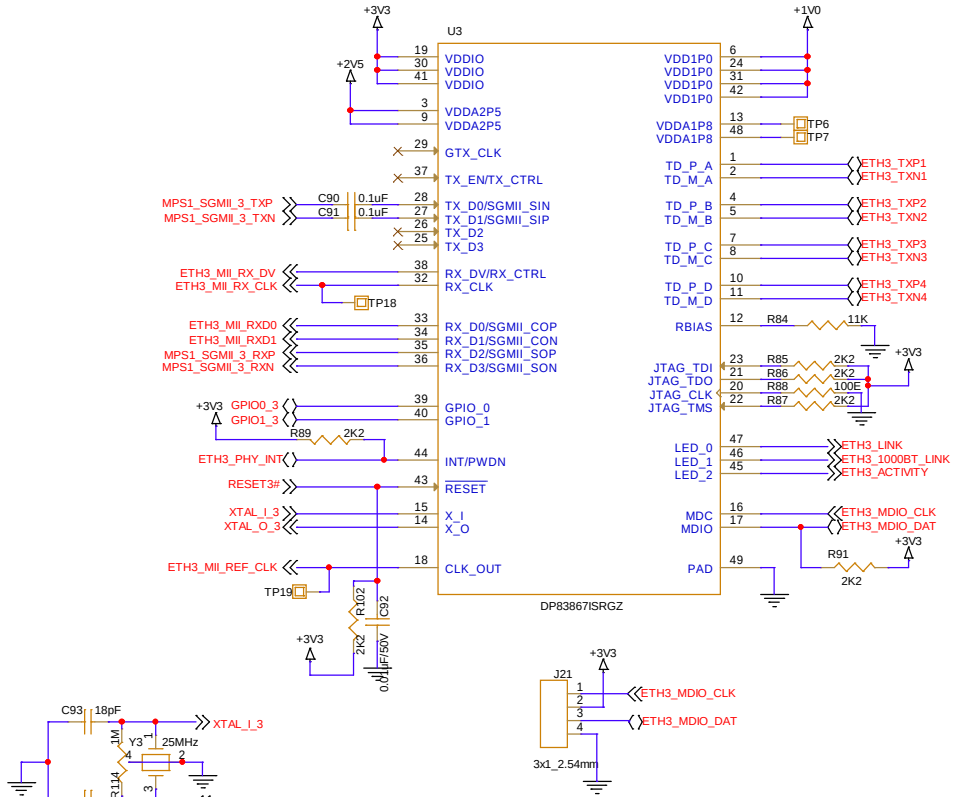
ETHERNET PHY



NOTE: place 1uf and 0.1uf near to every Power pins



STRAP CONFIGURATION RESISTOR VALUES FOR DIFFERENT MODES

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
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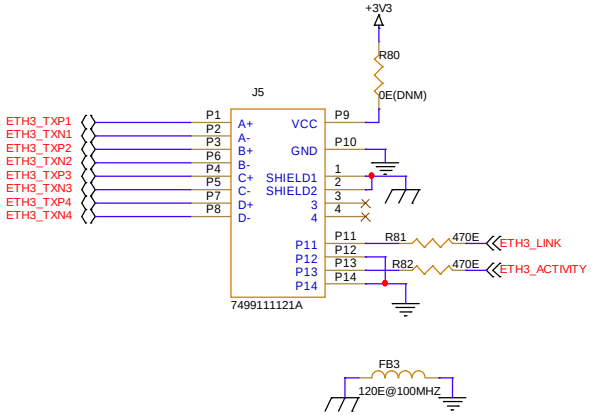
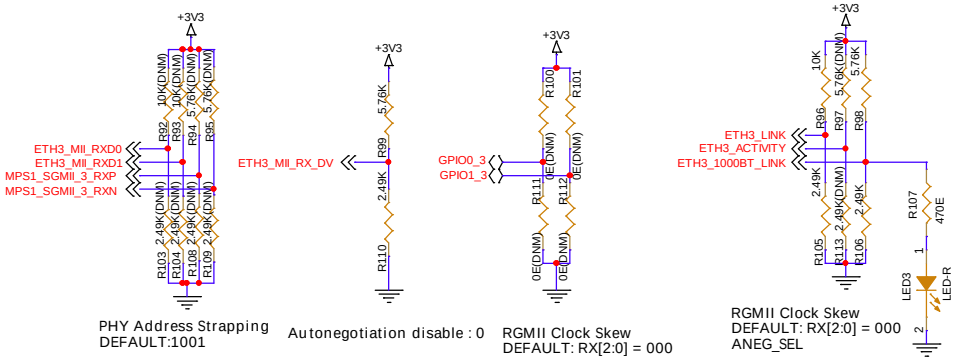
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

ETHERNET CONNECTOR



STRAP CONFIGURATION



PHY Address Strapping
DEFAULT:1001

Autonegotiation disable : 0

RGMII Clock Skew
DEFAULT: RX[2:0] = 000

RGMII Clock Skew
DEFAULT: RX[2:0] = 000
ANEG_SEL

PLACE CONFIURTION RESISTOR CLOSE TO IC PIN

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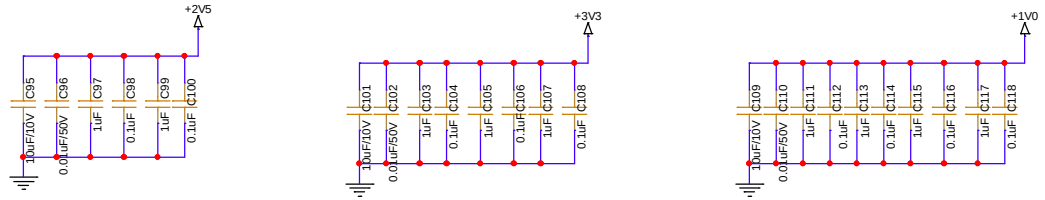
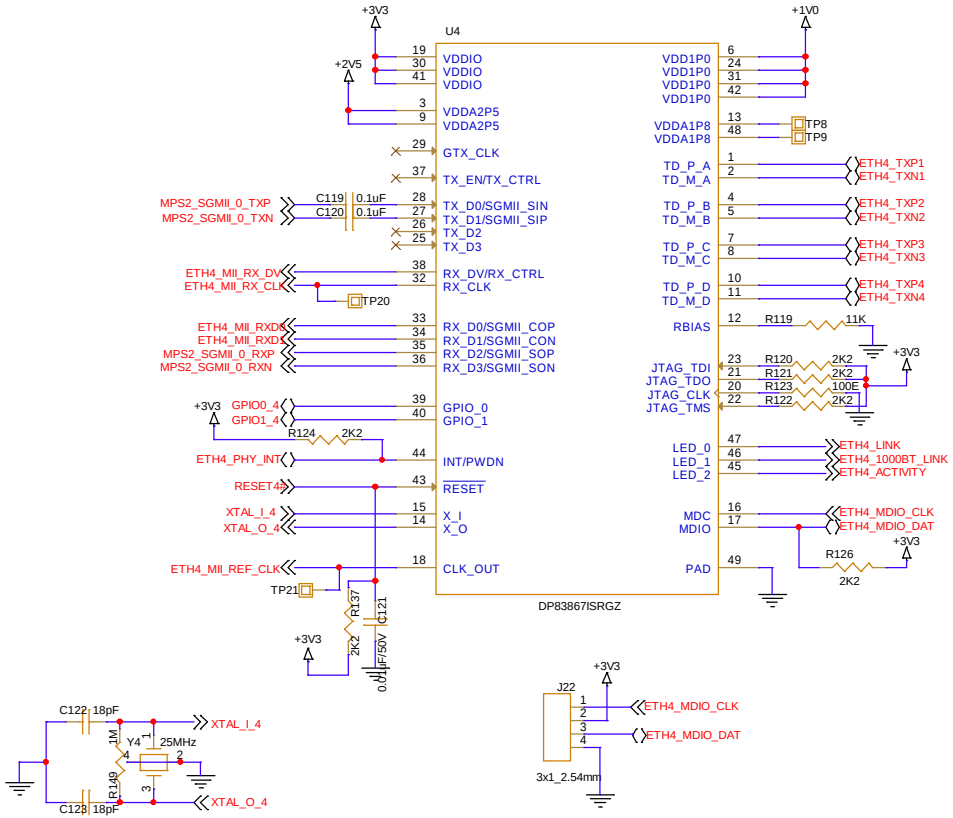
ETHERNET PHY



NOTE: place 1uf and 0.1uf near to every Power pins



STRAP CONFIGURATION RESISTOR VALUES FOR DIFFERENT MODES

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
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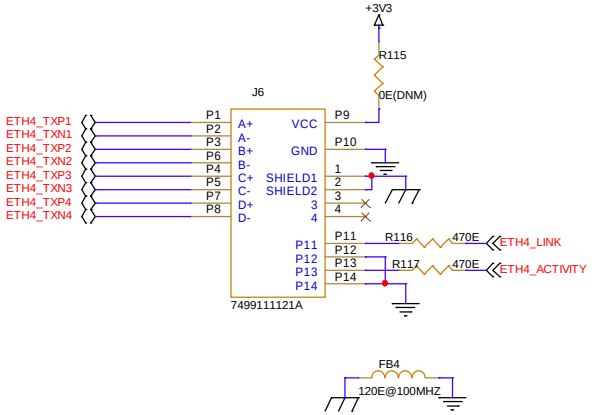
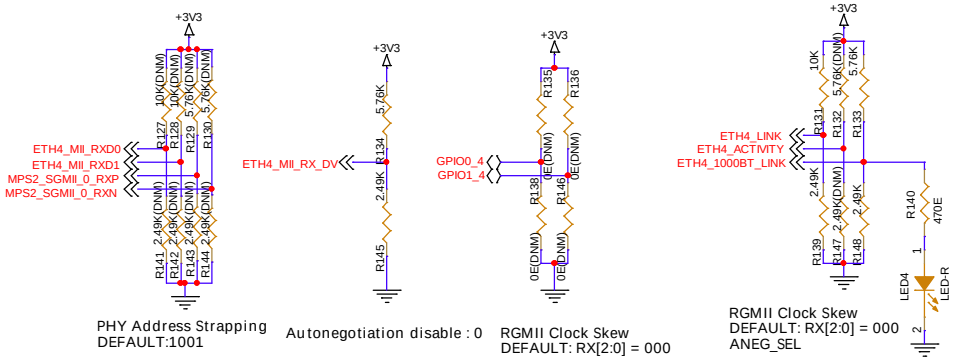
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

ETHERNET CONNECTOR



STRAP CONFIGURATION



PHY Address Strapping
DEFAULT:1001

Autonegotiation disable : 0

RGMII Clock Skew
DEFAULT: RX[2:0] = 000

RGMII Clock Skew
DEFAULT: RX[2:0] = 000
ANEG_SEL

PLACE CONFIURTION RESISTOR CLOSE TO IC PIN

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Size A3	Document Number <Doc>		Rev <RevCode>
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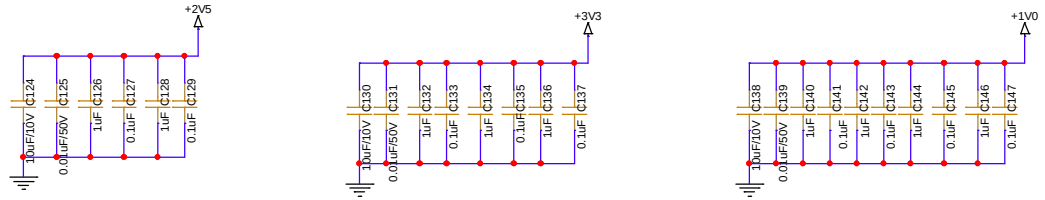
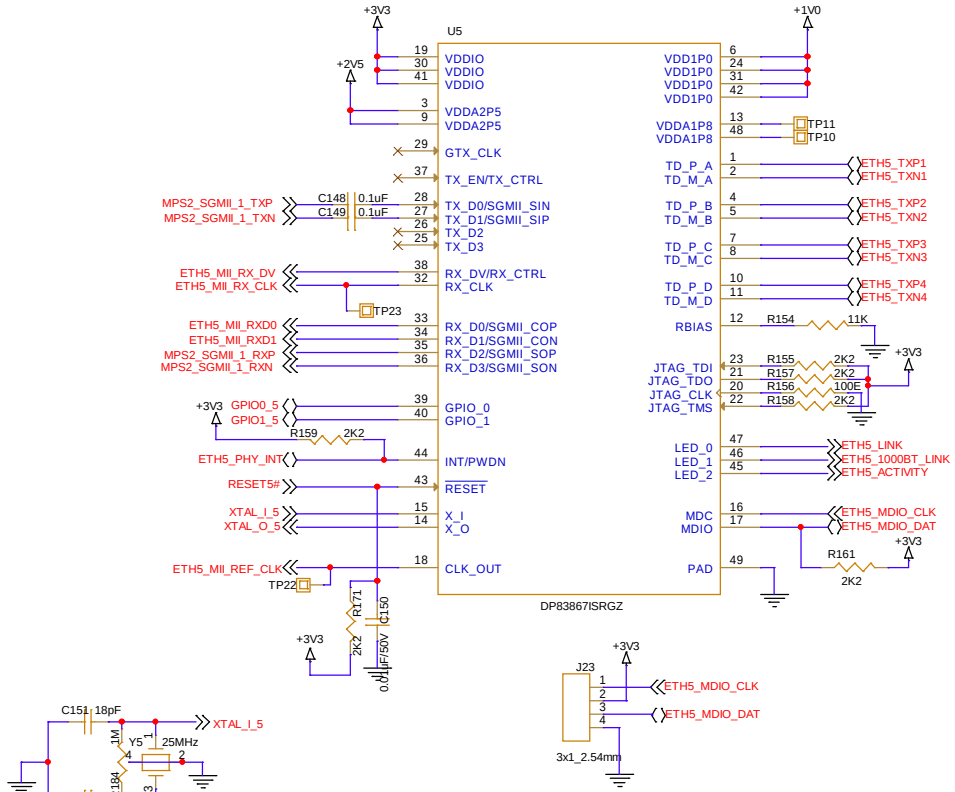
ETHERNET PHY



NOTE: place 1uf and 0.1uf near to every Power pins



STRAP CONFIGURATION RESISTOR VALUES FOR DIFFERENT MODES

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
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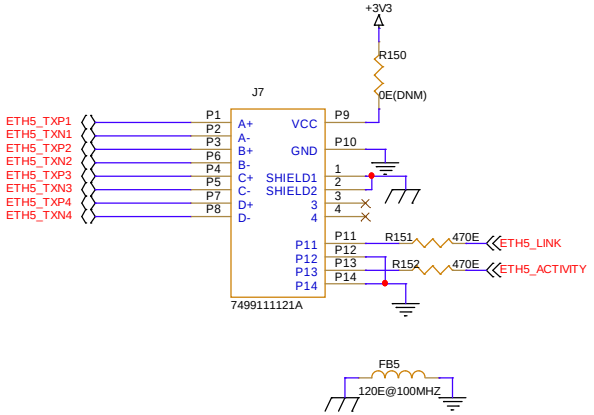
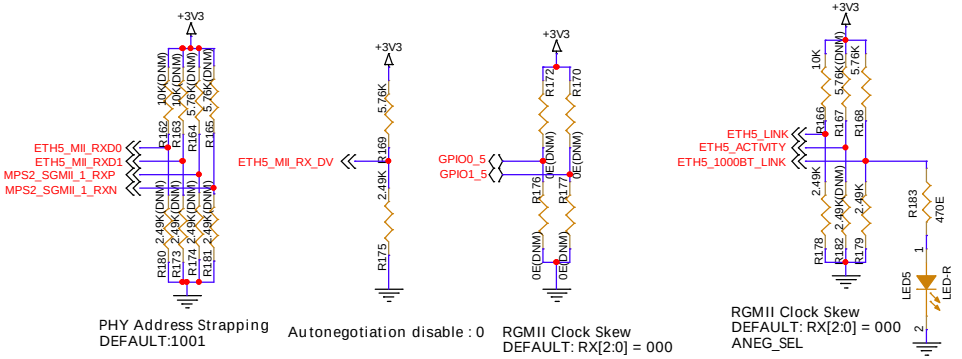
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

ETHERNET CONNECTOR



STRAP CONFIGURATION



PHY Address Strapping
DEFAULT:1001

Autonegotiation disable : 0

RGMII Clock Skew
DEFAULT: RX[2:0] = 000

RGMII Clock Skew
DEFAULT: RX[2:0] = 000
ANEG_SEL

PLACE CONFIURTION RESISTOR CLOSE TO IC PIN

Title	<Title>
Size A3	Document Number <Doc> Rev <RevCode>
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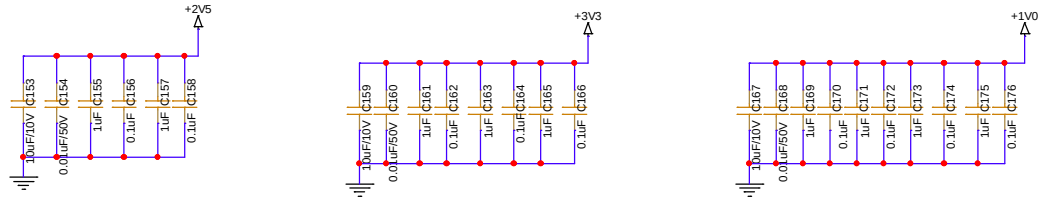
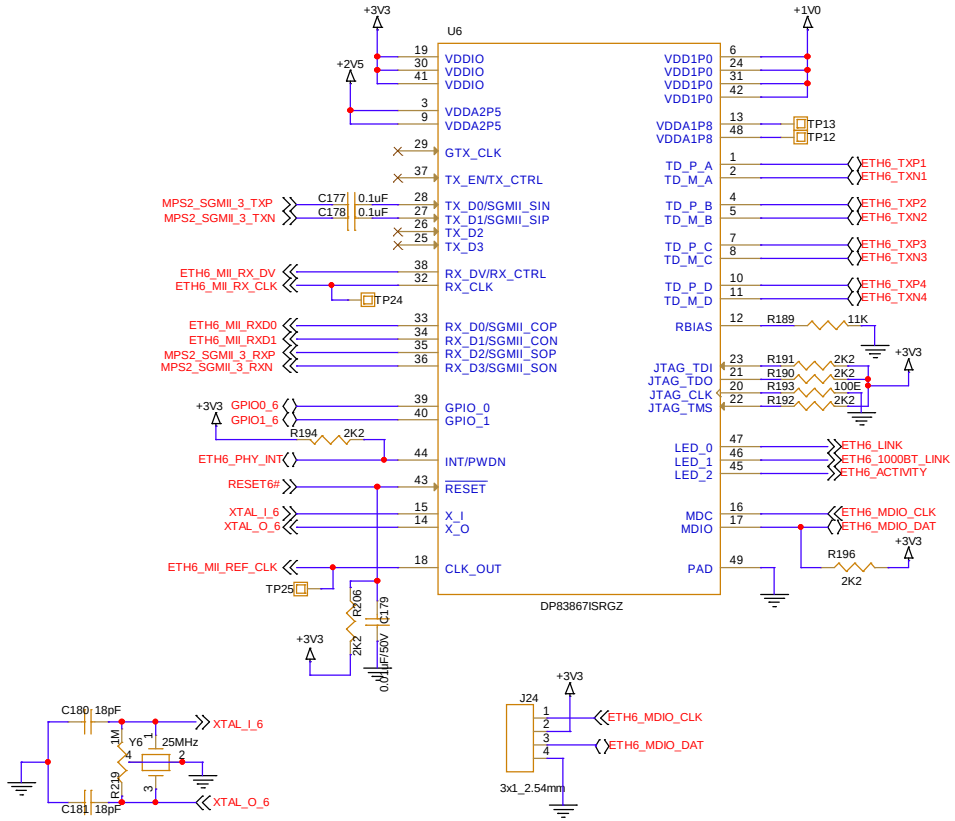
ETHERNET PHY



NOTE: place 1uf and 0.1uf near to every Power pins



STRAP CONFIGURATION RESISTOR VALUES FOR DIFFERENT MODES

MODE	TARGET VOLTAGE			IDEAL Rhi (kΩ)	IDEAL Rlo (kΩ)
	Vmin (V)	Vtyp (V)	Vmax (V)		
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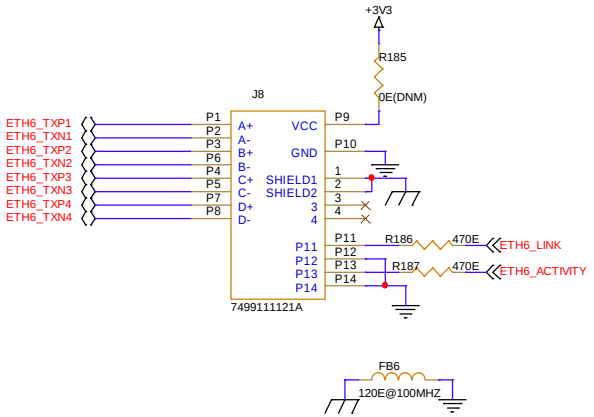
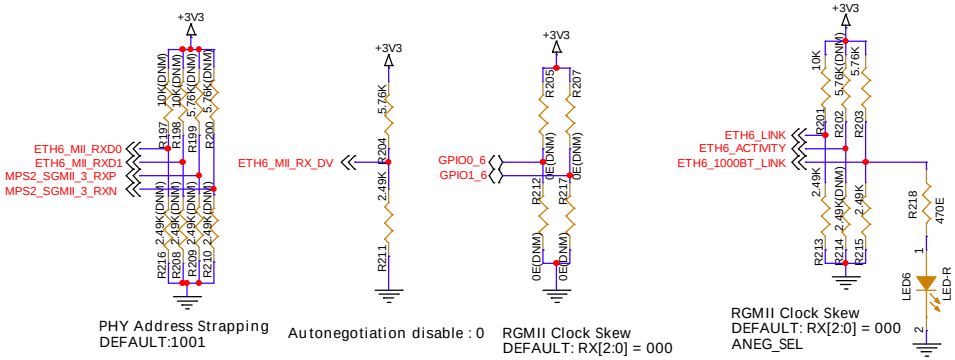
4	0.694 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

ETHERNET CONNECTOR



STRAP CONFIGURATION



PHY Address Strapping
DEFAULT:1001

Autonegotiation disable : 0

RGMII Clock Skew
DEFAULT: RX[2:0] = 000

RGMII Clock Skew
DEFAULT: RX[2:0] = 000
ANEG_SEL

PLACE CONFIURTION RESISTOR CLOSE TO IC PIN

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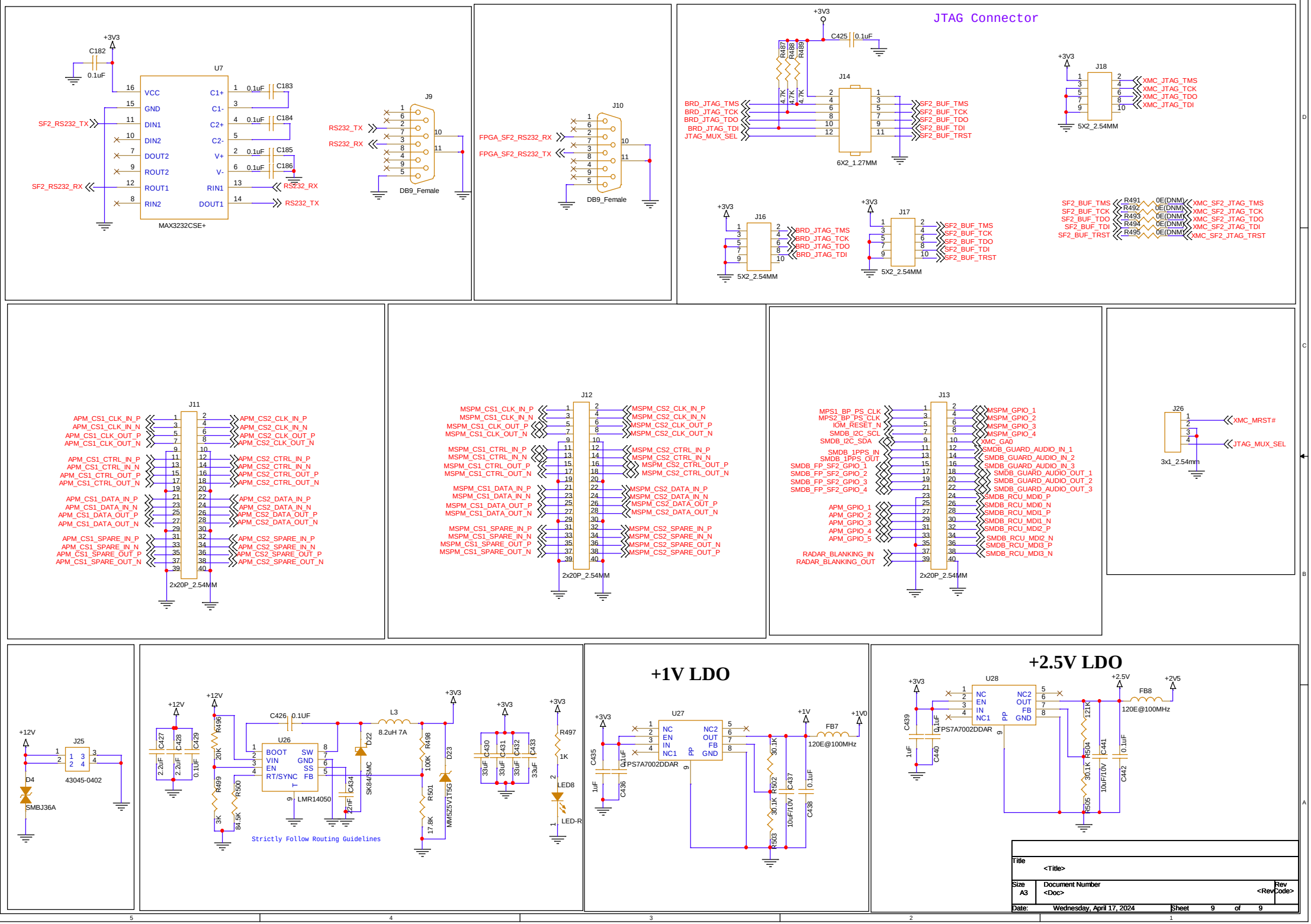
JTAG Connector
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+2.5V LDO
U7
MAX3232CSE+
J9
DB9_Female
J10
DB9_Female
J14
6X2_1.27MM
J18
5X2_2.54MM
J16
5X2_2.54MM
J17
5X2_2.54MM
J11
2x20P_2.54MM
J12
2x20P_2.54MM
J13
2x20P_2.54MM
J26
3x1_2.54mm
J25
43045-0402
U26
LMR14050
U27
PS7A7002DDAR
U28
PS7A7002DDAR
Strictly Follow Routing Guidelines
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